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Method Article

Fabrication methods for high reflectance dielectric-metal point contact rear mirror for optoelectronic devices

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A B S T R A C T

The patterned dielectric back contact (PDBC) structure can be used to form a point-contact architecture that features a dielectric spacer with spatially distributed, reduced-area metal point contacts between the semiconductor back not recognized contact layer and the metal back contact. In this structure, the dielectric-metal region provides higher reflectance and is electrically insulating. Reduced-area metal point contacts provide electrical conduction for the back contact but typically have lower reflectance. The fabrication methods discussed in this article were developed for thermophotovoltaic cells, but they apply to any III-V optoelectronic device requiring the use of a conductive and highly reflective back contact. Patterned dielectric back contacts may be used for enhanced sub-bandgap reflectance, for enhanced photon recycling near the bandgap energy, or both depending on the optoelectronic application. The following fabrication methods are discussed in the article

- PDBC fabrication procedures for spin-on dielectrics and commonly evaporated dielectrics to form the spacer layer.
- Methods to selectively etch a parasitically absorbing back contact layer using metal point contacts as an etch mask.
- Methods incorporating a dielectric etch through different process techniques such as reactive ion and wet etching.

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Background

A patterned dielectric back contact (PDBC) [1] mirror is a back contact architecture with a low refractive index, low-loss dielectric spacer layer between the semiconductor back contact layer (BCL) and the back mirror metal. It is often patterned with an array of spatially distributed metal point contacts (Fig. 1), but other patterns such as line contacts are certainly also possible and is referred to as "metal reduced-area contacts." The metal reduced-area contacts contact the BCL and the metal back electrode and provide electrical conduction between them. The dielectric-back mirror metal stack forms the back mirror, a highly reflective region between the reduced-area contacts, that typically has improved reflectance compared to the reduced-area contacts. The back mirror metal is often the same material as the back electrode metal but may differ in composition from the back electrode. The contact metal in the reduced area contact regions is often the same material as the back electrode metal but may also differ in composition from the back electrode metal and the back mirror metal. In the designs discussed here, the back mirror region is vertically non-conductive between the BCL and the back mirror metal, perpendicular to the plane of the device back surface, but the semiconductor BCL, back mirror metal, and back electrode metal are all laterally conductive along the plane of the device back surface.

The PDBC mirror can be used in semiconductor optoelectronic devices to improve rear reflectance. In photovoltaics [2–4], and LEDs [5] a PDBC mirror is used in part to improve rear reflectance of band edge emitted photons to boost photon recycling and the device performance. In thermophotovoltaics [6–9], the key function of the PDBC mirror is to improve rear reflectance in the incident broadband sub-bandgap spectrum to improve thermophotovoltaic conversion efficiency. These PDBC mirrors are also useful in solar thermal absorbers [10], to enhance solar absorptance and to minimize thermal emittance.

Multiple articles introduce PDBC [2–4] fabrication methods for various applications. In this article, we explore PDBC fabrication methods for different dielectric materials in detail. For instance, two different methods to fabricate PDBCs with SU-8 photoresist – that can be spin-coated, photolithographically processed, and hard-baked to remain in the device permanently as a dielectric spacer – are explored. Similarly, two different methods to fabricate PDBCs with commonly evaporated dielectrics like SiO_2 and MgF_2, as well as stacks of these dielectrics are also explored. The initial photolithography fabrication conditions are adapted from the manufacturer product specifications and are later experimentally optimized for the feature dimensions. These PDBC fabrication methods are developed with an eye for both commercial deployment with simple process flows, and for laboratory-scale use with improved flexibility. The equipment set used in this study includes: a spin coater and hotplate from Cost Effective Equipment (CEE); a tabletop photolithography exposure tool from ABM systems; a PlasmaPro 100 COBRA reactive ion etch tool from Oxford instruments; dielectric

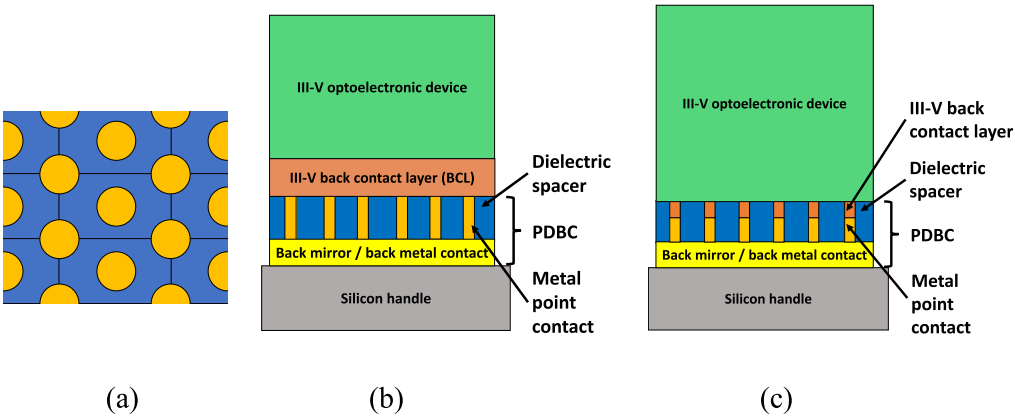


Fig. 1. (a) Plan-view schematic of the patterned dielectric back contact layer. Yellow discs are the spatially distributed point contacts, and the blue region is the dielectric spacer. Figures illustrating III-V optoelectronic devices with (b) III-V BCL intact; and (c) III-V BCL selectively etched patterned dielectric back contacts are shown.

deposition using a custom-built physical vapor deposition tool from Angstrom Engineering; and metal evaporation using Temescal FC2000 e-beam evaporation tool.

PDBC fabrication procedures

The PDBC fabrication process flows discussed in this article are generally applicable in full or part to semiconductor devices requiring a PDBC mirror or a reduced area contact device architecture. However, these processes were mainly designed with a focus on III-V optoelectronic devices, specifically, thermophotovoltaic cells. Each process flow has its advantages and disadvantages, that we summarize toward the end of the article in Table 6. A sub-group of these process flows are dielectric-specific or are specific to the back contact layer (BCL) selective etch used (Fig. 1). The primary purpose of a BCL selective etch (Fig. 1c) is to reduce parasitic light absorption in the epitaxial stack, increasing both sub-bandgap reflectance [1,5,6] and photon recycling [11,12], both of which can be important in different optoelectronic applications. Based on the selection of dielectric spacer between BCL and back mirror, the processes are broadly classified as process A (for spin-on dielectrics), and process B (for other commonly evaporated dielectrics) (Fig. 2).

Process A for SU-8 photoresist as dielectric

Process A (Fig. 3) is designed for SU-8 photoresist as a dielectric spacer. As pointed out in the previous section, several optoelectronic applications benefit from a selective etch of the highly doped BCL such that the BCL is present only between the semiconductor device and the metal point contacts (Fig. 1b). Etching highly doped layers can enhance sub-bandgap reflectance by reducing free carrier absorption and can enhance photon recycling by reducing band-edge absorption if the band edge energy of the BCL is similar to or lower than that of the active layer. The main purpose of highly doped BCL in these applications is to provide low specific contact resistivity to the metal point contacts and not necessarily to participate in lateral current transport. Depending on whether or not the BCL is etched, process A is classified into process A1 that does not support a BCL selective etch, and A2 that does support a BCL selective etch.

Process A1 for depositing SU-8 photoresist first

In the A1 process (Fig. 3a,b), SU-8 is spin-coated on the BCL, and vias extending through to the BCL are photolithographically patterned and developed. The vias are electroplated with the metals used to make electrical contact, followed by evaporated or sputtered metal to fabricate the back mirror.

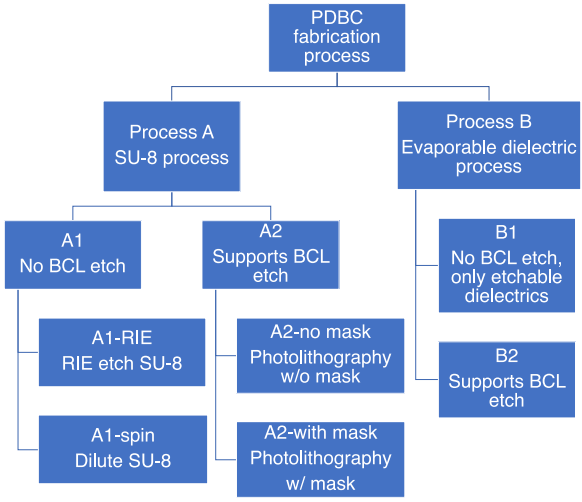


Fig. 2. Classification of PDBC fabrication processes.

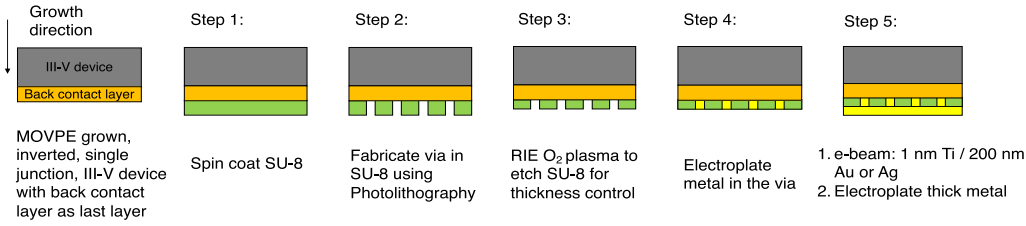
Table 1
Process details in process A1-RIE, for 100% SU-8.

Step	Equipment	Details	Comments
Photolithography to define via on 100% SU-8			
Spin-coat SU-8 6000.5	Spin-coater	1. 500 RPM, 5 s, 500 RPM/s 2. 6000 RPM, 36 s, 1000 RPM/s 3. 0 RPM, 6 s, 1000 RPM/s	SU-8 thickness 433 nm
Soft bake	Hot plate	100°C, 60 s	Hotplate surface temperature
Photolithography	Contact aligner/ stepper, photomask	76 mJ/cm^2, 365 nm (i-line) UV (Varies with SU-8 thickness)	Use index matching fluid to improve contact between SU-8 and mask and create hard-contact in the case of contact aligner.
Post-exposure bake	Hot plate	100°C, 120 s	Hotplate surface temperature
Develop in SU-8 developer	Wet bench	30 s	Vigorous swish. Wash developer in IPA, blow dry IPA in N_2
Hard bake	Hot plate	100°C, 30 mins	Hotplate surface temperature
Etch-back of the SU-8 to Desired Thickness			
SU-8 thickness control etch	RIE-ICP tool	RF power 50 W, ICP power 300 W, 50 sccm O_2, 10 mT, He backed substrate cooling at 10 torr	Refer Fig. 4a for SU-8 etch thickness as a function of time

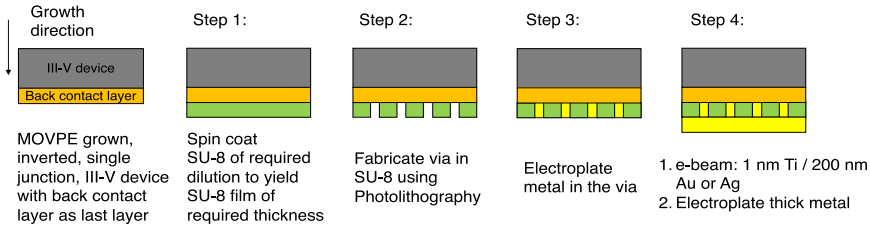
Many optoelectronic applications require adjusting the optical interference condition depending on the need to selectively reflect or transmit at the required wavelengths. Thickness control in the dielectric layer of the PDBC can be used in this way to engineer the optical interference condition as required. In process A1, two different approaches are considered to control the SU-8 thickness: A1-RIE and A1-spin

In process A1, SU-8 6000.5 from MicroChem is used and is hereafter referred to as 100% SU-8. In A1-RIE, a thick, as-spun, SU-8 film is etched back to the desired thickness using reactive ion etching. In A1-spin, the SU-8 6000.5 is diluted using CPG thinner from MicroChem to a concentration that will directly yield the desired thickness after spin-coat.

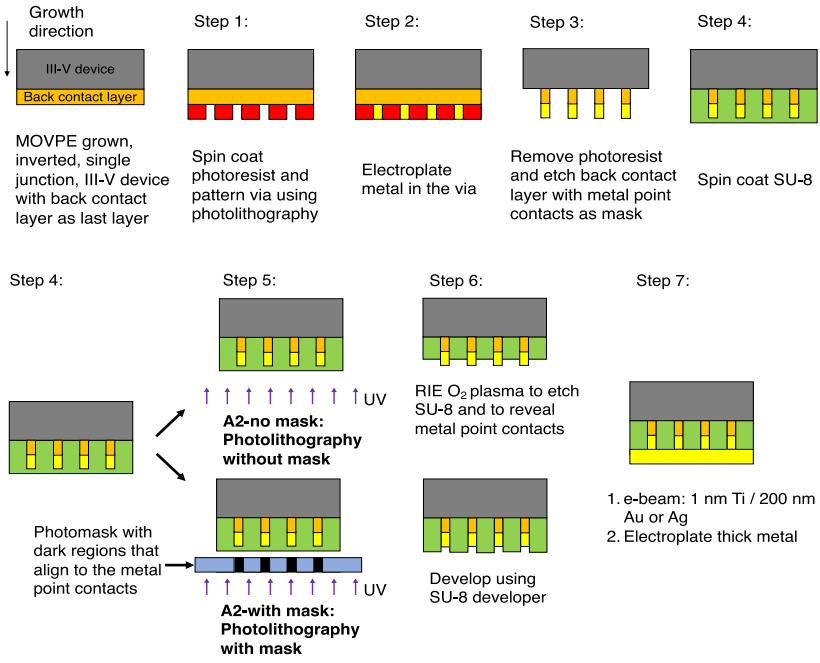
In process A1-RIE (Fig. 3a), we spin-coat, photolithographically process, and hard-bake the 100% SU-8, as shown in the recipe in Table 1. Since the SU-8 is a negative photoresist, the UV exposed region stays, and the unexposed region clears after development. Thus, a via or a clear region in the SU-8 after development corresponds to a dark region on the photomask. The smallest diameter via we were able to fabricate on 100% SU-8 was 3 μm on a 675-μm-thick Si substrate and 5 μm on a



(a)



(b)



(c)

Fig. 3. Schematic of PDBC fabrication process flow A, used primarily for SU-8 photoresist as the dielectric layer. Process A1 for SU-8 first process (a) A1-RIE – thickness control through RIE; (b) A1-spin – thickness control through SU-8 dilution; and (c) process A2 for metal point contact first process; for a structure in which the back contact layer is etched everywhere except at the point contacts; and shows the two different sub-processes A2-no mask and A2-with mask in steps 5, 6.

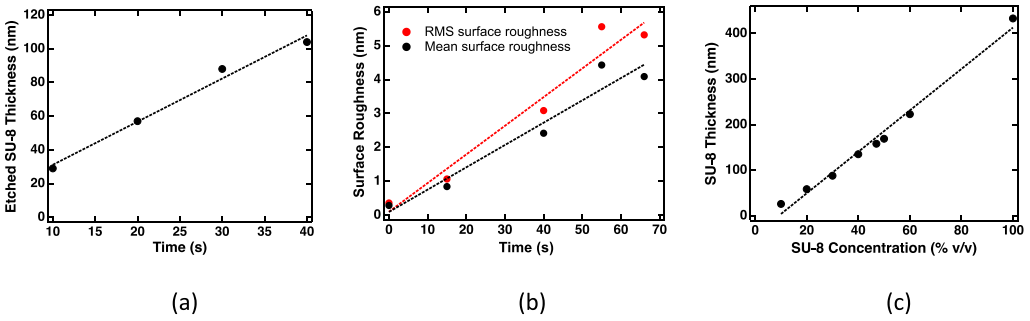


Fig. 4. (a) Etched SU-8 thickness as a function of RIE-ICP etch time in RF power 50 W, ICP power 300 W, 50 sccm O_2 flow, 10 mT chamber pressure in O_2 plasma with He backed substrate cooling at 10 torr (b) Mean, and RMS surface roughness measured using AFM (c) SU-8 thickness as a function of SU-8 concentration diluted in CPG thinner, spin-coated at 6000 RPM after hardbake at 100°C for 30 mins. Dashed lines in the figures indicate linear fits to the data.

325-μm-thick GaAs substrate using contact photolithography, and deionized (DI) water as an index-matching fluid during exposure. The substrate-photomask contact is better for thicker substrates than thinner substrates in contact photolithography.

After the hardbake, the SU-8 is etched [13] to the desired thickness using reactive ion etching (RIE) in inductively coupled plasma (ICP) mode using the recipe listed in Table 1. The etched SU-8 thickness has a linear dependence on the etch time as shown in Fig. 4a for the RIE-ICP recipe listed in Table 1. The advantage of this approach is that any SU-8 residue in the via is also etched away, creating a cleaner semiconductor surface for better electrical contact.

However, etching induces surface roughness on SU-8 which may lead to light scattering at the interface with the subsequently deposited metal mirror and thus higher absorption in the device. The mean and RMS surface roughness on the 100% SU-8 surface measured using atomic force microscopy (AFM) at different etch times are shown in Fig. 4b. The average surface roughness on as-spun 100% SU-8 is 0.36 nm, and it increases by ~15X to 5.32 nm after a 66 s RIE-ICP etch in O_2 plasma. The surface roughness indicates the height difference between peaks and valleys, but scattering is determined by the periodicity of the peaks and valleys in the lateral direction. So, the higher surface roughness may or may not directly correspond to increased scattering. One advantageous effect of process A1-RIE is that higher surface roughness promotes adhesion [14] between SU-8 and the back metal contact.

In process A1-spin (Fig. 3b), SU-8 is diluted using CPG thinner to achieve the desired thickness as-spun. Fig. 4c shows SU-8 thickness at different % volume/volume (%v/v) concentrations diluted in CPG thinner and spin-coated at 6000 RPM. The average SU-8 thickness is 223 nm at 60% v/v and this composition is hereafter referred to as 60% SU-8. The recipe to photolithographically fabricate 60% SU-8 film with via regions for point contacts is listed in Table 2. The UV exposure dose depends on the thickness of the SU-8 film and this data is not completely available for SU-8 compositions other than 60% and 100%. The photomask is the same as the one described in process A1-RIE. The average surface roughness measured using AFM is 0.19 nm on as-spun 60% SU-8, which is approximately two times lower than the average surface roughness of 0.36 nm on as-spun 100% SU-8, and far lower than the surface roughness of 100% SU-8 after RIE etching.

The SU-8 film thickness varies linearly with % v/v composition between 10% and 100%, and at 10% v/v SU-8 composition the average SU-8 film thickness is only 26 nm. Thus, SU-8 can be used as a replacement to SiO_2, due to their similar refractive indices [1], in cases in which thermal / e-beam evaporation of SiO_2 results in detrimental effects on the device.

The disadvantage of A1-spin is that it can be difficult to get good contact between a thin SU-8 film and the photomask in contact photolithography if the substrate is thin or has curvature. Poor contact can illuminate nominally dark resist areas through scattering, diffraction, or reflection. Therefore, the development of narrow spaces becomes difficult. This can be ameliorated by using index matching fluid between the SU-8 and photomask, through hard vacuum contact, and/or by using

Table 2
Process details in process A1-spin, for 60% SU-8.

Step	Equipment	Details	Comments
Photolithography to define via on 60% SU-8			
Spin-coat 60% SU-8 6000.5	Spin-coater	1. 500 RPM, 5 s, 500 RPM/s 2. 6000 RPM, 36 s, 1000 RPM/s 3. 0 RPM, 6s, 1000 RPM/s	SU-8 thickness 223 nm
Soft bake	Hot plate	100°C, 60 s	Hotplate surface temperature
Photolithography	Contact aligner/ stepper, photomask	329 mJ/cm^2, 365 nm (i-line) UV (Changes with SU-8 composition/thickness)	Use index matching fluid to improve contact between SU-8 and mask and create hard-contact in the case of contact aligner.
Post-exposure bake	Hot plate	100°C, 120 s	Hotplate surface temperature
Develop in SU-8 developer	Wet bench	30 s	Vigorous swish. Wash developer in IPA, blow dry IPA in N_2
Hard bake	Hot plate	100°C, 30 mins	Hotplate surface temperature

a photolithographic stepper instead of the aligner. With the 60% SU-8 in process A1-spin, the smallest diameter via we were able to fabricate was 5 µm on a 675 µm-thick Si substrate and 7 µm on 325 μm-thick GaAs substrate using contact photolithography, and DI water as an index-matching fluid.

Importantly, we found that 325-μm-GaAs substrates bend away from the photomask due to the force of the substrate vacuum, creating poor contact between SU-8 and the photomask. However, substrate vacuum is necessary to detach the thin GaAs substrate from the photomask, bound by the capillary action of the index matching fluid, after exposure. A satisfactory process to overcome these issues is to turn off the substrate vacuum right before exposure to create good contact between photomask and substrate, and then turn on the substrate vacuum to detach the substrate from the photomask.

Process A2 for forming metal point contacts first

In the A2 process (Fig. 3c), the metal point contacts are fabricated first, on the semiconductor BCL, followed by an optional selective etch of BCL using the metal point contacts as a mask, fabrication of the SU-8 dielectric spacer, and deposition of the back mirror. This process is preferred if the BCL must be selectively etched or if fabrication of a smaller diameter via or residue-free via through the SU-8 is difficult using process A1. As the metal point contacts are fabricated first in process A2, this process should be expected to result in better electrical contact. As the SU-8 is spin-coated after metal point contact fabrication, the SU-8 may completely or partially engulf the metal point contacts. So, the SU-8 on top of the metal point contacts must be removed to get electrical contact between the metal point contacts and the back mirror. In process A2, two different approaches, A2-no mask and A2-with mask, are considered for selectively removing the SU-8 on top of the metal point contacts for electrical contact. In A2-no mask, the SU-8 on top of the metal point contacts is cleared by reactive ion etching. In A2-with mask, the SU-8 on top of the metal point contacts is cleared through photolithography.

In process A2, a removable photoresist is spin-coated on the BCL, patterned, and developed with photolithography to fabricate vias extending through to the BCL. Any photoresist compatible with the via feature size, that can be stripped off after electroplating, can be used. In this study, Shipley S1818 positive photoresist is used. The spin-coat and photolithography recipes to fabricate vias in S1818 are listed in Table 3. In a positive photoresist, the regions that are exposed to UV are cleared, while the unexposed regions remain after development. So, the clear region in the photomask corresponds to the via region in the S1818 photoresist.

After via development, the metals for electrical contact are electroplated in the vias to fabricate the metal point contacts. Then the photoresist is stripped (the S1818 strip recipe is listed in Table 3). With these metal point contacts as masks, the BCL can be etched everywhere except the metal point contacts using a suitable selective etchant [15,16]. In this study 2:1:50 NH_4OH:H_2O_2:H_2O for 5 s was used to etch the p-AlGaAs BCL. The BCL selective etch can also be done through a suitable reactive ion etch (RIE) recipe [17]. After BCL etch, we spin-coated 100% SU-8 on the surface with metal point contacts. Depending on the spin-speed and metal point contact height, the SU-8 may or may not completely cover the metal point contacts. Two different process approaches, namely: A2-no mask –

Table 3
Process details to fabricate features in S1818 positive photoresist and to strip S1818 photoresist.

Step	Equipment	Details	Comments
Photolithography to define S1818 photoresist film with vias			
Spin-coat Shipley S1818	Spin-coater	4000 RPM, 30 s, 800 RPM/s	Approximately 1μm thick film
Soft bake	Hot plate	100°C, 5 min	Hotplate surface temperature
Photolithography	Contact aligner/ stepper, photomask	75 mJ/cm^2, 365 nm (i-line) UV	Use index matching fluid to improve the contact between photoresist and mask and create hard contact in the case of contact aligner.
Develop in MF CD-26 developer	Wet bench	30 s	Wash developer off in D.I. water and blow dry water in N_2
S1818 photoresist wet strip process			
Remove S1818 after metal point contact fabrication	Wet bench	Acetone, IPA, N_2 blow dry	Acetone removes S1818, IPA removes acetone, N_2 evaporates IPA

photolithography without photoresist mask, and A2-with mask – photolithography with a photoresist mask is explored to clear out the SU-8 on top of the metal point contacts for electrical contact to the back mirror/back metal contact, as shown in steps 5-7 of Fig. 3c.

In A2-no mask, we hard-bake the SU-8 and etch it in RIE-ICP O_2 plasma (Fig. 4a) to reveal the metal point contacts.

In A2-with mask, the metal point contact areas are revealed using photolithography. For negative photoresist, this involves the somewhat difficult step of aligning a photomask containing dark discs to the metal point contacts on the sample. This photomask is essentially an inverted design of the photomask used for fabricating vias on the S1818 positive photoresist in step 1. After photomask alignment, UV exposure, and development, the SU-8 on top of the metal point contacts is cleared, using the same recipe as in process A1-RIE listed in Table 1.

In both of the approaches for process A2, the RIE-ICP etch in step 6 (Fig. 4a) can be used to control the SU-8 thickness to engineer the optical interference conditions. Finally, the back mirror is fabricated by metal evaporation or sputtering.

For process A2 to work effectively, the SU-8 film after spin-coating should be thicker than the metal point contacts. Otherwise, the SU-8 flow will interfere with the metal point contacts during the spin-coat process and result in a non-planar film, possibly resulting in light scattering and thus undesirable absorption in the final device.

Process B for evaporable dielectrics

Process B is designed for fabricating PDBCs with evaporable dielectrics like SiO_2, MgF_2, ZnS, etc. Process B is further classified into process B1 and process B2. Process B1 does not support BCL selective etch and is applicable only for etchable dielectric. Process B2 supports BCL selective etch and is applicable for any evaporable dielectrics.

Process B1 for etchable dielectrics with no support for BCL etch

The etch-through process B1 (Fig. 5a) is suitable only for dielectrics that can be either dry or wet etched, selective to the photoresist used and the BCL. In this process, the BCL cannot be selectively etched. Process B1 is preferred over process B2 if photoresist lift-off in the via areas after the dielectric deposition in process B2 is a problem.

In process B1, the dielectric is deposited on the BCL first. In this study, we deposit ~200 nm SiO_2 by e-beam evaporation on the BCL. A photoresist film with vias of the required dimensions is deposited and patterned on the dielectric. In this study, we use Shipley S1818 positive photoresist, and the spin-coat and photolithography recipes are listed in Table 3. The dielectric is etched with the photoresist film as an etch mask everywhere except in the via region. In this study, SiO_2 is etched with a diluted buffered oxide etch (BOE - 7:1, HF: NH_4F = 12.5: 87.5%), using the process as listed in

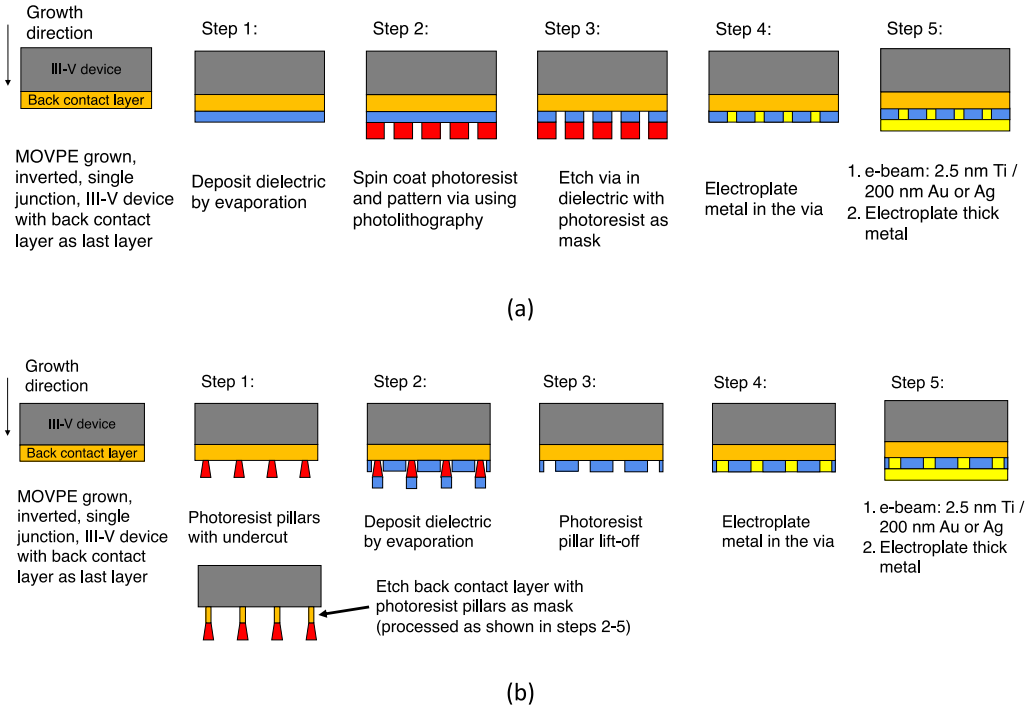


Fig. 5. Schematic of PDBC fabrication process flow B primarily for evaporable dielectrics: (a) process B1 for etchable dielectrics and no support for BCL etch; and (b) process B2 for any dielectrics that supports BCL etch.

Table 4
Process details in process B1 for etchable dielectrics.

Step	Equipment	Details	Comments
SiO_2 etch with S1818 photoresist as mask			
1:10 Buffered oxide etch (BOE):H_2O etchant	Wet bench	5 s	Wash 1:10 etchant off in D.I. water and blow dry water in N_2

Table 4. The photoresist mask is then stripped off in a suitable dry/wet stripper, leaving the dielectric with an array of patterned vias. In this study, acetone is used to strip the S1818 photoresist as listed in the strip recipe in Table 3. The metal point contacts are electroplated in the vias in the dielectric, and the back mirror is fabricated.

Process B2 for any evaporable dielectric with an option to support BCL etch

The liftoff process B2 (Fig. 5b) can be used for any evaporable dielectrics. In this process, the BCL can be optionally selectively etched with photoresist pillars as a mask.

An inversion photoresist that is processed negatively, or a negative photoresist, is spin-coated on the BCL and is photolithographically processed to reveal an array of photoresist pillars of the required dimensions with an undercut edge profile. The undercut is essential to lift off the dielectric material on top of the photoresist pillars after dielectric deposition. A negative photoresist stays in the region of UV exposure and clears in the region of no UV exposure after development. So, the photoresist pillars with undercut are fabricated at the locations of an array of clear circular areas in the photomask.

In this study, AZ5214-E from MicroChemicals GmbH, an inversion photoresist, is used for defining the photoresist pillars with an undercut. The spin-coat and photolithography recipes are listed in Table 5. A dielectric layer of the required thickness is deposited using a suitable method (thermal evaporation/ e-beam evaporation/ ALD) of deposition. The dielectric is deposited everywhere on

Table 5
Process to fabricate photoresist pillars using AZ5214-E photoresist and to lift-off AZ5214-E photoresist after dielectric deposition.

Step	Equipment	Details	Comments
Photolithography recipe to define AZ5214-E photoresist pillars with undercut			
Spin-coat AZ5214-E	Spin-coater	2500 RPM, 30 s, 2500 RPM/s	Approximately 1 μm thick photoresist film
Soft bake	Hot plate	95°C, 60 s	Hotplate surface temperature
Photolithography	Contact aligner / stepper, photomask	14.4 mJ/cm^2, 365 nm (i-line) UV	Use index matching fluid to improve contact between SU-8 and mask and create hard-contact in the case of contact aligner
Wait time	Wet bench / hood	5 mins	N_2 bubble release
Post-exposure bake	Hot plate	105°C, 60 s	Hotplate surface temperature.
Flood-expose	Contact aligner / stepper, no photomask	860 mJ/cm^2, 365 nm (i-line) UV	Image reversal
Develop in AZ300 MIF developer	Wet bench	30 s	Wash developer off in D.I. water and blow dry water in N_2
AZ5214-E photoresist lift-off recipe			
Soak in Remover PG stripper	Wet bench	20 mins on a hotplate set at 95°C	Occasional stirring
Ultrasonication in Remover PG stripper	Wet bench	20 mins	Heated / unheated water bath for ultrasonication

Table 6
Pros and cons of different PDBC fabrication process flows discussed in this study.

Process	Process sub-type	Different approaches	Pros	Cons
Process A (SU-8 process)	Process A1 (Does not support BCL etch; SU-8 first process)	A1-RIE	1. SU-8 thickness control after photolithography. 2. SU-8 etch also clears photoresist in via region (better electrical contact).	1. Dry etch (RIE-ICP) process step is required. 2. Higher SU-8 surface roughness (bad for certain applications).
		A1-spin	1. Fewer fabrication steps. 2. Dry etch is not necessary for thickness control but is possible.	1. Contact photolithography is difficult on thinner SU-8 films especially for smaller features.
	Process A2 (Supports BCL etch; metal point contact first process; better electrical contact than process A1)	A2-no mask	1. Relatively easy compared to A1-RIE because of the photomask-less metal point contact opening.	1. Dry etch (RIE-ICP) step is required for metal point contact opening.
		A2-with mask	1. Two photomasks are needed if a +ve photoresist is used for metal point contact fabrication.	1. Photomask alignment to metal point contacts is difficult.
Process B (Evaporable dielectric process)	Process B1 (No BCL etch)	NA	1. Dielectric deposition first process. So, less organic contamination on the device compared to the photoresist first process.	1. Does not support BCL etch. 2. Applicable only for etchable dielectrics.
	Process B2 (Supports BCL etch)	NA	1. Supports BCL etch. 2. Applicable for any evaporable dielectric.	1. Photoresist lift-off after dielectric deposition may sometimes be challenging.

the sample surface, including on top of the photoresist pillars. Following dielectric deposition, the dielectric on top of the photoresist pillars is lifted off using the recipe listed in Table 5. We then fabricate the metal point contacts in the vias, followed by the back mirror fabrication.

Multiple PDBC fabrication procedures are discussed in this study. These PDBC fabrication process flows have its advantages and disadvantages and are summarized in the Table 6.

Metal point contact and metal back mirror fabrication

If the stack of metals in the point contact via is different than the metals in the back mirror, electroplating of the contact metal in the vias only is a preferred process, made possible by selective electroplating only on the exposed semiconductor at the bottom of the via, rather than on the insulating dielectric. One key to high reflectance in the vias is a smooth semiconductor-metal contact interface, which can be achieved with slow electroplating rates of the metal point contacts. In addition, it is desirable to choose a metal for the contact that has high reflectance as well as low specific contact resistivity to the BCL; some metals such as Ti, Cr, and Ni have significantly lower reflectance than other metals. Some of these are metals that give low specific contact resistivity, so a tradeoff can occur between contact reflectivity and contact resistivity, influencing the contact metal selection. The back mirror metal is often either evaporated or sputter-coated. If the metal point contact and the back mirror consist of the same metal, evaporating or sputtering the metal would be preferred over electroplating, so that both the metal point contacts, and the back mirror are deposited simultaneously

We tried both electroplated Ni/Au and Au metal contacts in the via for electrical conduction. Both Ni/Au and Au contacts to a 4×10^{19} cm^{-3}, C-doped p-AlGaAs BCL, measured on a circular TLM pad [18] test structure, for full metal contact, showed a very low specific contact resistivity of 1×10^{-6} Ωcm^2. Similarly, the specific contact resistivity between a p-AlGaAs BCL and PDBC (reduced area metal contact) for electroplated Ni/Au point contact and e-beam evaporated 1 nm Ti/150 nm Au circular TLM test structure was measured to be 2.2×10^{-6} Ωcm^2. In the latter case, 1 nm Ti/150 nm Au mimics the back mirror that is discussed in the subsequent paragraph.

For the back mirror fabrication, we initially tried 200 nm e-beam evaporated Au and found that the adhesion between the dielectric and Au was insufficient. In this case, the devices either cracked or detached from the substrate, either during the substrate removal process or the mesa isolation process. Even sputtered Au did not offer satisfactory adhesion to the dielectric. Instead, a layer of 1 nm thick Ti for SU-8 and a layer of 2.5 nm Ti for SiO_2 was e-beam evaporated between the dielectric and the mirror metal, which gave satisfactory adhesion. These Ti layers are thin enough and transparent enough to incoming light for the dielectric-metal mirror to still be highly reflective. Thus, the blanket metal for the back mirror consisted in these experiments of a 1 to 2.5 nm Ti adhesion layer, depending on the dielectric used, followed by 200 nm of Au or Ag.

Summary

In this article, we have explored several methods for fabricating patterned dielectric back contact (PDBC) mirrors for improved rear reflectance, while enabling low-resistance electrical transport. The methods differ in the deposition method of the dielectric spacer, the dielectric material, the order of patterning and deposition steps, and in the ability to remove the parasitically absorbing back contact layer. SU-8 is a spin-on photosensitive dielectric with controllable thickness that can be left permanently in the device, although attaining a smooth film and removing the back contact layer present some processing challenges. Evaporated dielectrics allow for a wider range of materials and refractive indices, though the overall fabrication has more process steps. These PDBC processing methods apply in whole or in part to any semiconductor optoelectronic device that benefits from a highly reflective and conductive contact surface.

Data availability

No data was used for the research described in the article.

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