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# **Contacting individual graphene nanoribbons using carbon nanotube electrodes**

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### **CONTENTS**



#### <span id="page-2-0"></span>1. MATERIALS,CHARACTERIZATION AND DEVICE FABRICATION



#### <span id="page-2-1"></span>1.1. SWNT array, GNR array and their characterization

Figure 1. Charaterization of aligned SWNT array, aligned 9-AGNR array, and their transfers. (a) Raman map characterization of large-area uniaxially aligned SWNT arrays on  $\rm SiO_2$  substrate transferred from quartz crystal. (b) SEM characterization of the aligned SWNT arrays. The average separation distance of the SWNTs is  $\sim 10$  µm. (c) Raman characterization of the transferred individual SWNTs on  $SiO<sub>2</sub>$  substrate. The SWNTs used in this work have diameters of  $D = 1.5 \pm 0.2$  nm, as ditermined by the RBM peak statistics [\[1\]](#page-17-1). (d) Scanning tunneling micrograph (STM) of the 9-AGNRs on the Au (788) growth substrate, before transfer to the device substrate.The average GNR density is about 3 GNRs per terrace, with an average separation distance of 1.1 nm and an average length of 40-45 nm. (e) Typical Raman spectrum for 9-AGNRs on Pd substrate. The presence of the characteristic peaks (CH and RBLM) reveals the integrity of the 9-AGNRs upon annealing on the device substrate. (f) Polarization dependence of the G- and RBLM-peak intensity reveals almost perfect alignment with the source-drain axis. (g) Optical micrograph of a sample (global BG devices) with patterned SWNT electrode array and transferred GNRs/PMMA film. The GNR array is in parallel with the SWNT electrode array. (h) SEM characterization of a pair of representative SWNT electrodes with a gap size of  $\sim 22$  nm.

#### <span id="page-3-0"></span>1.2. Process flow of multi-gate device fabrication



<span id="page-3-1"></span>Figure 2. Schematic illustration of the process flow to fabricate multi-gate SWNT-GNR junction devices. (i-iii) On-surface synthesis of aligned 9-AGNRs and transfer to device substrate. (I-III) CVD synthesis of aligned SWNT arrays and transfer to device substrate. (a-g) Multi-gate substrate preparation and SWNT-GNR junction fabrication.

Figure [2](#page-3-1) shows the detailed process flow for the multi-gate device fabrication. First of all, we use a cleaned silicon/silicon dioxide (285 nm) with predefined alignment markers as substrate (a). Gate electrode arrays with 3 electrodes (FG, SG1 and SG2 in Fig. S2a-b) per device (3 nm Cr / 15 nm Pt) are fabricated on the substrate using standard electron-beam lithography (EBL), electron-beam evaporation (EBE) and followed by a lift-off process, as shown in (b). The substrate with metal gate electrodes is then deposited an  $Al_2O_3$  dielectric layer (30 nm) using atomic layer deposition (ALD) serving as a gate oxide (c). After that we spin-coated a 160 nm thick PMMA 950K (AR-P 672.02, Allresist GmbH) layer on the  $\rm Al_2O_3$  and used EBL to define an etch mask. A wet etching step of 30 minutes at room temperature using MF321 (DOW Chemical) opened the oxide on top of the gate for probing. The PMMA-based etch mask is removed using acetone and isopropanol followed by  $N_2$  blowdry. (I-III) show the growth of aligned SWNT arrays and transfer processes. Highly aligned SWNT arrays are grown on quartz wafers with relatively low coverage of Iron catalysts in a chemical vapor deposition (CVD) system. After growth, low-density (∼ 1 SWNTs per 10 µm) horizontally aligned SWNT arrays are synthesized (I). Transfer of the SWNT arrays

is carried out by using a "wet" process. A 400 nm PMMA film is spincoated onto the asgrown SWNT arrays on quartz, and then the chip is immersed in an aqueous KON solution to etch the quartz. After releasing, the PMMA film with SWNT arrays is transferred on  $\text{Al}_2\text{O}_3$  covered substrate (d). After the SWNT transfer, arrays of Cr/Pd (5 nm/60 nm) electrodes are fabricated for contacting SWNTs using standard EBL, EBE and followed by a lift-off process (e). The channel length is 2.5 µm while the channel width is designed as 10 µm for the purpose of contacting no more than 1 SWNT for each device. Afterward, a 60 nm thick CSAR resist (AR-P 6200.04, Allresist GmbH) is spin-coated, and followed by the electron beam exposure. Then the resist is developed using a suitable developer (AR 600- 546, Allresist GmbH) at room temperature for 1 min followed by an IPA rinse. After reactive ion etching (15 sccm Ar, 30 sccm  $O_2$ , 25 W, 18 mTorr) for 12 s to define nanogaps (15-25 nm) at SWNTs, the etching mask is removed by immersing in 1-Methyl-2-pyrrolidinone (NMP) (Sigma Aldrich) for 60 min at 80 °C, and rinsed with IPA, and blown dry with  $N_2$ . This approach yields clean and well-separated SWNT electrodes (f). Finally, uniaxially aligned 9-AGNRs are synthesized on Au(788) single crystal (GNRs grown along the narrow Au(788) terraces) and transferred from their growth substrate to the silicon-based substrates with predefined SWNT electrodes by an electrochemical delamination method using PMMA as described previously[\[2–](#page-17-2)[4\]](#page-17-3).

#### <span id="page-5-0"></span>1.3. Room-temperature electrical characterizations of devices



Figure 3. Room-temperature electrical characterizations of devices for pristine SWNT, after gap formation, and after 9-AGNR transfer. (a) IV for pristine SWNT (black curve), after gap formation (red curve), and after GNR transfer (green curve). The IV curves are acquired at zero gate voltage for all gates. (b) Current as a function of  $V_{FG}$  for pristine SWNT (black curve), after gap formation (red curve), and after GNR transfer (green curve) measured on a typical device with M-SWNT leads. After GNR transfer, the current show gate dependence because of the GNRs bridged in the channel and the surrounding GNR film. (c) Current as a function of  $V_{FG}$  for pristine SWNT (black curve), after gap formation (red curve), and after GNR transfer (green curve) measured on a typical device with S-SWNT leads.

#### <span id="page-6-0"></span>2. ELECTRON TRANSPORT IN GLOBAL BACK-GATE DEVICES



<span id="page-6-1"></span>Figure 4. Low-temperature transport measurements for D1 with global BG architecture. Colour scale differential conductance versus  $V_{BG}$  and  $V_{Bias}$  for a 9-AGNR device (D1) with S-SWNT leads.

For the first stage, GNR devices with global back-gate  $(285 \text{ nm } \text{SiO}_2)$  architectures were fabricated. In Fig. [4,](#page-6-1) the measurements for one 9-AGNR device (D1) with S-SWNTs as electrodes are shown. All measurements for global BG devices are performed in a cryogenic probe station with a base temperature of 9 K. Fig. [4](#page-6-1) shows the plot of differential conductance versus V<sub>Bias</sub> and global back-gate voltage (V<sub>BG</sub>) of D1. In the V<sub>BG</sub> range of -100 V  $\sim$  -40 V, a few Coulomb diamonds with crossing points and sometimes "overlapping" features (e.g., at  $\sim$  -90 V) are observed indicating the transport through a single 9-AGNR. When V<sub>BG</sub> >-40 V, the conductance is pinched off due to the bandgap of S-SWNTs or 9-AGNRs. Here we realized that with a global BG architecture the chemical potential of GNRs and SWNT electrodes are tuned simultaneously by the common BG, then it is hard to distinguish the transport features between GNRs and SWNT electrodes via the bias spectroscopy.

## <span id="page-7-0"></span>3. ADDITIONAL DATA FOR ELECTRON TRANSPORT IN MULTI-GATE DE-VICES



<span id="page-7-1"></span>3.1. D3: stability diagram recorded at  $V_{SG1} = V_{SG2} = 0$  V

Figure 5. Low-temperature transport measurements for multi-gate 9-AGNR devices (D3) with M-SWNT leads.dI/dV as a function of  $V_{FG}$  and  $V_{Bias}$  (stability diagram) for fixed side gate voltages of  $V<sub>SG1</sub> = V<sub>SG2</sub> = 0 V$ .

<span id="page-8-0"></span>3.2. Low-temperature transport measurements for D4 and D5 with M-SWNT leads



Figure 6. Low-temperature transport measurements for multi-gate 9-AGNR devices (D4 and D5) with M-SWNT leads. (a) Colour scale differential conductance versus  $V_{FG}$  and  $V_{Bias}$  for D4 with M-SWNT leads. The  $V_{SG1}$  and  $V_{SG2}$  are both fixed at 0 V. (b) Colour scale differential conductance versus  $V_{FG}$  and  $V_{Bias}$  for D5 with M-SWNT leads. The  $V_{SG1}$  and  $V_{SG2}$ are both fixed at 0 V. White arrows highlight the resonances originating from the modulation of DOS of M-SWNT leads.

In the given  $V_{FG}$  ranges,  $(-8 V, 8 V)$  for D4 and  $(-6 V, 6 V)$  for D5, multiple Coulomb diamonds are observed. However, these diamonds are irregular, aperiodic, and sometimes "overlapping" with addition energies varying between 50 meV and 100 meV for D4, and between 100 meV and 200 meV for D5. The diamond features most likely originate from GNR QD with localized states formed at the GNRs due to local confinement potentials. For D5, in the  $\mathrm{V_{FG}}$  range of 2 V to 6 V, several diagonal resonances at both the positive and negative  $\mathrm{V_{Bias}}$  are observed. These resonances are attributed to the SWNT lead states that have a much smaller coupling to the FG than that of the GNR QD.

<span id="page-10-0"></span>

Figure 7. Additional Franck-Condon analysis for D6. Differential conductance traces measured at fixed  $V_{FG}$ : (a) 1.20 V, (b) 3.08 V, (c) 2.04 V and (d) 3.76 V. The black solid lines are fits to (dI/dV)max using the Franck-Condon progression described in the main text. The average value of  $\lambda$  is 2.66  $\pm$  0.09.

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Figure 8. Additional QD analysis for D6. Map of the charge stability diagram in the (a)  $V_{FG}-V_{SG2}$  plane and (b)  $V_{FG}-V_{SG1}$  plane at  $V_{Bias}=100$  mV, showing diagonal resonance features. To determine the position of the QD along the SWNT-GNR-SWNT channel, we have analyzed the respective gate coupling of the SG1, FG, and SG2 for device D6. Here shows conductance measurements as a function of the  $V_{FG}$  and  $V_{SG2}$  (left), and as a function of the  $V_{FG}$  and  $V_{SG1}$ (right) at  $V_{\text{Bias}} = 100 \text{ mV}$ . From the change in the resonance position, we extract the following relative gate couplings  $\alpha_{\text{FG}}$ :  $\alpha_{\text{SG1}}$ :  $\alpha_{\text{SG2}} = 1$ : 0.81: 0.29. Based on these and position of the gates with respect to the SWNT-GNR-SWNT channel, we conclude that the QD is formed in the GNR, rather than the in SWNT leads.

#### <span id="page-12-0"></span>3.5. Tunnel coupling fitting



Figure 9. Coupling fitting using Breit-Wigner model. Fitting of a Coulomb peak at zero bias for one representative crossing point. The  $dI/dV$  data (blue points) are extracted from the differential conductance maps. The solid orange curve represents a fit to the Breit-Wigner (BW) model for resonant transport through a single-lifetime-broadened transport level.[\[5\]](#page-17-4). From the fitting, a coupling  $\Gamma$  of 4.9 meV is extracted. To exclude that the resonances are purely temperature-broadened, we fit our data to thermally broadened resonances (solid purple curve).[\[5\]](#page-17-4) We find that the equivalent temperature is around ∼46 K, which is significantly higher than the cryostat temperature (255 mK). This indicates that the broadening of the resonances observed in our measurement is the result of the combined effect of hybridization with the electrode and temperature.

In the Breit-Wigner model, the peak shape is described by:[\[5\]](#page-17-4)

$$
G(\Delta V_G) = \frac{e^2}{h} \frac{\Gamma_1 \Gamma_2}{(\Delta E^2 + \frac{\Gamma^2}{4})},\tag{1}
$$

with  $\Gamma = \Gamma_1 + \Gamma_2$  and the QD level detuning:

$$
\Delta E = -e\alpha(\Delta V_G - V_G^{(0)}),\tag{2}
$$

where  $V_G^{(0)}$  is the position of the resonance. Here,  $\alpha$  is the gate coupling of the backgate to the QD, described using the following relation:

$$
\alpha = \frac{\Delta V_{Bias}}{\Delta V_G}.\tag{3}
$$

The conductance of a thermally-broadened level is described as follows:[\[5\]](#page-17-4)

$$
G = \frac{e^2}{h} \frac{1}{4K_B T} \frac{\Gamma_1 \Gamma_2}{\Gamma} \cosh^{-2}(\frac{\Delta E}{2k_B T}),\tag{4}
$$

with  $k_B$  being the Boltzmann constant and  $T$ , the bath temperature.

#### <span id="page-14-0"></span>3.6. Low-temperature transport measurements for D8 with S-SWNT leads



Figure 10. Colour scale differential conductance versus  $V_{FG}$  and  $V_{Bias}$  at fixed  $V_{SG1}=V_{SG2}= 0$  V for a 9-AGNR device (D8) with S-SWNT leads. Several diamond-like features in the vertical direction are observed. Edges of one representative diamond are marked by white lines. We attribute these diamonds to the modulation of the discrete energy levels of GNR QD. In addition, several horizontal resonance lines in both positive and negative bias regimes are observed, as highlighted by grey arrows. We attribute these horizontal resonances to the modulation of the DOS of S-SWNT leads. One universal small bias gap is present in this device.

#### <span id="page-15-0"></span>4. TRANSMISSION THROUGH 9-AGNRS WITH SWNT ELECTRODES



Figure 11. Transmission through 9-AGNRs with SWNT electrodes. (a) Structures of 9-AGNRs with SWNT electrodes. Three GNRs 1-3 with different lengths are illustrated. (b) Transmission curves of the junctions shown in a with varying GNR lengths.

<span id="page-16-0"></span>

<span id="page-16-1"></span>Figure 12. Double QDs in series. (a) Schematic model of the double QDs with two capacitively coupled gates (FG and SG1). (b-d) Current maps as a function of FG voltage and SG1 voltage (charge stability diagram) in the double QD regime at  $V_{SG2}=-4$  V. (b) Overview map recorded at a negative bias of  $V_{Bias}$ =-250 mV. (c) High-resolution measurement recorded at negative bias  $V_{Bias} = -250$  mV. (d) High-resolution measurement recorded at positive bias  $V_{Bias} = 250$  mV.

A double quantum dot is formed in the nanojunction when two physical GNRs are connected in serial within the junction (as illustrated in Fig. [12a](#page-16-1)). Fig. [12b](#page-16-1)-d present several maps of the current as a function of the voltages on FG ( $V_{FG}$ ) and SG1 ( $V_{SG1}$ ). In Fig. [12b](#page-16-1)), an overview map is shown recorded at a negative bias voltage of  $V_{Bias} = -250$  mV and  $V_{SG2} = -250$ 4V. The map shows a honeycomb-like pattern, characteristic for charge stability diagrams of double QD systems. Here, the two gates FG and SG1 control the number of charges on dot 1 and 2, respectively. At low-bias, the corners of the honeycomb correspond to the triple points at which the energy level of the left dot aligns with the energy level of the right dots. As such, transport through the two QDs is allowed. As in our measurements the bias voltage is high, these triple points are expected to become triangular. Fig. [12c](#page-16-1) zooms in on a particular region of large current, highlighting the triangular shape of the triple points. This shape is characteristic for double QD systems. We note that as the bias voltage is large, some of the current triangles overlap with adjacent ones. Fig. [12d](#page-16-1) shows a representative triangle measured at a large positive bias of  $V_{Bias}$  = +250 mV. The bias triangles change direction upon a reversal of the bias voltage, a key feature for double QD systems. Altogether, our measurement are in line with the formation of a double QD system being formed on our junction, the presence of which is verified using a multi-gate measurement scheme.

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