Supplementary Information: Electrochemical etching strategy for shaping monolithic 3D structures from 4H-SiC wafers

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Implantation:

- A 50 nm Al scattering layer is deposited before implantation.
- The simulated implantation profile computed with TRIM [1] software is shown in **Figure S1**. The dark grey shaded area represents the Al scattering layer (the SiC surface is at the depth of 0 nm); a detailed collection of the implantation profiles used for our experiment is given in [2] together with a script to reproduce **Figure S1** as well as **Figure 2** of the main manuscript.
- The sample is kept at room temperature during the implantation. The implantation is conducted with our two in-house ion implanters covering energy ranges from 10 keV up to 2 MeV.
- The ion source was a hot cathode source for Nitrogen and a sputter source for Aluminum.



Figure S1: TRIM implantation profile. Grey area indicates the 50 nm Al scattering layer. Aluminium (Al) is used for p-doping. A counter-implantation of Nitrogen (N) is conducted to re-establish a top n-type SiC layer. The solid black line represents the effective p-type doping concentration, i.e. the sum of all Al implantation profiles minus the sum of the N counter-implantation profiles.

Post-implantation annealing:

• A post-implantation annealing for 30 minutes at 1700°C (900 mbar Ar) with a carbon-cap (C-cap) is needed in order to reduce implantation damage and activate the dopants [3, 4].

Electrochemical etching:

- A 1M KOH (1 mol/liter) solution is used.
- Electrochemical etching is conducted at room temperature without stirring.
- The sample is etched at an applied voltage of 1.65 V for 22 h resulting in an undercut of 31 μ m (etch rate = 1.4 μ m/h). The sample contains more than 50 different cantilever structures.
- In **Figure S2**, the time evolution of the etching current and the reference voltage are displayed, see also [2] for details.



Figure S2: Electrochemical etching characteristics for the fabrication of free-standing cantilevers. Current and reference voltage over time.; etching duration of 22 h at 1.65 V.

High-temperature annealing experiments:

- Annealing is performed in a vertical cold-wall reactor comprising a double-walled, water-cooled quartz tube and a graphite susceptor in Ar flow. No bake out in vacuum was performed. The sample was annealed under 900 mbar Ar atmosphere for 30 minutes and subsequently cooled down for 1 h.
- Graphene growth takes place via sublimation of Si from the surface (SiC(s) → Si(g) + C(s)), with C atoms diffusion and nucleation into graphene islands [5, 6]. As Si and C atoms are bonded more weakly on the step edges, Si desorption and graphene growth is faster on the step edges as on the terraces. Different decomposition velocities of terraces in 4H-SiC result in step bunching, at temperatures above 1200°C [6]. Here we utilize a Silicon Carbide container as supply of a background pressure of silicon vapor to prevent further loss of Si from the sample (often referred to as "sublimation sandwich" technique), resulting in higher quality graphene growth [5].

Porous p-SiC removal:

- After electrochemical etching, an undesired porous p-type structure often remains (goat beard), see Figure S3 (a) and (b).
- Using a homogenous Ni hard mask as etch mask (50 nm homogeneously sputtered on the whole sample), this porous p-SiC can be removed by an isotropic dry etch in a RIE: 190 mTorr, $CF_4 = 20.4$ sccm, $N_2 = 10.6$ sccm, $O_2 = 12.2$ sccm, 300 W.
- While the homogeneous Ni mask protects the top surface and the sidewalls, the thin porous p-SiC is successfully removed, see Figure S3 (c) and (b).



Figure S3: Porous p-SiC after ECE. (a) / (b) Cantilever directly after ECE with remaining porous p-SiC. (c) / (d) Cantilever after removal of porous p-SiC by isotropic dry etching (RIE, 190 mTorr, $CF_4 = 20.4 \text{ sccm}$, $N_2 = 10.6 \text{ sccm}$, $O_2 = 12.2 \text{ sccm}$, 300 W, using a Ni hard mask). Scale-bar of SEM micrographs: 5 μ m.

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