## **Supplementary Note**

## Ultra-low power electronic analog of a biological Fitzhugh-Nagumo neuron

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## S1. FN neuron model:



Figure S1: (a) Nullclines and trajectory of a FN neuron. (b) Typical oscillation waveforms of FN neuron.



Figure S2: FN neuron nullclines and trajectories for (a) different values of  $I_{ext}$  for r = 1 and (b) different values of r when  $I_{ext} = 0.5$ 

#### S2.1. Current scaling of tunnel diodes with physical diode area

This work uses the J-V and C-V curves reported by Yan et. al.<sup>1</sup> for the simulations (Figure S3a). The I-V curves are calculated by linearly scaling the J-V curve for a given physical diode area. Since the tunnel diodes fabricated and I-V curves reported by Yan et. al.<sup>1</sup> and another similar work<sup>2</sup> by the same research group have physical diode junction area exceeding  $25 \,\mu\text{m}^2$ , it is necessary to validate this linear scaling approach for nanoscale diodes. To the best of our knowledge, nanoscale diodes fabricated by a similar approach have not been reported. However, another work has reported silicon nanowire tunnel diodes with a diameter of 60 nm fabricated using a different approach<sup>3</sup>. The peak current densities (1.7-4  $\mu$ A/ $\mu$ m<sup>2</sup>) observed for these diodes are similar to those reported by Yan et. al.<sup>1</sup> for similar doping densities of the  $p^{++}$  (~10<sup>20</sup> cm<sup>-3</sup>) and  $n^{++}$  (~10<sup>20</sup> cm<sup>-3</sup>) regions. Figure S3b summarizes the peak current densities reported by different works for silicon homojunction tunnel diodes. These results show that a similar current density can be maintained for the nanoscale silicon tunnel diodes. In addition, Shao et. al.<sup>4</sup> have reported GaSb/InAs heterojunction nanowire tunnel diodes which exhibit an almost constant peak current density across a large range of diameters (between 9 nm and 1000 nm). These results therefore support our assumption of linear scaling behavior of current with area. It is also important to note that tunnel diodes operate in the forward bias and their capacitance directly results from the diffusion of carriers. Since diffusion capacitance is directly proportional to current, diode capacitance is also expected to scale linearly with physical diode area. In addition, Si/Ge nanowire tunnel diodes with a diameter of 20 nm have also been fabricated and reported by Fung et. al<sup>5</sup>. The



Figure S3: (a) Experimentally measured J-V and C-V curves of a silicon tunnel diode. (b) Peak current density of silicon homojunction and (c) GaSb/InAs heterojunction tunnel diodes of different diode area.

reported silicon homojunction nanowire tunnel diode and Si/Ge heterojunction nanowire tunnel diodes support our claim that it is possible to fabricate silicon based tunnel diodes at nanoscale.

## S2.2. Signal to noise ratio estimation

Signal to noise ratio (SNR) is of great importance for low power electronic devices. In the context of computing, we can compare the precision of computing between digital and analog systems by estimating an equivalent number of bits (ENOB),

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02}$$

The primary source of noise in oscillators is the thermal noise. For a signal bandwidth of  $\Delta f$ , thermal noise power is given by  $P_{thermal} = k_B T \Delta f$ . Power consumption in the oscillator is  $P_{osc} \approx 2I_{peak}V_{peak} = 2J_{peak}V_{peak}A$  where  $J_{peak}$  and  $V_{peak}$  are the current density and voltage of tunnel diode at the peak of NDR region and A is the area of the diode. Then the SNR is given in decibels by

$$SNR_{dB} = 10 \times \log_{10} \frac{P_{osc}}{P_{thermal}} = 10 \times \log_{10} \frac{2J_{peak}V_{peak}A}{k_{B}T\Delta f} = 10 \times \log_{10} 1.27 \times 10^{23} \frac{A(m^{2})}{\Delta f(Hz)}$$

Since FN neurons have a fundamental oscillation frequency of ~100 MHz, a bandwidth of 1 GHz is enough to maintain oscillations without any significant distortion of signal. For  $\Delta f = 1 GHz$  and  $A = 100 nm \times 100 nm = 10^{-14} m^2$ , we get an SNR of ~31.04 dB (ENOB = 4.86 bits). For  $A = 20 nm \times 20 nm = 4 \times 10^{-16} m^2$  which is the smallest tunnel diode that we have considered and have an estimated energy cost of 2 aJ/cycle, SNR is ~17 dB (ENOB = 2.53 bits).

#### **S3. Small signal model of Hara active inductors:**

Figure 2a show the small signal model of the Hara inductor. From the small signal model, we can construct the following equations:

$$(\frac{1}{R_G} + j\omega C_{gd})(V_{in} + V_{gs}) + j\omega C_{gs}V_{gs} = 0$$
$$(\frac{1}{R_G} + j\omega C_{gd})V_{in} + (\frac{1}{R_G} + j\omega C_{gd} + j\omega C_{gs})V_{gs} = 0$$

$$\begin{split} V_{gs} &= -\frac{\left(\frac{1}{R_G} + j\omega C_{gd}\right) V_{in}}{\frac{1}{R_G} + j\omega C_{gd} + j\omega C_{gs}} \\ I_{in} + g_m V_{gs} + j\omega C_{gs} V_{gs} - j\omega C_{ds} V_{in} = 0 \\ I_{in} + \left(-\left(g_m + j\omega C_{gs}\right) \frac{\left(\frac{1}{R_G} + j\omega C_{gd}\right)}{\frac{1}{R_G} + j\omega C_{gd} + j\omega C_{gs}} - j\omega C_{ds}\right) V_{in} = 0 \\ \frac{I_{in}}{V_{in}} &= \left(g_m + j\omega C_{gs}\right) \frac{\left(\frac{1}{R_G} + j\omega C_{gd}\right)}{\frac{1}{R_G} + j\omega C_{gd} + j\omega C_{gs}} + j\omega C_{ds} \\ &= \left(g_m + j\omega C_{gs}\right) \frac{1}{\frac{1}{R_G} + j\omega C_{gd}} + j\omega C_{ds} \\ &= \frac{g_m}{1 + \frac{j\omega C_{gs}}{\left(\frac{1}{R_G} + j\omega C_{gd}\right)}} + \frac{j\omega C_{ds}}{1 + \frac{j\omega C_{gs}}{\left(\frac{1}{R_G} + j\omega C_{gd}\right)}} + j\omega C_{ds} \\ &= \frac{1}{\frac{1}{g_m} + \frac{j\omega R_G C_{gs}}{g_m \left(1 + j\omega R_G C_{gd}\right)}} + \frac{1}{j\omega C_{gs}} + \frac{1}{\left(\frac{1}{R_G} + j\omega C_{gd}\right)} + j\omega C_{ds} \end{split}$$

When  $C_{gs} >> C_{gd}$ , this equation can be simplified to

$$\frac{I_{in}}{V_{in}} = \frac{1}{\frac{1}{g_m} + \frac{j\omega R_G C_{gs}}{g_m}} + \frac{1}{\frac{1}{j\omega C_{gs}} + R_G} + j\omega C_{ds}$$

These equations can be visualized as an equivalent circuit shown in figure 2b where  $L_{eq} = \frac{R_G C_{gs}}{g_m}$ .

## S4. Numerical model of FN neuron with Hara active inductor

The dynamic variables that need to be updated at every time step are  $i_C$ ,  $i_{NDR}$ ,  $i_g$ ,  $i_{ds}$ ,  $i_{gd}$ ,  $i_{gs}$ ,  $V_g$ ,  $V_s$ . The following pseudo-code can be used to update their values.

Start of time step (j + 1)

$$\frac{dV_s}{dt} = -\frac{i_C(j)}{C_{ds}}$$

$$\frac{dV_g}{dt} = \frac{1}{(C_{gs} + C_{gd})} \left( C_{gs} \frac{dV_s}{dt} - i_g(j+1) \right)$$

$$V_s(j+1) = V_s(j) + \frac{dV_s}{dt} \Delta t$$

$$V_g(j+1) = V_g(j) + \frac{dV_g}{dt} \Delta t$$

$$i_g(j+1) = \frac{V_g(j+1) - V_G}{R_G}$$

$$i_{ds}(j+1) = F(V_g(j+1), V_d = 0, V_s(j+1))$$

$$i_{NDR}(j+1) = G(V_s(j+1), V_{applied})$$

$$i_{gd}(j+1) = C_p \left( \frac{i_{NDR}(j+1) + i_{ds}(j+1)}{C + C_{ds}} - \frac{i_g(j+1)}{C_{gs}} \right)$$

$$i_C(j+1) = -(i_{NDR}(j+1) + i_{ds}(j+1)) + i_{gd}(j+1)$$

# End of time step (j + 1)

Here,  $C_p$  is the series equivalent capacitance of  $C_{gd}$ ,  $C_{gs}$ , and  $C_{ds} + C$ . Voltage across all capacitors are set to 0V at the beginning of simulation. All the currents are set to 0A at the beginning of simulation. F and G are the nonlinear functions describing the drain current of the MOSFET and the current through the tunnel diode.



## S5. Insensitivity of oscillation behavior on MOSFET size

Figure S4: Oscillation (a) frequency, (b) amplitude, (c) power consumption and (d) energy consumption for different NMOS area for a tunnel diode area of  $0.02 \ \mu m^2$ ,  $R_G = 110 \ M\Omega$ ,  $V_{applied} = 0.39 \ V$ .

The NMOS typically operates at the subthreshold regime in an FN neuron. The drain to source capacitance is the parasitic junction capacitance at the drain and source terminals due to formation of a depletion region. This capacitance per unit area is given by

$$C_{ds} = \frac{\epsilon_{Si}}{x_{dep}}$$

Here,  $\epsilon_{Si}$  is the permittivity of silicon and  $x_{dep}$  is the width of the depletion region. At the subthreshold regime,  $x_{dep}$  is approximately given by,

$$x_{dep} = \sqrt{\frac{2\epsilon_{Si}V_{FB}}{qN_A}}$$

Here,  $V_{FB}$  is the flatband potential at the junction, q is the charge of an electron and  $N_A$  is the acceptor doping concentration at the NMOS channel. Then the drain to source capacitance becomes,

$$C_{ds} = \frac{\epsilon_{Si}}{\sqrt{\frac{2\epsilon_{Si}V_{FB}}{qN_A}}} = \sqrt{\frac{q\epsilon_{Si}N_A}{2V_{FB}}}$$

For a typical NMOS,  $N_A \approx 10^{15} cm^{-3}$ ,  $V_{FB} \approx 0.2V$  and therefore  $C_{ds} \approx 0.2 fF/\mu m^2$  whereas parasitic capacitance of tunnel diode is  $C_{diode} \approx 20 \frac{fF}{\mu m^2} \gg C_{ds}$ . We have then simulated the oscillation behavior for a tunnel diode with area of  $0.02 \ \mu m^2$ ,  $R_G = 110 \ M\Omega$ ,  $V_{applied} = 0.39 V$  as we varied both NMOS area and the gate voltage V<sub>G</sub>. It is worth noting that the NMOS model is kept the same as the one for 65 nm process. For this simulation, when the NMOS area is smaller than that allowed by 65 nm process, we assumed that the model is still valid and the current and capacitances are linearly varied as a function of area. As shown in Figure S4, the only when NMOS area becomes large so that drain to source capacitance becomes comparable or larger than that of tunnel diode, the oscillation frequencies start decreasing. Otherwise, the same oscillation frequency, amplitude, power consumption and energy consumption can be maintained by decreasing the gate voltage V<sub>G</sub> with increasing NMOS area.

## S6. Unit oscillator circuit for Ising machine and max cut problems



Figure S5: (a) Simple 2-node max cut problem (b) Mapping 2-node max cut problem to FN neurons (c)  $P_{solution}$  as a function of  $R_{coupling}$  (d) Evolution of oscillation waveform towards correct solution

Applying KCL at node X of the circuit in supplementary Figure S6c,

$$C_{gs}\frac{d(V_1 - V_2)}{dt} = -\frac{V_1}{R_G}$$
$$R_G C_{gs}\frac{dV_1}{dt} + V_1 = R_G C_{gs}\frac{dV_2}{dt}$$

Applying KCL at node Y and assuming subthreshold operation for MOSFET ( $I_D = g_m V_{th}$ ),

$$C_{gs}\frac{d(V_2 - V_1)}{dt} + I_{NDR} + C_D\frac{dV_2}{dt} - g_m V_{th} = 0$$

$$C_{gs} \frac{d^{2}(V_{2} - V_{1})}{dt^{2}} + \frac{dI_{NDR}}{dV_{2}} \frac{dV_{2}}{dt} + C_{D} \frac{d^{2}V_{2}}{dt^{2}} = 0$$

$$C_{gs} \frac{d^{2}(V_{2} - V_{1})}{dt^{2}} + G \frac{dV_{2}}{dt} + C_{D} \frac{d^{2}V_{2}}{dt^{2}} = 0$$

$$\frac{1}{R_{G}} \frac{dV_{1}}{dt} + G \left(\frac{dV_{1}}{dt} + \frac{V_{1}}{R_{G}C_{gs}}\right) + C_{D} \left(\frac{d^{2}V_{1}}{dt^{2}} + \frac{1}{R_{G}C_{gs}} \frac{dV_{1}}{dt}\right) = 0$$

$$C_{D} \frac{d^{2}V_{1}}{dt^{2}} + \left(G + \frac{1}{R_{G}} + \frac{C_{D}}{R_{G}C_{gs}}\right) \frac{dV_{1}}{dt} + \left(\frac{G}{R_{G}C_{gs}}\right)V_{1} = 0$$

For  $G + \frac{C_D}{R_G C_{gs}} \gg \frac{1}{R_G}$ ,

$$C_D \frac{d^2 V_1}{dt^2} + \left(G + \frac{C_D}{R_G C_{gs}}\right) \frac{dV_1}{dt} + \left(\frac{G}{R_G C_{gs}}\right) V_1 = 0$$

Here, we have ignored  $V_G$  and  $V_{applied}$  under small signal assumptions. When there is any fluctuation in G and correlated fluctuation in  $C_D$ , the coefficient of each term scales by the same factor and the equation remains the same and therefore makes FN neuron immune to



Figure S6: (a) Symbol for oscillator circuit and the actual circuit (b) Mapping 8-node max cut problem on FN neurons (c) Circuit model of a FN neuron

fluctuations. However, large fluctuations in G and  $C_D$  could lead to situations where G +

 $\frac{C_D}{R_G C_{gs}} \approx \frac{1}{R_G}$  and such an immunity to fluctuations may not hold anymore.

## **References:**

(1) Yan, Y.; Zhao, J.; Liu, Q.; Zhao, W.; Seabaugh, A. Vertical tunnel diodes on high resistivity silicon. In *Conference Digest [Includes' Late News Papers' volume] Device Research Conference, 2004. 62nd DRC.*, 2004; IEEE: pp 27-28.

(2) Wang, J.; Wheeler, D.; Yan, Y.; Zhao, J.; Howard, S.; Seabaugh, A. Silicon tunnel diodes formed by proximity rapid thermal diffusion. In *Proceedings. IEEE Lester Eastman Conference on High Performance Devices*, 2002; IEEE: pp 393-401.

(3) Schmid, H.; Bessire, C.; Björk, M. T.; Schenk, A.; Riel, H. Silicon nanowire Esaki diodes. *Nano letters* **2012**, *12* (2), 699-703.

(4) Shao, Y.; Pala, M.; Esseni, D.; del Alamo, J. A. Scaling of GaSb/InAs vertical nanowire Esaki diodes down to sub-10-nm diameter. *IEEE transactions on electron devices* **2022**, *69* (4), 2188-2195.

(5) Fung, W. Y.; Chen, L.; Lu, W. Esaki tunnel diodes based on vertical Si-Ge nanowire heterojunctions. *Applied Physics Letters* **2011**, *99* (9).