Supplementary information

Cryogenic III-V and Nb electronics integrated on silicon for large-scale quantum computing platforms

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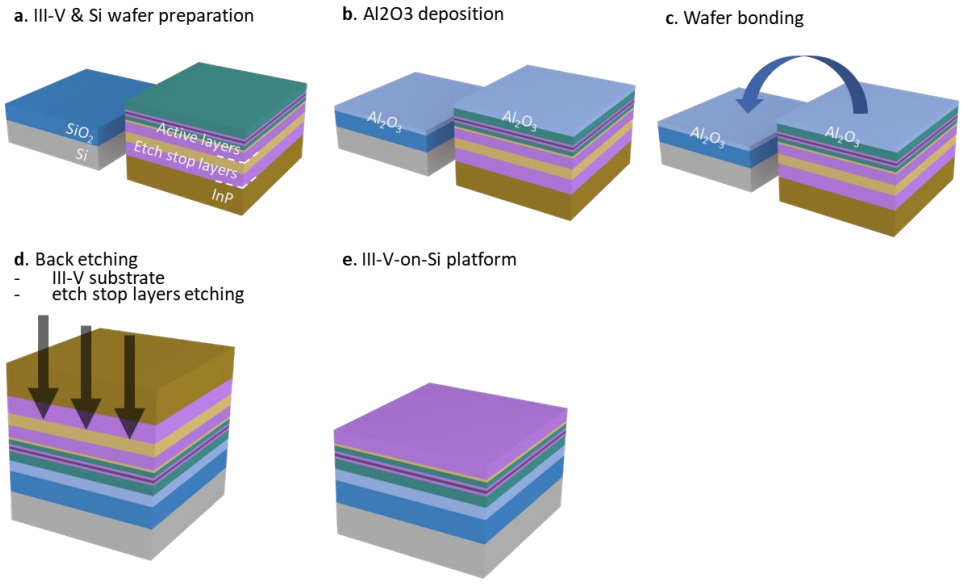
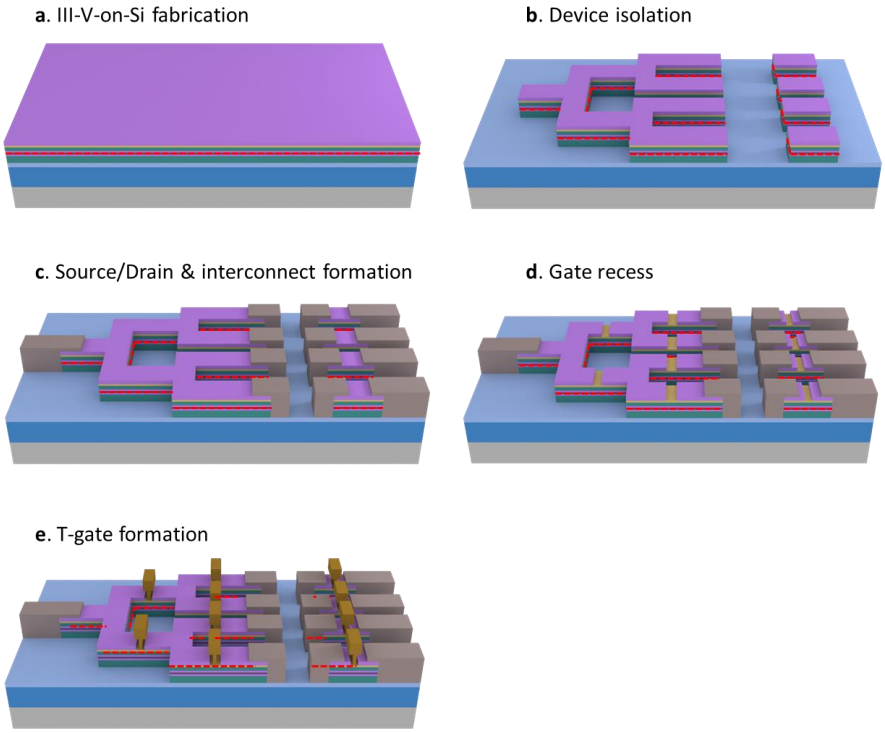
Supplementary Section 1. Fabrication process

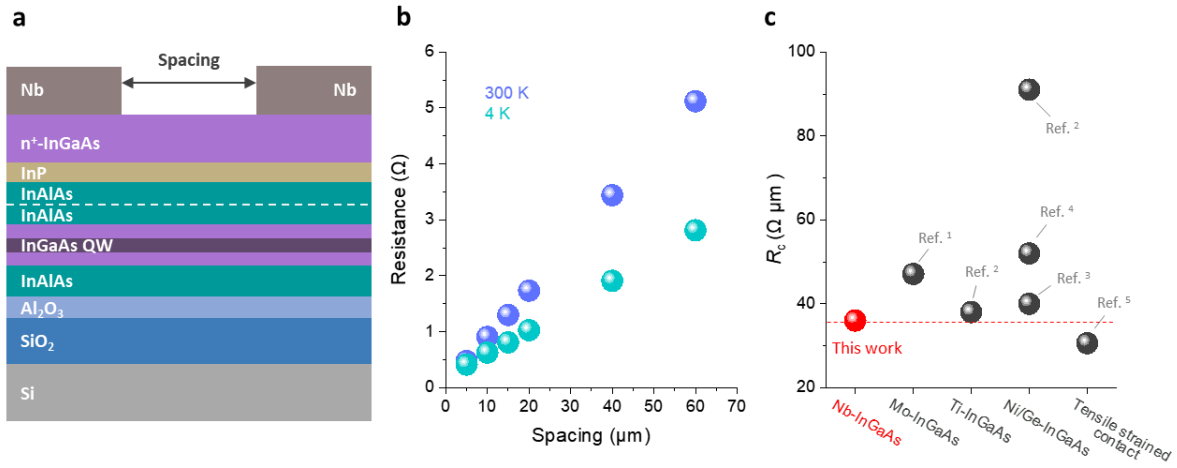


Supplementary Figure 1 | III-V-on-Si platform. a–**e**, Fabrication process flow of the III-V-on-Si platform using direct wafer bonding technique.



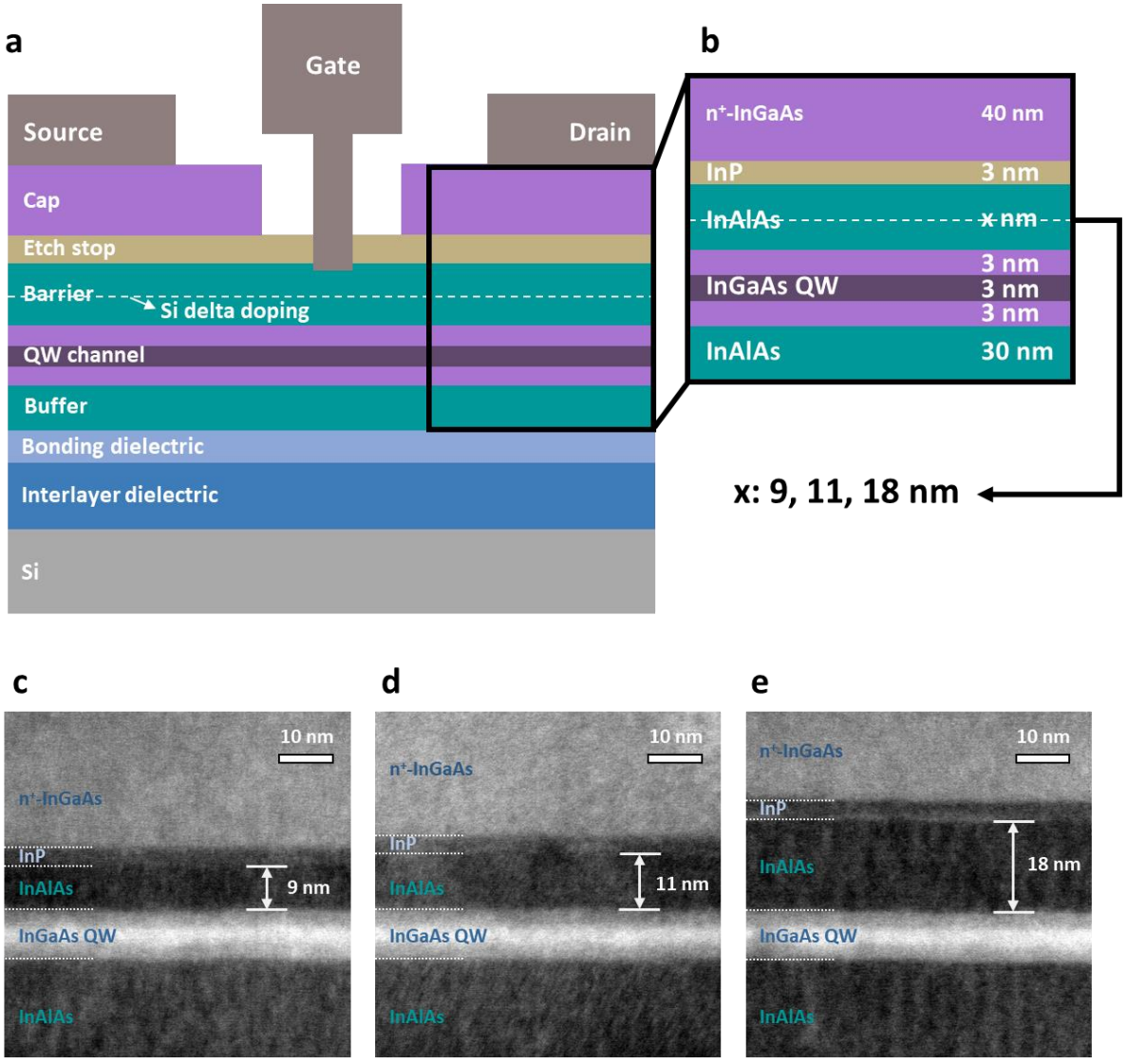
Supplementary Figure 2 | Cryogenic III-V and Nb electronics integrated on Si. a–**e**, Fabrication process flow of heterogeneous and monolithic 3D integrated III-V and Nb-based cryogenic RF transistors and routing circuits using III-V-on-Si platform.

Supplementary Section 2. Contact characterization of Nb/n$^+$-InGaAs



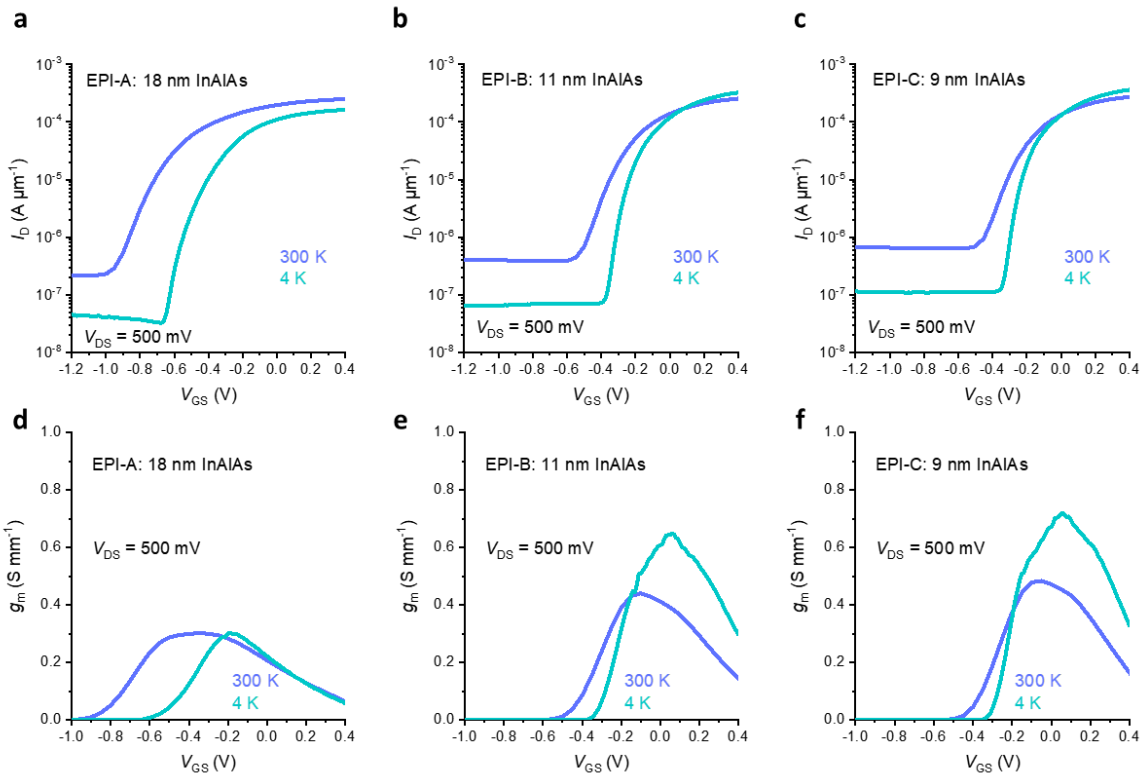
Supplementary Figure 3 | Characteristics of Nb/n$^+$-InGaAs contact. a, Schematic of the transfer length method (TLM) measurement configuration for Nb/n$^+$-InGaAs contact. **b**, TLM resistance as a function of spacing length of Nb/n$^+$-InGaAs contact at 300 K and 4 K. **c**, Benchmarking of contact resistance (R_c) at cryogenic temperature with previously reported values for n$^+$-InGaAs.

Supplementary Section 3. STEM analysis on III-V heterostructure



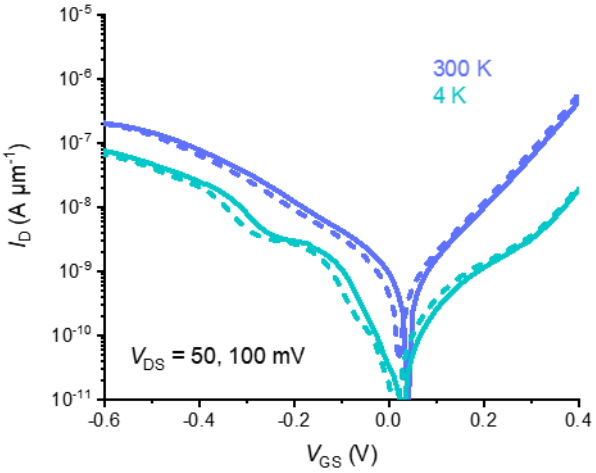
Supplementary Figure 4 | III-V heterostructure with different barrier thicknesses. a, Schematic of III-V and Nb-based HEMT integrated on Si. **b**, Zoomed structure of active III-V layers, featuring barrier thickness of 9, 11, and 18 nm. **c**,**d**,**e**, Scanning transmission electron microscopy (STEM) images of III-V heterostructures, each illustrating divergent InAlAs thickness: (c) 9, (d) 11, and (e) 18 nm. It was clearly confirmed that the epitaxial layers are uniformly grown with the target design thickness of each layer.

Supplementary Section 4. Device cryogenic characterization according to III-V heterostructure



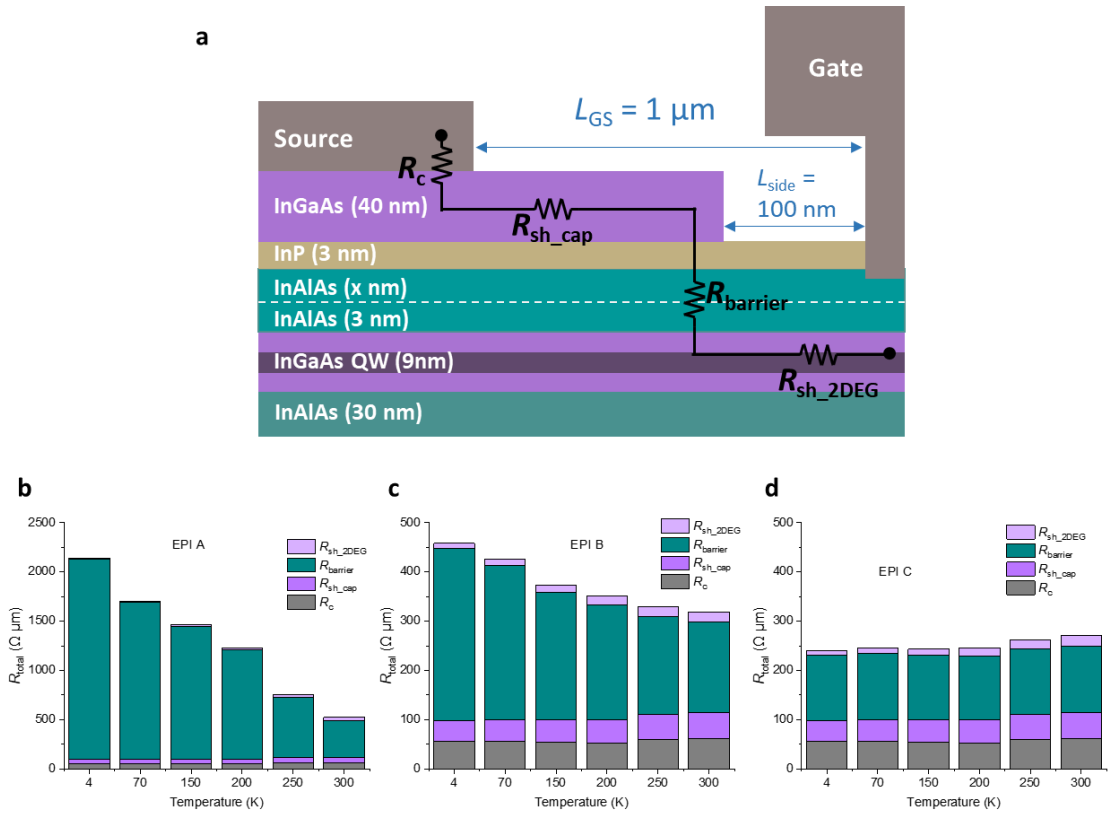
Supplementary Figure 5 | Cryogenic characteristics depending on the III-V heterostructure. a–c, Transfer characteristics of III-V HEMTs on Si with L_G = 2 μm and different barrier thicknesses of 9 nm (a), 11 nm (b), 18 nm (c) at 300 K and 4 K. **d–f**, Transconductance characteristics of III-V HEMTs on Si with L_G = 2 μm and different barrier thicknesses of 9 nm (d), 11 nm (e), 18 nm (f) at 300 K and 4 K.

Supplementary Section 5. Gate leakage characteristics of a short channel device



Supplementary Figure 6 | Gate leakage characteristics of the devices. Gate leakage current of III-V HEMTs on Si for the same device as in Figure 3a measured at V_{DS} of 50 (dashed) and 100 mV (solid). The measurements were conducted at 300 K and 4 K.

Supplementary Section 6. Analysis of parasitic resistance components according to temperature



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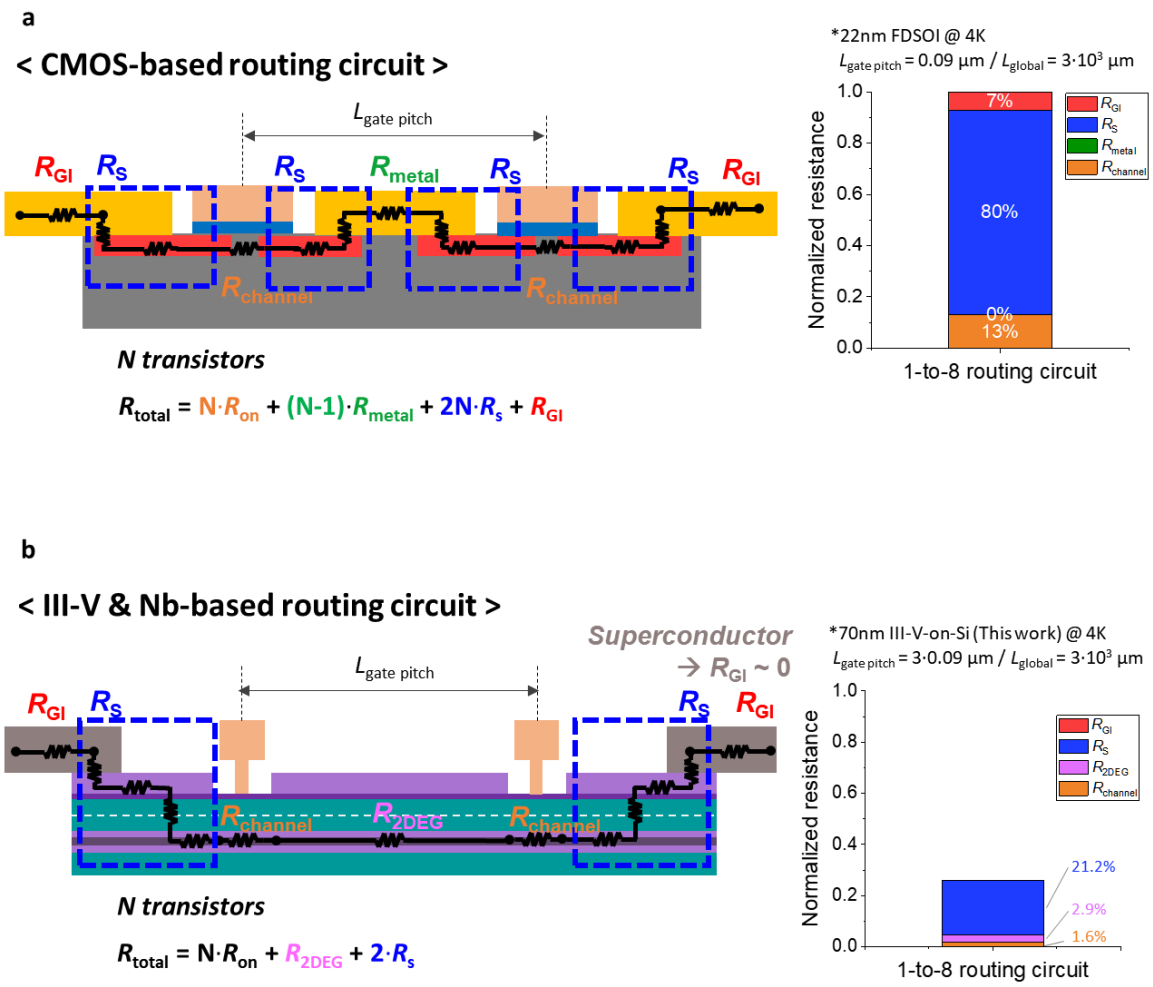
Supplementary Section 7. Structure and resistance analysis of routing circuits



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Supplementary References:

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