nature portfolio

Peer Review File

Cryogenic III-V and Nb electronics integrated on silicon for large-scale quantum computing platforms

Corresponding Author: Professor Sanghyeon Kim

This file contains all reviewer reports in order by version, followed by all author rebuttals in order by version.

Version 0:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors demonstrate III-V cryogenic transistors integrated on Si. The devices show excellent performance, in particular high-frequency metrics, and could be applied to quantum computing applications. A use case of signal routing using such devices is also demonstrated.

1. Why would the R2deg increase with thicker InAlAs? One would expect the opposite.

2. You write L.148 that the InAlAs does not significantly influence R2deg but your data shows almost 2x increase at 4 K, which sounds significant.

3. 35 mV/decade at 4 K is not exceptionally low, since other works have reported even <10 mV/decade. Could you provide a comment on this?
Do you see any dependence of SS on the InAlAs barrier thickness?

4. In Fig. 5 the ft versus NIF is benchmarked. However, the ft is given at VDS = 0.5 V and the NIF at 100 mV. It would be important to be clear about this in the text and caption.

5. In your previous work, gm is significantly higher, almost 2 S/mm at 4 K, while in this work the gm reported in supplementary material is lower, both at 0.5 V. However, ft/max are reporting similar values. What is the explanation for this?

6. Does RC change when Nb becomes superconducting? It seems not from supplementary data? But did you confirm the critical current density of the Nb superconductor?

Reviewer #2

(Remarks to the Author)
The manuscript by Jeong et al report on III-V and Nb-based cryogenic low-power electronics on a Si platform.

The major novelty is the successful demonstration of functional routing circuits based on InGaAs HEMTs and Nb superconducting metallization on Si using direct wafer bonding.
As a result, routing circuits and LNAs can be designed in the technology making it feasible for control and readout circuits at 4 K with high performance at low power dissipation. Together with CMOS at 4 K, the reported technology can be attractive for handling the large number of qubits predicted in the on-going upscaling of quantum process units. In my view, however, the full integration in a quantum system (or as the authors claim ”potentially solve the power consumption problem and pave the route towards a large-scale quantum computer”) will still be challenging because of the fragile qubit information including quantum-noise limited amplifiers, isolators, filters etc in the full readout chain.

The successful integration of Nb metallization in a HEMT process on Si is original and is definitively of interest. Routing circuits are demonstrated. However, the authors have missed some references:
Some of the results in the manuscript has previously been published by the authors at VLSI Symposium 2023. Some plots are fully or partly the same (Figs. 1d, 3e,3f, 4a,4b, suppl. Fig. 3b,3c)). The VLSI Symp. paper must be included in the

reference list of the current manuscript.

The integration of InGaAs HEMT circuits (MMICs) on silicon is not new. Please, refer to Leuther et al Proc. 50th European Microwave Conference 2021 , pp. 187.

The work claims ”state-of-the-art cryogenic performances” with respect to fT, fmax and ”noise indicator” sqr(Id)/gm. Also it is claimed rows 202-205: ” These results demonstrate that III-V HEMT on Si-based cryogenic RF transistors not only outperform CMOS-based cryogenic RF transistors but also provide the best performance when compared to conventional III-V-based cryogenic RF transistors.”

For reading out qubit signals, the ft, fmax and noise indicator are at best indicative of the gain and true noise performance in the microwave range 4-12 GHz crucial for qubit signal readout. Indeed, the noise indicator is not the minimum noise figure. The level of SS and DC curves at 4 K in Fig. 3 suggest that the gm/gds may not be sufficient for competing with the lowest noise HEMTs so far. Only cryogenic noise measurements can tell.

With regard to the HEMT LNA fort qubit readout, state of the art is amplification is typically 40 dB and average noise temperature of 1.4 K in the bandwidth of 4-8 GHz [Ref J. Li, IEEE EDL 43(7) 1029 2022]. This transforms to a minimum noise temperature of the HEMT slightly below 1.0 K at 6 GHz.

The Nb metallization approach in the manuscript is very interesting since it will provide very low loss at microwave frequencies. However, a drawback, not mentioned by the authors, is that this means a non-alloyed contact for the HEMT and the associated path to the 2DEG. As analyzed by the authors, this will give a high barrier resistance. In a traditional alloyed contact (not superconducting metallization), the barrier resistance does not normally present a problem at 4 K. In a HEMT LNA designed for qubit readout, the channel (gds) will in fact be the dominant noise source.

To be able to reproduce the experiment, details of the InP HEMT channel design must be given.

More comments:
Rows 63 and 64: ”To overcome this bottleneck, the idea of placing the control and readout electronics closer to the qubits was proposed as an intermediate solution”. Please, give reference.

Row 114: Language: a HEMT

Rows 125-128: “Through careful design of III-V heterostructure and the introduction of Nb superconductors suitable for III-V, high-performance cryogenic devices with high-frequency, low-noise, and low- power operation were achieved at 4 K, achieving a figure of merit that far exceeds the current state of the art.” Do you mean that you will describe this below? Please, consider to reformulate.

Row 135: “(several 10,000 cm2 V-1 s-1)”. Please, be more specific.

Row 150: 91 ohm/sq is relatively high Rsheet at 4 K. This may be due to the Nb metallization approach without alloying. Compare with Schleeh et al, IEEE EDL 33(5) 664 2012: Rsheet = 20 ohm/sq at 4 K .

Row 156: ” For non-optimized barrier thickness such as EPI-A, the..” Please, refer to definition of EPI-A in Fig. 2c.

Rows 164-166: ”However, over-scaling the barrier thickness can 164 cause high gate leakage and generate additional noise, so designing an appropriate barrier 165 thickness is very important, and the 9 nm barrier was used in this study.” This is true- however, the design of a low-noise HEMT for qubit readout can be made with a more aggressive aspect ratio (gate length to gate-to-channel distance). This is different compared to the design of a THz HEMT or an RF power HEMT. The control over the 2DEG is also dependent on your channel design where details now are left out, see comment above.

Rows 284-286: ”Second, our device not only surpasses CMOS performance but also demonstrates superior performance compared to previously reported III-V devices.” Please, provide references.

Fig 2e: On the x-axis, specify which thickness.

Supplementary Figure 5 caption: Transconductance: Replace (a), (b) ,(c) with (d), (e), (f)

Supplementary Figure 6: Please, specify the EPI, A, B or C

Supplementary row 134: Replace Figure 7 with Figure 8.

End review

Version 1:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
No further questions to the authors.

Reviewer #2

(Remarks to the Author)
The authors have made an extensive work in responding to all my comments and questions given in the orignal review.
I appreciate this work by the authors which now has increased the quality of the manuscript.

Aa a result, I recommend the Editor to accept this contribution to Nature Communications for publishing.

Title: Cryogenic III-V and Nb electronics integrated on silicon for large-scale quantum computing platforms

Authors: Jaeyong Jeong, Seong Kwang Kim, Yoon-Je Suh, Jisung Lee, Joonyoung Choi, Joon Pyo Kim, Bong Ho Kim, Juhyuk Park, Joonsup Shim, Nahyun Rheem, Chan Jik Lee, Younjung Jo, Dae-Myeong Geum, Seung-Young Park, Jongmin Kim and Sanghyeon Kim*

Manuscript ID: NCOMMS-24-44839-T

First of all, we would have really appreciated the valuable review and comments of the reviewer for our paper. According to the reviewer's comments, we have revised the paper carefully. The detailed one-to-one responses to the reviewers' comments are described in the following.

[Reviewer 1]

[Reviewer's comment]

Comments to the Author

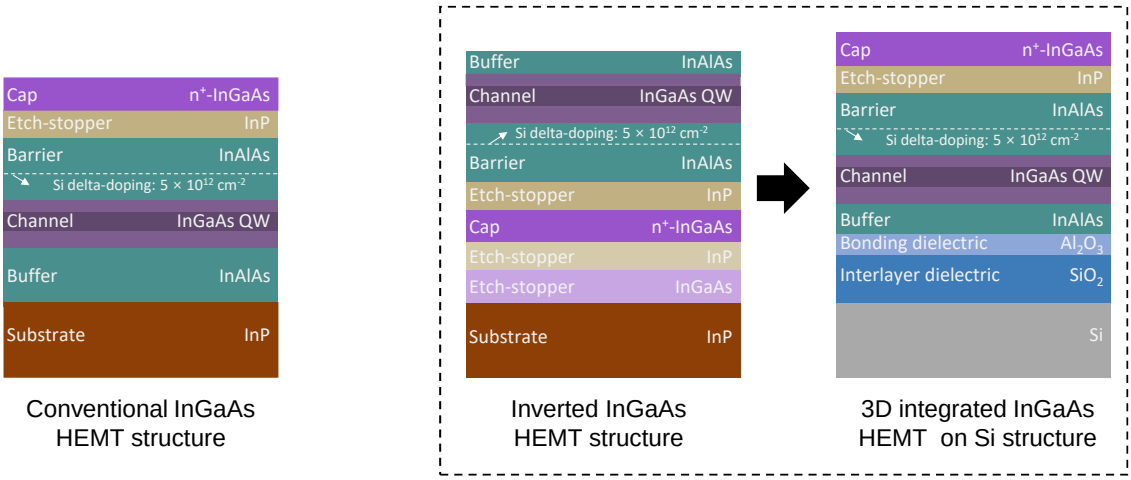
The authors demonstrate III-V cryogenic transistors integrated on Si. The devices show excellent performance, in particular high-frequency metrics, and could be applied to quantum computing applications. A use case of signal routing using such devices is also demonstrated.

[Comments 1]

1. Why would the R2deg increase with thicker InAlAs? One would expect the opposite.

[Reply 1]

As the reviewer noted, in conventional InGaAs HEMT structure, R_{2DEG} typically decreases as the InAlAs barrier thickness increases. However, our structure differs due to its 3D integration. Specifically, we used an inverted InGaAs HEMT structure with a bonding dielectric, enabling 3D integration of InGaAs HEMTs on a silicon substrate as shown below.



The difference between the conventional InGaAs HEMTs and 3D integrated InGaAs HEMTs would be the existence of the backside interface (Channel/buffer/oxide interface). In conventional InGaAs HEMT structure, R_{2DEG} is influenced by InAlAs(barrier)/InGaAs(channel) design, traps between the buffer and bottom of the channel, and surface states on top of the barrier. On the other hand, In 3D integrated InGaAs HEMT structure, the traps between the bonding dielectric and buffer introduce additional impact on R2DEG.

Conventional InGaAs HEMTs are reported with an R_{2DEG} around 20 ~ 90 Ω sq^{-1}, as referenced below.

- Schleeh, J. *et al.* Ultralow-power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz, *IEEE Electron Device Lett.* **33**, 664–666 (2012).
- Cha, E. *et al.* Cryogenic InGaAs HEMTs with Reduced On-Resistance using Strained Ohmic Contacts. In *International Electron Devices Meeting (IEDM)* 34.5.1–34.5.4 (IEEE, 2023).
- Alt, A. R. & Bolognesi, C. R. Temperature dependence of annealed and nonannealed HEMT ohmic contacts between 5 and 350 K. *IEEE Trans. Electron Devices* **60**, 787–792 (2013).
- Watanabe, I. *et al.* Thermal stability of Ti/Pt/Au ohmic contacts for cryogenically cooled InP-based HEMTs on (4 1 1)A-oriented substrates by MBE. J. Cryst. Growth 301–302, 1025–1029 (2007).
-

However, in our 3D integrated InGaAs HEMTs, the R_{2DEG} shows a slightly higher resistance range of 91 ~ 132 Ω sq^{-1}. We believe that this difference of 91 to 132 Ω sq^{-1} is mainly due to the difference in the backside interface condition. Therefore, it is very important to mitigate the impact of the backside interface in the future. Nevertheless, the main focus of this paper is on the effect of InAlAs thickness on the overall device resistance, and our analysis that the barrier resistance due to InAlAs thickness has dominantly affected the overall resistance is still valid. If the influence of the backside interface becomes eliminated in the future, the barrier resistance will become even more important.

To explain this, we added the following explanation.

Newly added part:

manuscript, line 155-158:

The sheet resistances of 2DEG (R_{2DEG}) in our 3D integrated InGaAs HEMTs range from 91 to 132 Ω sq^{-1} at 4 K, which is slightly higher than the R_{2DEG} for state-of-the-art conventional InGaAs HEMTs (20 to 90 Ω sq^{-1})[20,30,31,32], mainly due to backside interface, which requires further study to mitigate its impact in the future.

References:

[30] Schleeh, J. *et al.* Ultralow-power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz, *IEEE Electron Device Lett.* **33**, 664–666 (2012).

[31] Alt, A. R. & Bolognesi, C. R. Temperature dependence of annealed and nonannealed HEMT ohmic contacts between 5 and 350 K. *IEEE Trans. Electron Devices* **60**, 787–792 (2013).

[32] Watanabe, I. *et al.* Thermal stability of Ti/Pt/Au ohmic contacts for cryogenically cooled InP-based HEMTs on (4 1 1)A-oriented substrates by MBE. J. Cryst. Growth 301–302, 1025–1029 (2007).

[Comments 2]

2. You write L.148 that the InAlAs does not significantly influence R2deg but your data shows almost 2x increase at 4 K, which sounds significant.

[Reply 2]

As the reviewer noted, in our 3D integrated InGaAs HEMTs, the R_{2DEG} shows a slight difference between 91 to 132 Ω sq^{-1} for different InAlAs thicknesses. However, our statement that "the InAlAs does not significantly influence R_{2DEG}" is based on the data in Figure 2f, where the variation in $R_{barrier}$ with different InAlAs thicknesses is much more pronounced than the variation in R_{sh_2DEG} observed in Supplementary Figure 7. This indicates that the overall side resistance is more substantially affected by changes in $R_{barrier}$ than by R_{sh_2DEG} variations due to InAlAs thickness differences. However, as the reviewer pointed out, stating that "the InAlAs does not significantly influence R2DEG" could indeed be confusing to readers without additional context.

To eliminate this ambiguity and clarify our argument, we revised the following explanation to the manuscript to provide a more precise interpretation of our findings.

Revised part:

manuscript, line 167-169:

It should be noted that the thickness of the InAlAs barrier does not considerably influence the sheet resistance of 2DEG (Fig. 2d).

→ This demonstrates that the thickness of the InAlAs barrier has a dominant effect on $R_{barrier}$ and, consequently, plays a crucial role in determining the overall device resistance at cryogenic temperature.

[Comments 3]

3. 35 mV/decade at 4 K is not exceptionally low, since other works have reported even <10

mV/decade. Could you provide a comment on this? Do you see any dependence of SS on the InAlAs barrier thickness?

[Reply 3]

As the reviewer pointed out, the SS value of 35 mV/decade at 4K is not exceptionally low. SS is one of the very important parameters in cryogenic electronics. Accordingly, in our previous work, we analyzed the SS mechanism in cryogenic InGaAs HEMTs, as referenced below:

- Jeong, J. *et al.* Impact of the channel thickness fluctuation on the subthreshold swing of InGaAs HEMTs at cryogenic temperature down to 4 K for ultra low power LNAs. *IEEE International Electron Devices Meeting (IEDM)* T34-4 (2023).
- Jeong, J. *et al.* Influence of Channel Structure on the Subthreshold Swing of InGaAs HEMTs at Cryogenic Temperatures Down to 4 K. *IEEE Trans. Electron Devices* **71**, 3390–3395 (2024).

In our previous work, we found that the degree of disorder within the device impacting SS arises from potential fluctuations in the conductive channel, which are directly linked to the channel thickness fluctuations. We also discovered that the degree of potential fluctuation caused by these intrinsic variations in the channel is not constant; rather, it exhibits a distinct variation depending on the specific structure of the channel. Therefore, we believe that the SS of cryogenic InGaAs HEMTs is strongly dependent on the channel structure and the main reason of “not exceptionally low” is caused of the channel design. These insights contribute to a more comprehensive understanding of the causes of SS variation in cryogenic devices. Therefore, we believe that SS can be further improved in the future by channel structure optimization.

To explain this, we added the following explanation.

Newly added part:

manuscript, line 191-195:

The SS value of 35 mV dec^{-1} is not exceptionally low compared to previously reported cryogenic devices[20,21,33,34]. This is attributed to fluctuations in the channel potential[35,36], which influence the level of disorder within the device, thereby impacting the SS of the device. This effect largely depends on the channel structure[35,36], making the design of an appropriate channel structure important for quantum computing applications.

References:

[33] Ferraris, A., Cha, E., Mueller, P., Moselund, K. & Zota, C. B. Cryogenic quantum computer control signal generation using

high-electron-mobility transistors. *Commun. Eng.* **3**, 1–7 (2024).

[34] Han, Y. *et al.* High Performance 5 nm Si Nanowire FETs with a Record Small SS = 2.3 mV/dec and High Transconductance at 5.5 K Enabled by Dopant Segregated Silicide Source/Drain. In *IEEE Symposium on VLSI Technology and Circuit (VLSI)*, p. T8-4 (2023).

[35] Jeong, J. *et al.* Impact of the channel thickness fluctuation on the subthreshold swing of InGaAs HEMTs at cryogenic temperature down to 4 K for ultra low power LNAs. In *IEEE International Electron Devices Meeting (IEDM)* T34-4 (IEEE, 2023).

[36] Jeong, J. *et al*. Influence of Channel Structure on the Subthreshold Swing of InGaAs HEMTs at Cryogenic Temperatures Down to 4 K. *IEEE Trans. Electron Devices* **71**, 3390–3395 (2024).

[Comments 4]

4. In Fig. 5 the ft versus NIF is benchmarked. However, the ft is given at V_{DS} = 0.5 V and the NIF at 100 mV. It would be important to be clear about this in the text and caption.

[Reply 4]

We believe that it is very meaningful to compare fT and NIF at each optimal operating point to show the full potential of the cryogenic device. However, as the reviewer noted, there was no explanation about it. We agree that clarity in the text and caption is essential.

To address this, we added more detailed information about f_T versus NIF benchmark to the text and caption.

Newly added part:

manuscript, line 300-302:

The f_T and $\sqrt{I_D}\ g_m^{-1}$ are extracted at their respective optimum bias point. For our device, f_T is extracted at V_{DS} of 500 mV and $\sqrt{I_D}\ g_m^{-1}$ is extracted at V_{DS} of 100 mV.

Figure 5a (caption), line 563-564:

The f_T and $\sqrt{I_D}\ g_m^{-1}$ are extracted at each optimum bias point, not at the same bias.

[Comments 5]

In your previous work, gm is significantly higher, almost 2 S/mm at 4 K, while in this work the gm

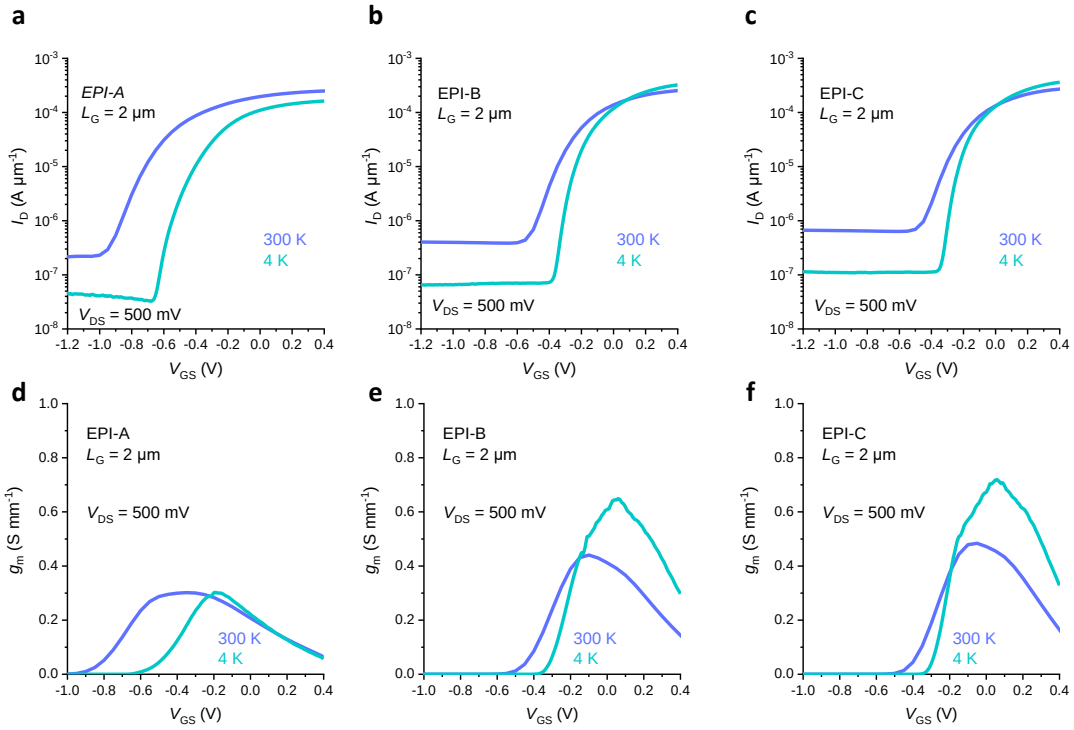
reported in supplementary material is lower, both at 0.5 V. However, ft/max are reporting similar values. What is the explanation for this?

[Reply 5]

The transfer characteristics in Supplementary Figure 5 are those of long-channel devices with L_G = 2 μm for comparing between different barrier thicknesses. Therefore, the g_m of long-channel devices is significantly low compared to our short-channel devices. And we think the confusion is caused because we didn't indicate the gate length of the devices. To avoid any confusion on this point, we added the gate length in Supplementary Figure 5.

Revised part:

Supplementary Figure 5 :



Supplementary Figure 5 | Cryogenic characteristics depending on the III-V heterostructure. **a–c**, Transfer characteristics of III-V HEMTs on Si with L_G = 2 μm and different barrier thicknesses of 9 nm (a), 11 nm (b), 18 nm (c) at 300 K and 4 K. **d–f**, Transconductance characteristics of III-V HEMTs on Si with L_G = 2 μm and different barrier thicknesses of 9 nm (d), 11 nm (e), 18 nm (f) at 300 K and 4 K.

[Comments 6]

6. Does RC change when Nb becomes superconducting? It seems not from supplementary data? But did you confirm the critical current density of the Nb superconductor?

[Reply 6]

As shown in Supplementary Figure 7, we analyzed the R_C at temperatures of 4, 70, 150, 200, 250, and 300 K, and the R_C changes were not significant. When referring to the following recent studies, superconducting properties do not seem to have a significant effect on contact resistivity.

- Zheng, G. *et al.* First Demonstration of Superconducting Nb contact on Heavily-Doped Group IV Semiconductor. *IEEE Symposium on VLSI Technology and Circuit (VLSI)*, p. T14.3 (2024).

In the case of critical current density, although we didn't measure the critical current density of the Nb superconductor, we think that it is a not significant issue because we used this for extremely low-power applications. When referring to the following previous studies, it is well known that the critical current density of thin film Nb superconductors ranges from a few MA/cm^2 to over 10 MA/cm^2.

- Il'in, K. *et al.* Influence of thickness, width and temperature on critical current density of Nb thin film structures. *Phys. C Supercond. its Appl.* **470**, 953–956 (2010).

Because our thin film Nb has a height of 270 nm and width of 20 μm, the critical current is expected to be in the hundreds of mA. Our target application is extremely low-power cryogenic electronics, which generally operate at the range of 10 mA/mm ~ 100 mA/mm (0.2 mA ~ 2 mA). Therefore, we expect that the critical current density will not be a major issue.

To explain this, we added the following explanation.

Newly added part:

Supplementary Infomation, Supplementary Figure7:

Comparing the R_C values from 300 K to 4 K, the R_C changes are not significant.

[Reviewer 2]

[Reviewer's comment]

Comments to the Author

The manuscript by Jeong et al report on III-V and Nb-based cryogenic low-power electronics on a Si platform. The major novelty is the successful demonstration of functional routing circuits based on InGaAs HEMTs and Nb superconducting metallization on Si using direct wafer bonding. As a result, routing circuits and LNAs can be designed in the technology making it feasible for control and readout circuits at 4 K with high performance at low power dissipation. Together with CMOS at 4 K, the reported technology can be attractive for handling the large number of qubits predicted in the on-going upscaling of quantum process units. In my view, however, the full integration in a quantum system (or as the authors claim "potentially solve the power consumption problem and pave the route towards a large-scale quantum computer") will still be challenging because of the fragile qubit information including quantum-noise limited amplifiers, isolators, filters etc in the full readout chain.

[Comments 1]

The successful integration of Nb metallization in a HEMT process on Si is original and is definitively of interest. Routing circuits are demonstrated. However, the authors have missed some references:

Some of the results in the manuscript has previously been published by the authors at VLSI Symposium 2023. Some plots are fully or partly the same (Figs. 1d, 3e,3f, 4a,4b, suppl. Fig. 3b,3c)). The VLSI Symp. paper must be included in the reference list of the current manuscript.

[Reply 1]

As the reviewer pointed out, we reported some of the results of III-V and Nb-based cryogenic electronics in VLSI 2023, which was selected as a highlight paper in VLSI 2023 and a research highlight in Nature Electronics. At that time, we just demonstrated the III-V and Nb-based cryogenic devices. However, in this paper, we provide an extension in terms of results, analysis, and implications over the conference proceedings paper: 1) we provide the cryogenic transport mechanism analysis of III-V heterostructure that needs to be considered for low-power and low-noise operation; 2) we electrically validated all considerations including not only high-frequency characteristics but also noise indication factors for ultralow-power and low-noise cryogenic electronics; 3) we convince why cryogenic III-V and Nb electronics integrated on silicon

are needed for large-scale quantum computing systems through comparison with CMOS-only technology.

To clarify this, we added the reference.

Newly added part:

manuscript, line 94-96:

In this Article, we report high-frequency, low-noise, and low-power cryogenic RF transistors and routing circuits by utilizing III-V-based high-mobility two-dimensional gas (2DEG) channels and Nb-based superconductors integrated on Si, which we conceptually presented in our previous work[22]. Here, we provide an extension in terms of results, analysis and implications over the previous work.

References:

[22] Jeong, J. *et al*. Cryogenic RF Transistors and Routing Circuits Based on 3D Stackable InGaAs HEMTs with Nb Superconductors for Large-Scale Quantum Signal Processing. In *IEEE Symposium on VLSI Technology and Circuit (VLSI)*, p. T7-5 (2023).

[Comments 2]

The integration of InGaAs HEMT circuits (MMICs) on silicon is not new. Please, refer to Leuther et al Proc. 50th European Microwave Conference 2021 , pp. 187.

[Reply 2]

As the reviewer noted, the integration of InGaAs HEMT on Si is already an area of active research by Fraunhofer IAF, IBM, and our group (KAIST). However, most presentations from these groups have demonstrated and analyzed this integration at room temperature. The novelty and/or significance of this study lies in the demonstration of a cryogenic device, specifically designed dedicated to operate at cryogenic temperatures, which needs quite different holistic optimization from the room temperature operation. Additionally, we have successfully introduced Nb superconductors, going beyond the simple integration of InGaAs HEMT on Si, which is highly valuable.

However, as the reviewer pointed out, we agree it is important to inform readers about the existence of InGaAs HEMT on Si technology, and we have included the relevant references below.

Newly added part:

manuscript, line 116-117:

By employing III-V on Si technology through wafer bonding, even RF circuits can be implemented[23,24].

References:

[23] Leuther, A. *et al.* InGaAs HEMT MMIC Technology on Silicon Substrate with Backside Field-Plate. *2020 50th Eur. Microw. Conf. EuMC 2020* 187–190 (2021).

[24] Tessmann, A. *et al.* 20-nm In0.8Ga0.2As MOSHEMT MMIC Technology on Silicon. *IEEE J. Solid-State Circuits* **54**, 2411–2418 (2019).

[Comments 3]

The work claims “state-of-the-art cryogenic performances” with respect to fT, fmax and “noise indicator” sqr(Id)/gm. Also it is claimed rows 202-205: ” These results demonstrate that III-V HEMT on Si-based cryogenic RF transistors not only outperform CMOS-based cryogenic RF transistors but also provide the best performance when compared to conventional III-V-based cryogenic RF transistors. For reading out qubit signals, the ft, fmax and noise indicator are at best indicative of the gain and true noise performance in the microwave range 4-12 GHz crucial for qubit signal readout. Indeed, the noise indicator is not the minimum noise figure. The level of SS and DC curves at 4 K in Fig. 3 suggest that the gm/gds may not be sufficient for competing with the lowest noise HEMTs so far. Only cryogenic noise measurements can tell.

With regard to the HEMT LNA fort qubit readout, state of the art is amplification is typically 40 dB and average noise temperature of 1.4 K in the bandwidth of 4-8 GHz [Ref J. Li, IEEE EDL 43(7) 1029 2022]. This transforms to a minimum noise temperature of the HEMT slightly below 1.0 K at 6 GHz.”

[Reply 3]

Thank you for your insightful comments. As the reviewer highlighted, only direct noise measurement can tell the minimum noise figure. We agree that “the f_T, f_{MAX} and noise indicator are indispensable parameters in evaluating cryogenic devices for qubit signal readout and assessing their overall potential, but the cryogenic performance, especially noise performance, can not be determined by these three parameters”. Recent studies have also reported that the SS of a device is a characteristic that is strongly correlated with noise figures at cryogenic temperature, and as the reviewer said, there is also research that the g_{ds} actually account for a very large portion of the noise source.

- Li, J., Pourkabirian, A., Bergsten, J., Wadefalk, N. & Grahn, J. Influence of Spacer Thickness on the Noise Performance in InP HEMTs for Cryogenic LNAs. IEEE Electron Device Lett. 43, 1029–1032 (2022).

- Li, J., Bergsten, J., Pourkabirian, A. & Grahn, J. Investigation of Noise Properties in the InP HEMT for LNAs in Qubit Amplification: Effects From Channel Indium Content. IEEE J. Electron Devices Soc. 12, 243–248 (2024).

From this perspective, SS and g_{ds} of our devices have not yet been optimized. Nevertheless, the good thing would be that many hints from state-of-the-art stand-alone HEMT technology can be taken in the future. In this context, the claim of "best performance when compared to conventional III-V-based cryogenic RF transistors" may be a bit excessive, as the reviewer pointed out.

Therefore, we softened the relevant claims a bit and added an explanation that it is important to measure the actual minimum noise figure by manufacturing the LNA in relation to noise and that if we introduce a channel structure that is currently being actively studied to reduce noise, the noise characteristics can also be improved further.

Revised part:

manuscript, line 218-221:

These results demonstrate that III-V HEMT on Si-based cryogenic RF transistors not only outperform CMOS-based cryogenic RF transistors but also provide the best performance when compared to conventional III-V-based cryogenic RF transistors.

→ These results demonstrate that III-V HEMT on Si-based cryogenic RF transistors not only outperform CMOS-based cryogenic RF transistors but also provide competitive performance when compared to conventional III-V-based cryogenic RF transistors.

Newly added part:

manuscript, line 221-225:

Recently, researchers have been exploring optimal barrier, spacer, and channel structures to further enhance the 40 dB gain and 1.4 K average noise temperature of state-of-the-art InGaAs HEMT LNAs for quantum computing applications[38,39]. Incorporating such optimized designs into this study could bring us a significant step closer to achieving large-scale quantum computing platforms.

Newly added part:

References:

[38] Li, J., Pourkabirian, A., Bergsten, J., Wadefalk, N. & Grahn, J. Influence of Spacer Thickness on the Noise Performance in InP HEMTs for Cryogenic LNAs. *IEEE Electron Device Lett.* **43**, 1029–1032 (2022).

[39] Li, J., Bergsten, J., Pourkabirian, A. & Grahn, J. Investigation of Noise Properties in the InP HEMT for LNAs in Qubit Amplification: Effects From Channel Indium Content. *IEEE J. Electron Devices Soc.* **12**, 243–248 (2024).

Newly added part:

manuscript, line 313-316:

Of course, f_T and noise indicators do not directly represent the gain and minimum noise levels in an LNA circuit, but it is clear that our device has sufficient potential as a qubit signal readout device. In future studies, a comprehensive evaluation of the minimum noise after LNA fabrication will be necessary[19,38,39].

[Comments 4]

The Nb metallization approach in the manuscript is very interesting since it will provide very low loss at microwave frequencies. However, a drawback, not mentioned by the authors, is that this means a non-alloyed contact for the HEMT and the associated path to the 2DEG. As analyzed by the authors, this will give a high barrier resistance. In a traditional alloyed contact (not superconducting metallization), the barrier resistance does not normally present a problem at 4 K. In a HEMT LNA designed for qubit readout, the channel (gds) will in fact be the dominant noise source.

[Reply 4]

As the reviewer noted, non-alloyed contacts result in high barrier resistance when we design the barrier with thick thickness. However, as our analysis in this paper shows, with an appropriate barrier thickness, the barrier resistance is not very large even with non-alloyed contacts. So the scaling of the barrier is important and this is also a necessary factor for alloyed contacts due to the scaling of gate-to-channel distance. In particular, as can be seen in our recent paper below, if the channel and barrier structure are well designed, the contact resistance can be reached to a ‘state-of-the-art’ alloyed contact.

- Jeong, J. *et al.* Influence of Channel Structure on the Subthreshold Swing of InGaAs HEMTs at Cryogenic Temperatures Down to 4 K. *IEEE Trans. Electron Devices* **71**, 3390–3395 (2024).

Furthermore, non-alloyed contacts are well known for offering better control in processing, improved device reliability, and temperature-independent contact characteristics, as referenced below.

- Alt, A. R. & Bolognesi, C. R. Temperature dependence of annealed and nonannealed HEMT ohmic contacts between 5

and 350 K. *IEEE Trans. Electron Devices* **60**, 787–792 (2013).

- Y. Zhong, W. Wang, S. Sun, P. Ding, Z. Jin, Long-Time Thermal Stability Comparison of Alloyed and Non-Alloyed Ohmic Contacts for InP-Based HEMTs, Phys. Status Solidi Appl. Mater. Sci. **214**, 1700411-1–1700411-5 (2017).

In addition, Nb-based non-alloyed contact will open up new possibilities for achieving extremely low loss at microwave frequencies as the reviewer mentioned. Furthermore, recent research efforts are actively exploring hybrid materials, such as an InAs 2DEG combined with in-situ deposited Nb superconductors, expanding the potential across even more fields. Therefore, we think that the Nb-based non-alloyed contact will better choice for future quantum computing applications. Therefore, we think that the Nb-based non-alloyed contact will better choice for future quantum computing applications.

Newly added part:

manuscript, line 121-123:

Furthermore, the Nb and InGaAs contact is expected to exhibit excellent device reliability due to its non-alloyed nature[25,26]. Recently, research has progressed towards epitaxially growing Nb on III-V materials[27], further expanding its potential across quantum computing applications.

References:

[25] A. R. & Bolognesi, C. R. Temperature dependence of annealed and nonannealed HEMT ohmic contacts between 5 and 350 K. *IEEE Trans. Electron Devices* **60**, 787–792 (2013).

[26] Y. Zhong, W. Wang, S. Sun, P. Ding, Z. Jin, Long-Time Thermal Stability Comparison of Alloyed and Non-Alloyed Ohmic Contacts for InP-Based HEMTs, *Phys. Status Solidi Appl. Mater. Sci.* **214**, 1700411-1–1700411-5 (2017).

[27] Shabani, J. *et al.* Two-dimensional epitaxial superconductor-semiconductor heterostructures: A platform for topological superconducting networks. *Phys. Rev. B* **93**, 1–6 (2016).

[Comments 5]

To be able to reproduce the experiment, details of the InP HEMT channel design must be given.

[Reply 5]

As the reviewer commented, we added the details of the channel design to MATERIALS AND METHODS – Fabrication of heterogeneous and monolithic 3D integrated InGaAs HEMTs on Si.

Newly added part:

manuscript, line 347-349:

The active layers consist of a 40 nm n^+-InGaAs contact layer, 3 nm InP etch stop layer, 9 nm InAlAs barrier with Si delta doping, InGaAs-based QW channel ($In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$, 1/4/3 nm), and 30 nm InAlAs back barrier.

[Comments 6]

Rows 63 and 64: ”To overcome this bottleneck, the idea of placing the control and readout electronics closer to the qubits was proposed as an intermediate solution”. Please, give reference.

[Reply 6]

As the reviewer commented, we added the references.

Revised part:

manuscript, line 63-64:

To overcome this bottleneck, the idea of placing the control and readout electronics closer to the qubits was proposed as an intermediate solution (Fig. 1a (center))[6,7,8].

References:

[7] Craninckx, J. *et al.* CMOS cryo-electronics for quantum computing. In *International Electron Devices Meeting (IEDM)* 25.1.1-25.1.4 (IEEE, 2020).

[8] Charbon, E. *et al.* Cryo-CMOS for quantum computing. In *International Electron Devices Meeting (IEDM)* 13.5.1-13.5.4 (IEEE, 2017).

[Comments 7]

Row 114: Language: a HEMT

[Reply 7]

As the reviewer commented, we revised it.

Revised part:

manuscript, line 117:

an III-V HEMT → a HEMT

[Comments 8]

Rows 125-128: “Through careful design of III-V heterostructure and the introduction of Nb superconductors suitable for III-V, high-performance cryogenic devices with high-frequency, low-noise, and low- power operation were achieved at 4 K, achieving a figure of merit that far exceeds the current state of the art.” Do you mean that you will describe this below? Please, consider to reformulate.

[Reply 8]

Yes, we wrote it to mean that it will be explained below. However, as pointed out by the reviewer, the phrasing used in our original text was ambiguous and could potentially lead to misinterpretation among readers.

To address these concerns and enhance clarity, we have revised the manuscript as follows.

Revised part:

manuscript, 131-135:

Through careful design of III-V heterostructure and the introduction of Nb superconductors suitable for III-V, high-performance cryogenic devices with high-frequency, low-noise, and low- power operation were achieved at 4 K, achieving a figure of merit that far exceeds the current state of the art.

➔ The subsequent discussion details how the careful design of III-V heterostructure and the introduction of Nb superconductors compatible for III-V materials enabled the development of high-performance cryogenic devices. These devices operate at 4 K with high-frequency, low-noise, and low-power consumption, achieving a figure of merit that significantly surpasses the current state of the art.

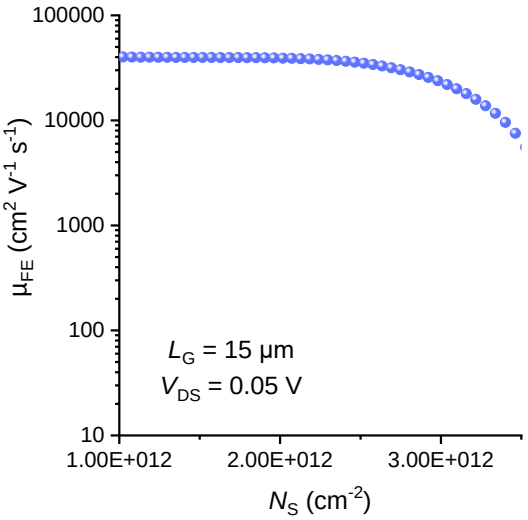
[Comments 9]

Row 135: “(several 10,000 cm2 V-1 s-1)”. Please, be more specific.

[Reply 9]

As the reviewer commented, we provided specific field-effect mobility of our devices.

We extracted the field-effect mobility from long-channel devices as follows.



Revised part:

manuscript, line 142:

mobility (several 10,000 cm^2 V^{-1} s^{-1}) → mobility (40,000 cm^2 V^{-1} s^{-1} at 4 K)

[Comments 10]

Row 150: 91 ohm/sq is relatively high Rsheet at 4 K. This may be due to the Nb metallization approach without alloying. Compare with Schleeh et al, IEEE EDL 33(5) 664 2012: Rsheet = 20 ohm/sq at 4 K .

[Reply 10]

As we replied to [comment 1] of Reviewer 1, we think the main reason why the sheet resistance of our 3D integrated InGaAs HEMTs is slightly higher than that of conventional InGaAs HEMTs is due to the backside interface rather than the introduction of Nb-based non-alloyed contact.

To explain this, we added the following explanation.

Newly added part:

manuscript, line 155-158:

The sheet resistances of 2DEG (R_{2DEG}) in our 3D integrated InGaAs HEMTs range from 91 to 132 Ω

sq^{-1} at 4 K, which is slightly higher than the R_{2DEG} for state-of-the-art conventional InGaAs HEMTs (20 to 90 Ω sq^{-1})[20,30,31,32], mainly due to backside interface, which requires further study to mitigate its impact in the future.

[Comments 11]

Row 156: ” For non-optimized barrier thickness such as EPI-A, the..” Please, refer to definition of EPI-A in Fig. 2c.

[Reply 11]

As the reviewer commented, we revised it.

Revised part:

manuscript, line 164-165:

For non-optimized barrier thickness such as EPI-A,

→ For non-optimized barrier thickness such as EPI-A as shown in Fig. 2c,

[Comments 12]

Rows 164-166: ”However, over-scaling the barrier thickness can 164 cause high gate leakage and generate additional noise, so designing an appropriate barrier 165 thickness is very important, and the 9 nm barrier was used in this study.”

This is true- however, the design of a low-noise HEMT for qubit readout can be made with a more aggressive aspect ratio (gate length to gate-to-channel distance). This is different compared to the design of a THz HEMT or an RF power HEMT. The control over the 2DEG is also dependent on your channel design where details now are left out, see comment above.

[Reply 12]

As the reviewer commented, we added the details of the channel design to MATERIALS AND METHODS – Fabrication of heterogeneous and monolithic 3D integrated InGaAs HEMTs on Si.

Furthermore, we agree with the reviewer that a channel structure suitable for quantum computing is also essential in addition to barrier scaling. This can be seen in detail in papers published by other groups and in a recent paper published by our group.

- Jeong, J. *et al.* Influence of Channel Structure on the Subthreshold Swing of InGaAs HEMTs at Cryogenic Temperatures Down to 4 K. *IEEE Trans. Electron Devices* **71**, 3390–3395 (2024).

- Cha, E. *et al.* Optimization of Channel Structures in InP HEMT Technology for Cryogenic Low-Noise and Low-Power Operation. *IEEE Trans. Electron Devices* **70**, 2431–2436 (2023).

To note the importance of proper channel design for quantum computing applications, we added the following explanation.

Newly added part:

manuscript, line 347-349:

The active layers consist of a 40 nm n^+-InGaAs contact layer, 3 nm InP etch stop layer, 9 nm InAlAs barrier with Si delta doping, InGaAs-based QW channel ($In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$, 1/4/3 nm), and 30 nm InAlAs back barrier.

manuscript, line 193-195:

This effect largely depends on the channel structure[35,36], making the design of an appropriate channel structure important for quantum computing applications.

[Comments 13]

Rows 284-286: ”Second, our device not only surpasses CMOS performance but also demonstrates superior performance compared to previously reported III-V devices.” Please, provide references.

[Reply 13]

As the reviewer commented, we added the references.

Revised part:

manuscript, line 299-301:

Second, our device not only surpasses CMOS performance but also demonstrates superior performance compared to previously reported III-V devices[18,20,21,48,49,50,51].

[Comments 14]

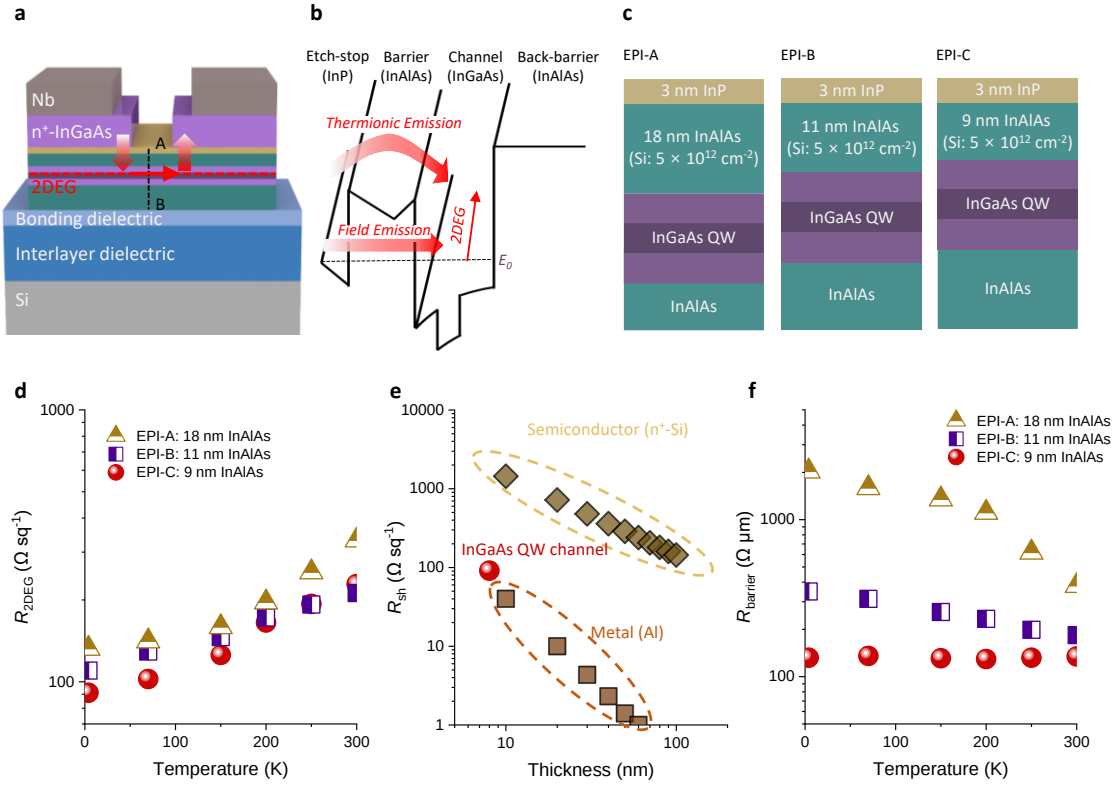
Fig 2e: On the x-axis, specify which thickness.

[Reply 14]

We think that the reviewer pointed this out because it was unclear what thickness “III-V 2DEG” refers to. Thus, to clearify, we revised “III-V 2DEG” to “InGaAs QW channel” as below.

Revised part:

manuscript, Figure 2e:



[Comments 15]

Supplementary Figure 5 caption: Transconductance: Replace (a), (b) ,(c) with (d), (e), (f)

[Reply 15]

As the reviewer commented, we replaced (a), (b), (c) with (d), (e), (f).

Revised part:

Supplementary information, Supplementary Figure 5

Supplementary Figure 5 | Cryogenic characteristics depending on the III-V heterostructure. **a–c**, Transfer characteristics of III-V HEMTs on Si with L_G = 2 μm and different barrier thicknesses of 9 nm (a), 11 nm (b), 18 nm (c) at 300 K and 4 K. **d–f**, Transconductance characteristics of III-V HEMTs on Si with L_G = 2 μm and different barrier thicknesses of 9 nm (d), 11 nm (e), 18 nm (f) at 300 K and 4 K.

[Comments 16]

Supplementary Figure 6: Please, specify the EPI, A, B or C

[Reply 16]

As the reviewer commented, we specified the detail information in Supplementary Figure 6.

Revised part:

Supplementary information, Supplementary Figure 6

Gate leakage current of III-V HEMTs on Si for the same device as in Figure 3a measured at V_{DS} of 50 (dashed) and 100 mV (solid). The measurements were conducted at 300 K and 4 K.

[Comments 17]

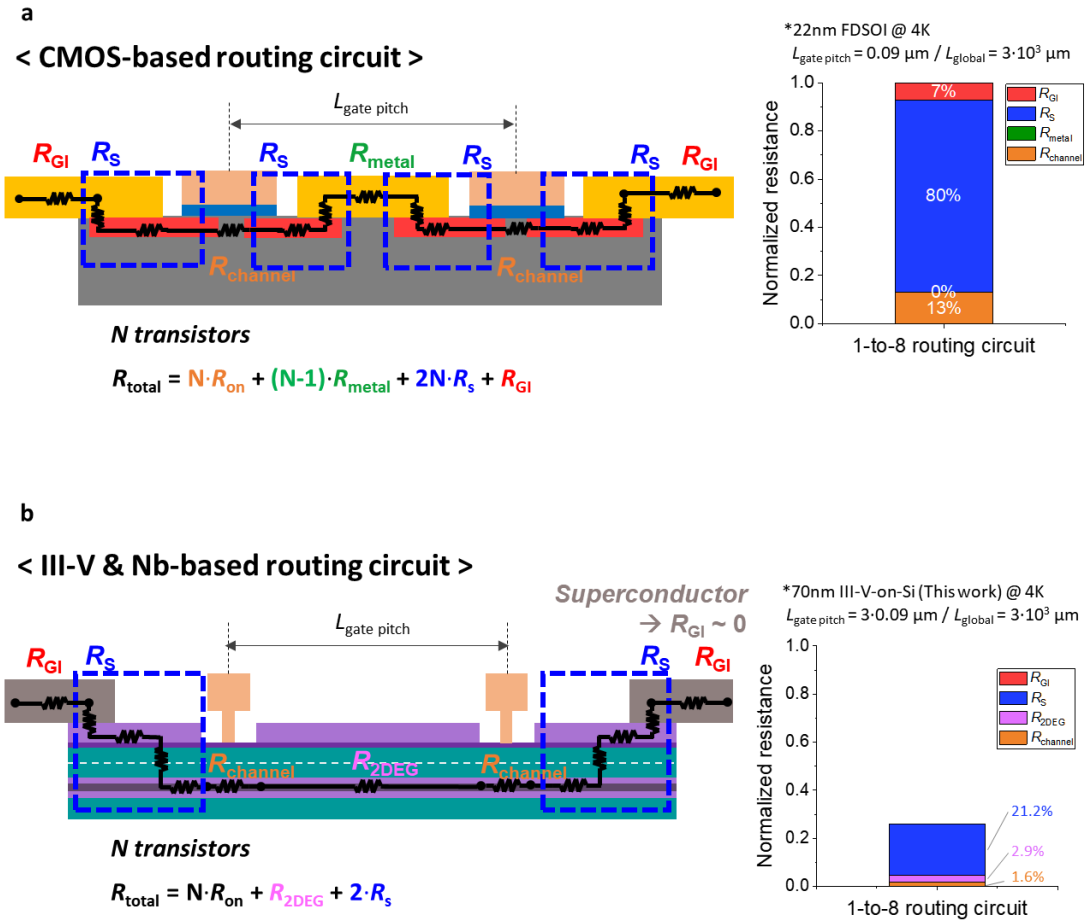
Supplementary row 134: Replace Figure 7 with Figure 8.

[Reply 17]

As the reviewer commented, we replaced Supplementary Figure 7 with Supplementary Figure 8.

Revised part:

Supplementary information, Supplementary Figure 8



Supplementary Figure 7 | Routing circuit structure analysis and resistance comparison when using CMOS (a) and III-V 2DEG & Nb technologies (b).

→

Supplementary Figure 8 | Routing circuit structure analysis and resistance comparison when using CMOS (a) and III-V 2DEG & Nb technologies (b).

We would hope that these revisions, described above, would meet the requirements that the reviewer would need for a publication in *Nature Communications*.

Finally, we would appreciate the reviewer again for his/her valuable comments, which were indispensable in the appropriate revisions of the present paper.

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