Supplementary information for
2D MoS_2-based reconfigurable analog hardware

Supplementary Note

Supplementary Figures

Supplementary Table

Section S1. Fabrication of hardware

The manufacturing details:

UV Photolithography for Source/Drain Electrode Patterning: Ultraviolet (UV) photolithography (MA8 system) was employed on the target substrate to precisely define the geometry and location of the source and drain electrodes. An electron beam evaporation system uniformly deposited a Cr/Au layer (5 nm/35 nm). The thin metal thickness reduced the height difference between the electrodes and the substrate to facilitate a securer transfer of the MoS_2 film.

MoS_2 Protection and Wet Transfer: The MoS_2 film on the SiO_2 substrate was coated with PMMA using spin coating to protect it from damage during the wet transfer process. Wet transfer involved etching the SiO_2 substrate with a 30% KOH solution, and then transferring of the MoS_2 film to the target substrate.

Positive Photoresist Lithography for Channel Definition: After close contact, positive photoresist lithography was performed to pattern the FET channel region and protect the underneath MoS_2 during subsequent etching steps. Ar/SF_6 plasma etching in an ICP system was employed to precisely etch the MoS_2 film, forming the desired channel and other necessary structures.

Dielectric Layer Preparation: Initially, atomic layer deposition (ALD) was utilized to deposit a 30 nm gate oxide layer Al_2O_3 (control oxide) on MoS_2, using trimethylaluminum and water at 250°C. Positive photoresist lithography was applied to define the gate oxide layer pattern, ensuring its protection during subsequent etching steps. Ar/BCl_3 plasma etching was employed to accurately etch the Al_2O_3 layer, forming the required pattern.

Gate Electrode Definition: UV photolithography was performed to define the gate electrode pattern with its shape and size match the design requirements. Using an electron beam evaporation system, a Cr/Au layer (5 nm/50 nm) was deposited to form the gate electrode.

Section S2. Reconfigurable functionality

Reconfigurable functionality is a crucial aspect of modern neuromorphic computing systems, enabling adaptability to various tasks and scenarios. Here, we detail the methodology employed to achieve reconfigurable functionality using synapse, heterosynapse, and soma modules.

Synapse module: The reconfigurability of the synapse module is achieved by controlling external signals to modulate the gate voltage of multiple cascade MoS_2 FETs. This modulation simulates synaptic plasticity by allowing dynamic tuning of the conductance states of cascade FETs under different gate voltages. The conductance state of each FET operates based on a customizable discrete function denoted, enabling the system to emulate various synaptic behaviors and learning rules. This capability

enhances the hardware's adaptability in signal processing within the neuromorphic architecture.

Heterosynapse module: The heterosynapse module is designed to facilitate dynamic connections between different components of the neural circuit-mimicked hardware. It comprises operational amplifiers (OPAs) and multiple MoS_2 FETs (T1–T6). The OPAs serve to isolate the influence of the heterosynapse module on the FETs within the synapse module. The reconfigurability of the heterosynapse module hinges on precise gate control of the MoS_2 FETs in different pathways, enabling the switching among distinct neural pathways. By meticulously adjusting the gate voltages of the FETs, we can selectively activate or deactivate specific connections, thereby altering the behavior of the whole hardware. This capability allows for the establishment or disruption of connections between the synapse module and the soma module. By dynamically configuring these connections, multitasking functionality is achieved, allowing the system to adapt to different tasks by facilitating the flow of information through various pathways within the neuromorphic architecture.

Soma module: The soma module integrates signals transmitted from the front-end circuits—the synapse and heterosynapse modules—and generates a soma-like response, which serves as the output of the neural circuit. It consists of MoS_2 FET-based OPAs and feedback loops that are pivotal in signal processing. The reconfigurability of the soma module is managed by dynamically adjusting the supply voltage. By varying the feedback circuit, we can achieve different operational states of the soma module, altering how incoming signals are processed and integrated. This allows for the execution of diverse computational functions, enhancing the system's adaptability to various computational tasks.

External signals configuring the hardware:

Gate voltage: The gate voltage is the primary external signal controlling the state of the FETs in the heterosynaptic module. By adjusting the gate voltage, each FET’s conduction state can be modulated, enabling or interrupting synaptic connections between neurons. This allows dynamic control over signal transmission within the neural network.

Feedback loops and paths: These gate voltages also regulate the selection of feedback loops within the system. By controlling which feedback loops are activated or deactivated, the heterosynaptic module can dynamically adjust the flow of information through the hardware, simulating various neural processing functions.

Power supply for OPA Structures: In addition to controlling the FETs, the module’s operational amplifier (OPA) structures also require a dedicated power supply. This power supply ensures stable operation and supports the amplification and signal processing tasks within the heterosynaptic module.

Section S3. Design of the operational amplifier

The operational amplifier (OPA) is designed with three stages, including a differential input stage, a main gain stage, and an output stage (Fig. S5). In this three-stage amplifier design, the low-frequency gain of each stage is determined by the square root of the relative W/L ratio of the input transistors. This design philosophy aims to optimize the overall performance of the amplifier with stable and efficient amplification across a wider spectrum.

In hardware implementation, the Wilson current mirror was introduced, consisting of transistors M_5, M_6, and M_8, to provide the necessary bias current for the gain stage. Although bias current is typically supplied by an integrated self-compensating current source, we opt for an external source to simplify the overall circuit design while allowing independent adjustment of bias for each device according to performance requirements. Additionally, the external bias current source provides greater flexibility in circuit design, allowing easier substitution with an external circuit. By considering the characteristics of each stage, the behavior of the entire amplifier can be controlled flexibly, ensuring excellent performance across various application scenarios.

The DC drive voltage was V_{cc}=−V_{ee} = 5V, and the input bias current I_b was 5 μA in experiments. When the OPA functioned as a trans-resistance amplifier, a feedback resistance was introduced between the inverting input and the output, as shown in Fig. S6a. Fig. S6b-d respectively showcase the output characteristics of the inverting voltage amplifier under triangular, sinusoidal, and square wave input waveforms, with input frequencies at 1, 10, 100 and 1000 Hz. Since $R_M = R_{ref}$ = 300 kΩ, the output waveform showed the same amplitude but the opposite phase as the input waveform. The OPA functioned as a voltage comparator without feedback, with the circuit shown in Fig. S7a. Fig. S7b-d respectively present the output characteristics of the voltage comparator under the threshold voltage of 0V, −0.5V, and 0.5V, and various input frequencies of 100, 200, 500, and 1000Hz. The threshold voltage also changed the output square wave duty cycle. For the nonlinear function example of the transition from a low voltage level to a high voltage level in Fig. 1e, the inverting input terminal of the OPA was connected to M_1-M_8, and the threshold voltage V_{th} was 0.3 V at the non-inverting input terminal.

By utilizing a combination of feedback capacitors and resistors, the OPA operated as an integrator and differentiator for integral and differential operations, respectively (Fig. S8 and S9). Fig. S8 shows the feedback circuit and output characteristics of the integration operator under square waves with frequencies of 100, 200, 500, and 1000Hz. The output characteristics satisfy the formula: $V_{out} = -\frac{1}{R_M C_f}\int V_{in} dt$. Fig. S9 shows the feedback circuit and output characteristics of the differentiation operator under square waves with frequencies of 100, 200, 500, and 1000Hz. The output characteristics satisfy the formula: $V_{out} = -R_M C_f \frac{dV_{in}}{dt}$. In addition, the operational amplifiers-based adders and

subtractors were used to add or subtract multiple input voltages. The circuits are shown in Fig. S10. Fig. S11 shows the output characteristics of the adder under square wave (Fig. S11a) and sinusoidal wave (Fig. S11b) with frequencies of 100, 200, 500, and 1000Hz. The output characteristics satisfy the formula: $|V_{out}| = V_{in}^1 + V_{in}^2$. Fig. S12 shows the output characteristics of the subtractor under square wave (Fig. S12a) and sinusoidal wave (Fig. S12b) with frequencies of 100, 200, 500, and 1000Hz. The output characteristics satisfy the formula: $|V_{out}| = V_{in}^1 - V_{in}^2$. These functions made the hardware widely used in electronic circuits and completed complex signal processing and computing tasks. The detailed circuit design is summarized in Table S1.

Section S4. Mechanism of 8-bit DAC

The circuit structure of the 8-bit DAC is illustrated in the left panel of Fig. 2a, comprising 8 cascaded MoS_2 transistors (M_1-M_8). The conductances of the transistors were G_1 (6.06 μS), $G_1/2$, $G_1/4$, $G_1/8$, $G_1/16$, $G_1/32$, $G_1/64$, and $G_1/128$ for M_1-M_8, respectively. In this configuration, one terminal of each transistor received the input signal, while the other terminal was connected to the inverting input of the OPA. The non-inverting input of the OPA was grounded. Simultaneously, a feedback resistor (R_{ref} = 300 kΩ) was introduced between the inverting input and the output of the OPA.

Within the synapse module, the 8-bit input signals were distributed across the 8 cascaded MoS_2 FETs, all contributing to the overall analog output. The conductance of each MoS_2 FET modulated the transformed analog voltage level to the corresponding bit. The grounded terminal of the transistors provided a common reference point for the input signal, facilitating a controlled and precise conversion process. Within the soma module, the OPA functioned as a trans-resistance amplifier to convert the current signal into the voltage signal. The feedback resistor R_{ref} controlled the gain and shapes the analog output, further enhancing the accuracy of generating the analog signal. The RAH ensures a reliable and controlled digital-to-analog conversion process, crucial for various applications in signal processing and communication systems.

To utilize hardware resources more efficiently with adjustable resolution, the 4-bit and 6-bit DACs were designed using the same method. In this configuration, the FET resistance was regulated according to the discrete equation j_1. The output characteristics of transistors M1-M4 in the 4-bit DAC (M1-M6 in the 6-bit DAC) are shown in the inset of Fig. 1a (I). In the soma module, the OPA still acted as an inverting voltage amplifier. Fig. S14a (Fig. S17a) represents encoded square wave voltage signals of V_{DA1} – V_{DA4} (V_{DA1} – V_{DA6}) for the 4-bit DAC (6-bit DAC). Therefore, the output signal satisfies eq. 1 (eq. 2) for the 4-bit (a 6-bit) DAC.

$$V_{out} = -\left(\frac{V_{DA1}}{R_1} + \frac{V_{DA2}}{R_2} + \frac{V_{DA3}}{R_3} + \frac{V_{DA4}}{R_4}\right) \times R_{ref} \quad (1)$$

$$V_{out} = -\left(\frac{V_{DA1}}{R_1} + \frac{V_{DA2}}{R_2} + \frac{V_{DA3}}{R_3} + \frac{V_{DA4}}{R_4} + \frac{V_{DA5}}{R_5} + \frac{V_{DA6}}{R_6}\right) \times R_{ref} \quad (2)$$

Fig. S14b and c (Fig. S17b and c) show the output current and output voltage according to the above equations. The 4-bit DAC had an output voltage range of 0-0.36V, while the 6-bit DAC had an output voltage range of 0-0.9V. Furthermore, the voltage values of adjacent digits can be distinguished, confirming the adjustable DAC resolution.

Section S5. Mechanism of 8-bit ADC

The circuit of the 8-bit ADC, as shown in the right panel of Fig. 2a in the main text, employs cascaded MoS_2 transistors (M1-M8) of the synapse module and a voltage comparator in the soma module. The cascading 8 MoS_2 transistors (M_1-M_8) were interconnected with the inverting input terminal of the OPA. Additionally, a load resistor (R_{load} = 300 kΩ) was integrated at the inverting input to establish the reference voltage, V_{load}, which linearly increases within each conversion cycle. The conductance of each transistor was designated as G_1 (6.06 μS), $G_1/2$, $G_1/4$, $G_1/8$, $G_1/16$, $G_1/32$, $G_1/64$, and $G_1/128$ to M_1-M_8, respectively.

The cascading 8 MoS_2 transistors received 8 square wave signals with an exponentially increasing frequency (the fundamental frequency of the input signal (V_{AD1}) is 1Hz), a peak voltage of 0.1V, and a duty cycle of 50%, to sweep V_{load}. The analog voltage to be converted was introduced to the non-inverting input and compared with V_{load}. When the input voltage keeps exceeding V_{load}, the square wave output signal of the ADC is at a high level, otherwise the ADC outputs a low voltage level. Thus, the square wave output signal of the ADC shows varying time widths in each conversion cycle, applied to obtain the corresponding 8-bit binary digital signal. The formula $B = f(256 * t / t_{period})$ is used to convert the time width t to a binary digital signal B, where f is the function used for decimal to binary conversion and t_{period} (= 1s) is the time of a conversion period.

To utilize hardware resources more efficiently, the 4-bit and 6-bit ADCs were designed using the same method. Fig. S15a (Fig. S18a) shows the encoded square wave input signals V_{AD1} -V_{AD4} (V_{AD1} -V_{AD6}) for the 4-bit ADC (6-bit ADC). An approximate sine shape input signal V_{in} was quantized by a sampling V_{sh}, as shown in Fig. S15b (Fig. S18b). The 4-bit binary or 6-bit binary digital signal was obtained by measuring the time width of the square wave output signals of the 4-bit ADC or the 6-bit ADC. The evolutions of V_{out} and V_{ref} during the converting process were measured in Fig. S14c and Fig. S17c. This ADC hardware exhibited outstanding performance, accuracy, and versatility for applications demanding high resolution and efficient data acquisition.

Section S6. Image pixel conversion within the 8-bit DAC and ADC

Image pixels were converted based on the 8-bit DAC and ADC, with the procedure

shown in Fig. 2e. First, each selected pixel value was encoded into an 8-bit binary digital signal. In this encoding process, the binary digit "1" was mapped to a voltage of 0.1V, and the binary digit "0" was mapped to a voltage of 0V (Fig. 2e (I)). Then each 8-bit voltage signal was transmitted into the corresponding input port V_{DAj} (j = 1-8) of the DAC and the respective analog voltage values at the output port were recorded (Fig. 2e (II)), thus achieving the conversion of digital signals to analog signals. The analog voltage output values of the DAC were 0.255 V, 0.269 V, 0.637 V, 1.889 V, 1.437 V, and 3.070 V, respectively, for the 6 selected pixels (Fig. 2f). Subsequently, the obtained analog voltage output values were fed into the non-inverting input port of the OPA in the ADC, to convert it back into the binary representation for comparison with the original values. The eight programmed MoS_2 transistors connected to the inverting input of the OPA in the ADC received square wave signals with exponentially increasing frequencies (peak voltage of 0.1V, duty cycle of 50%), as shown in Fig. 2e (III). The fundamental frequency of the input signal V_{AD1} was 1 Hz and the load resistance (R_{load}) was 300 kΩ. The voltage comparator in the ADC output square wave signals with varying time widths in each converting period (Fig. 2e (IV)). The time widths were used to obtain the corresponding 8-bit binary digital signal to complete the conversion of analog signals to digital signals. In experiments, the selected 6 grayscale pixels exhibited converting time widths t of 70.313 ms, 74.219 ms, 175.781 ms, 519.531 ms, 394.531 ms, and 843.750 ms, respectively (Fig. 2g). Then the selected 6 grayscale pixels were encoded into binary digital signals of A (00010010), B (00010011), C (00101101), D (10000101), E (01100101), and F (11011000), respectively (Fig. 2d).

Section S7. Operation processing of sparse coding model

To construct a sparse coding model, we started by selecting a column vector containing 256 random coefficients, which were then converted into 256 8-bit digital signals for subsequent processing. Here, bit “1” was mapped to 0.1V, and bit “0” was mapped to 0V. In the forward DA conversion, 256 DACs converted these 256 sets of digital signals into 256 sets of analog voltages. The first iteration of forward DA conversion is shown in Fig. 3c (I). Subsequently, these 256 sets of analog voltage signals were used to generate 64 sets of analog signals after multiplication and sum operations within a 256 × 64 memory array. Then in the forward AD conversion, 64 ADCs converted these 64 sets of analog signals back into 64 sets of digital signals. The first iteration of forward AD conversion is shown in Fig. 3c (II). These 64 sets of digital signals from the forward calculation output and the corresponding original 8 × 8 image patch were subtracted for error calculation, generating 64 sets of digital signals for backward computation.

In the backward DA conversion, the 64 sets of digital error values were fed back into 64 DACs, converted into 64 sets of analog voltage values. The first iteration of

backward DA conversion is shown in Fig. 3c(III). These 64 sets of analog voltage values were then subjected to the same multiplication and sum operations in the memory array, transformed to 256 sets of analog voltage values. Finally, in the backward AD conversion, the 256 sets of analog voltage outputs from the memory array were reconverted into digital signals using 256 ADCs. The first iteration of backward AD conversion is shown in Fig. 3c (IV).

Through iterative forward and reverse calculation processes (Fig. S19), we obtained precision-optimized high-quality sparse coefficients. The establishment of this sparse coding model effectively utilizes the reciprocal conversion between digital signals and analog voltages, as well as the iteration between forward and reverse calculations, resulting in the efficient generation of high-quality sparse coefficients. In the process of sparse coding training, a dictionary containing 256 basis functions was introduced to achieve an effective representation of new signals (Fig. S20a). These basis functions were converted into analog voltages through DAC and underwent multiplication and operations in the memory array. After 100 iterations of sparse coding ($\lambda = 2.2$), the activation levels of each basis function were adjusted to adapt to the characteristics of the input signal, further enhancing the effectiveness of sparse coding.

To assess the effectiveness of the hardware, hardware function 6 was implemented to perform Gaussian convolution operations, as found in Fig. S24. Subsequently, the noise was introduced to clear images of buildings and vegetables using hardware function 6 (Fig. S25a (I) and b (I)). Experimentally, the peak signal-to-noise ratio (PSNR) reached 20.1026 dB for the building image, and the PSNR was 20.2940 dB for the vegetable image, confirming the effective addition of noise (Fig. S25a (II) and b (II)). Fig. S25a (III) and b (III) illustrate the reconstructed results, where the PSNR for the building image reached 27.1774 dB, and for the vegetable image, the PSNR was 28.5609 dB, providing further validation of the effective image reconstruction. These experiments substantiate the outstanding performance of the hardware in noise processing and image reconstruction. It establishes a solid foundation for its reliable application in various scenarios.

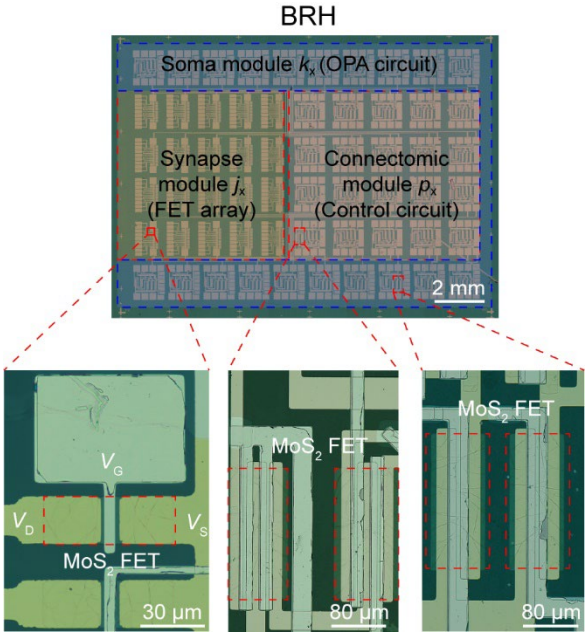
Section S8. Mechanism of the visual persistence and the switch attention

Fig. 4a shows the schematic of attention switching and visual persistence for auto driving. Neurons accept input data from the range of the receptive field (RF), and they can process input data through attention switching and visual persistence. Autonomous driving systems require the capability to allocate and switch attention to different scenes and events. Attention switching in hardware can enable flexible responses to complex traffic environments, promptly attending to sudden occurrences such as obstacles or pedestrians unexpectedly entering the roadway.

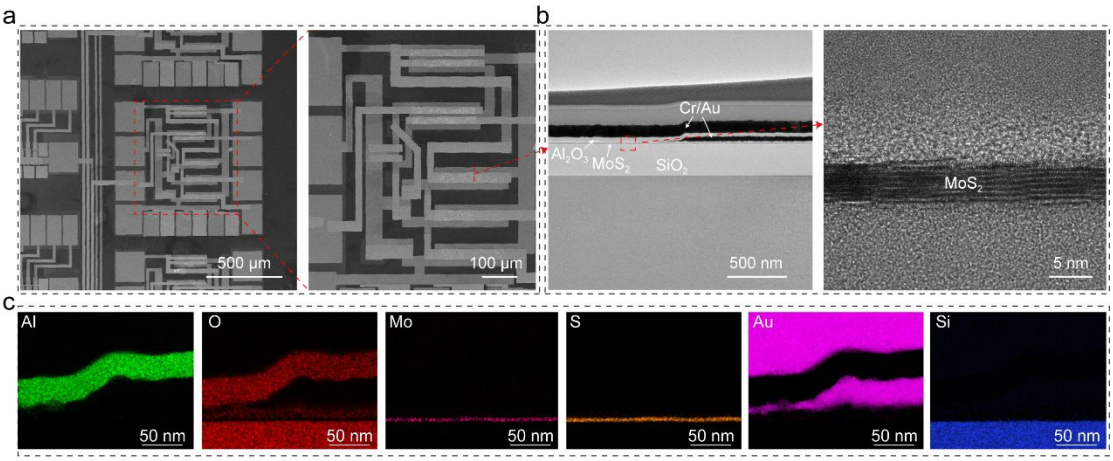
As shown in Fig. 4a (I), when external objects move from the left side of the field

of view to the right, the RF of the visual system can rapidly switch from the left to the right, effectively shifting attention. Without visual persistence, only the environmental information acquired in the active receptive field will be processed, while the system ignores information outside the active receptive field (Fig. 4a (II)). Therefore, the output signal changes immediately when the RF is shifted. This RF selection serves to enhance data sparsity, reduce redundancy, and better capture critical features. With visual persistence, the visual system still computes information from the previous RF in a short timescale after shifting the active RF (Fig. 4a (III)). Therefore, the output signal responded to the previous RF persists and its disappearance is delayed after the RF is shifted. This visual persistence mechanism allows more complex bio-behaviors such as the prediction of object trajectories, which can be implemented to greatly enhance the precision of decision-making in autonomous driving scenarios. Therefore, applying these processes in autonomous driving systems can enhance the vehicle's understanding of and responsiveness to the surrounding environment. In addition, visual persistence can simulate the driver's observation habits, where memorized information continues to be considered by the system for a period after the stimulus vanishes, thereby improving the efficiency of utilizing momentary information.

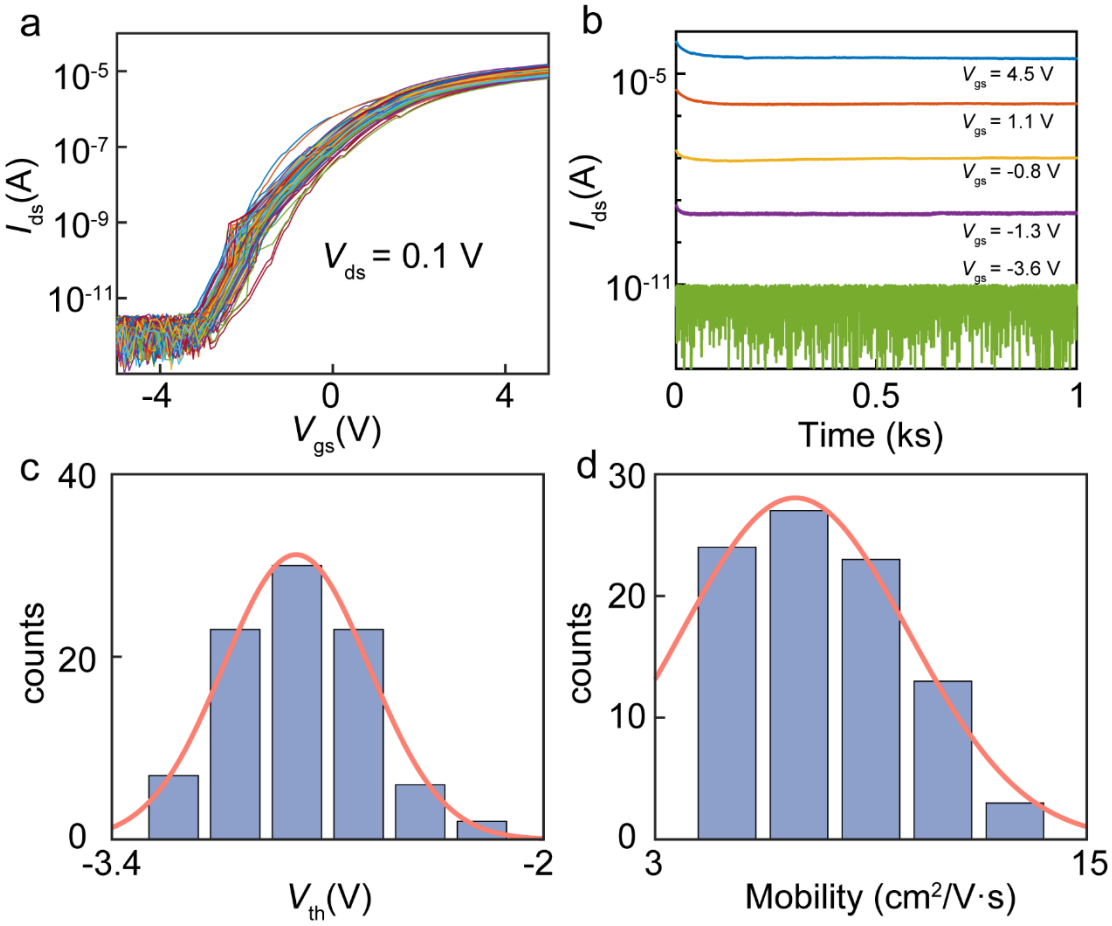
Our experimental outcome underscores the impact of the conductivity of each perceptron neuron on RF characteristics, indicating that differences in conductivity can be utilized to modulate the sensitivity and response of the RF. The adjustable sensitivity of the RF is also discussed in detail (Fig. S28). The geometric sequence equation j_4 was programmed for the synapse module, in which each FET (M_1–M_8) represented a separate neuron. In the soma module, the first-stage OPA worked as a current-to-voltage conversion sub-function k_1 and the second-stage OPA worked as a voltage comparator sub-function k_2. A fixed threshold voltage (V_{th}) was applied to the inverting input of the second-stage OPA. The square wave signals with an input pulse width of 10 ms and an amplitude of 0.1 V were applied to M_1 or M_2 as stimulus signals in sequence. At the high amplitude $V_{th} = -0.3$V, both stimulation to M_1 or M_2 generated a low-level output. However, at the $V_{th} = -0.15$V, the low-level output was maintained during stimulation to M_1, representing that the perception in M_1 didn't activate the RF. In contrast, stimulation to M_2 generated high-level output, indicating the RF was activated by the perception in M_2. This was due to the higher conductivity of M_2 than that of M_1. Under low V_{th} conditions, the activated RF exhibited high sensitivity to stimuli, making it easier to generate a high-level output under external stimuli. Under high V_{th} conditions, the response of the RF to the stimulus was weakened, making it harder to activate the RF. This conductivity-based RF modulation approach holds promise for information processing and sensing applications, particularly in scenarios requiring dynamic adjustments to perceptual sensitivity.



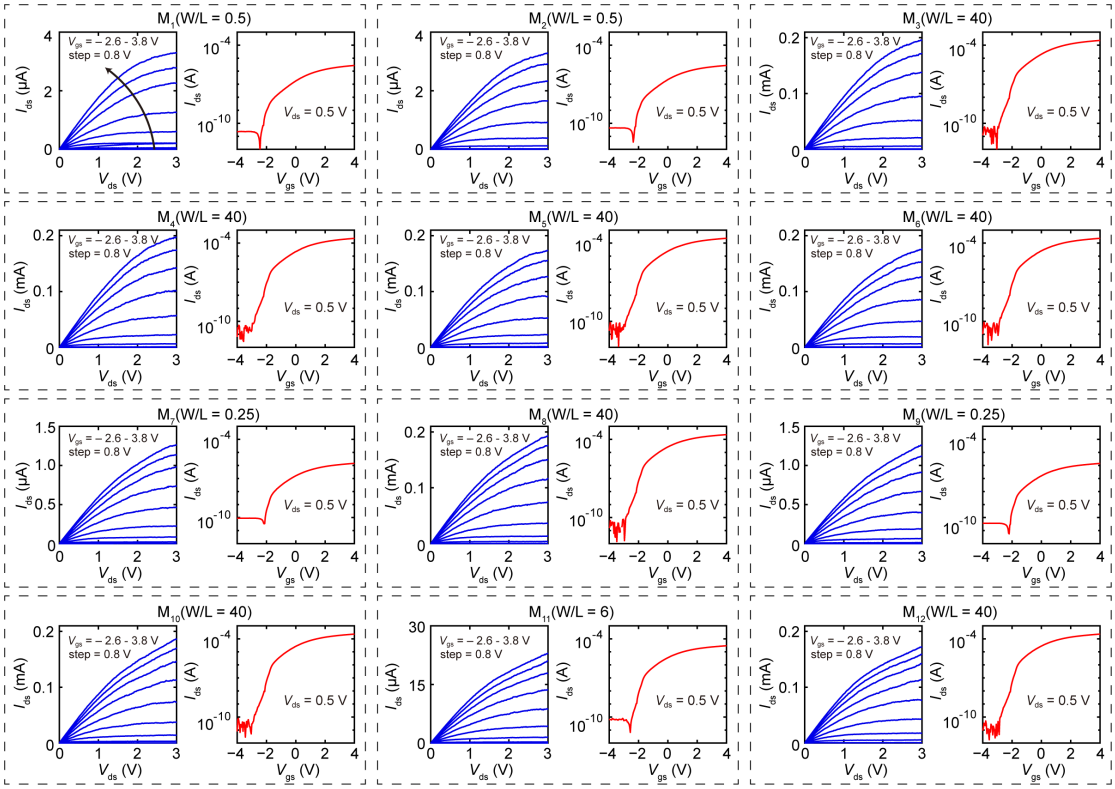
Supplementary Fig. 1 | The optical images of the biology-inspired reconfigurable hardware (RAH). The optical images of the entire hardware (the upper panel) and the zoomed-in units (the bottom panel) including a synapsemodule, a connectomic module, and a soma module.



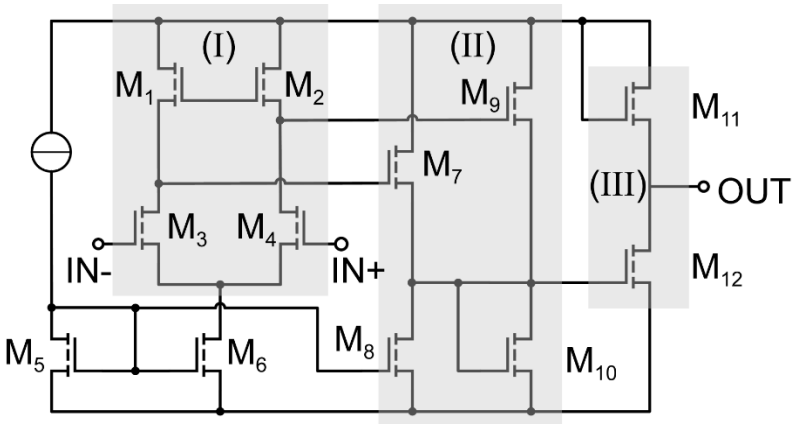
Supplementary Fig. 2 | SEM, STEM, and EDS Analysis of RAH. a, Scanning electron microscope (SEM) images of the device, with the left panel depicting the overall structure and the right panel presenting a magnified view, respectively. **b,** Scanning transmission electron microscope (STEM) cross-sectional images. **c,** Energy-dispersive X-ray spectroscopy (EDS) elemental mapping, showing the distribution of Al, O, Mo, S, Au, and Si across the cross-section of device.



Supplementary Fig. 3 | The experimental cascade transistor characteristics of the hardware. a, Transfer characteristics of 90 transistors spread over the hardware area (V_{DS} = 0.1 V). **b,** Stable conductivity over multiple gate voltages. **c,** Histogram of the threshold voltage values extracted from the transfer characteristics in (a). **d,** Histogram of the electron mobility values extracted from the transfer characteristics in (a).

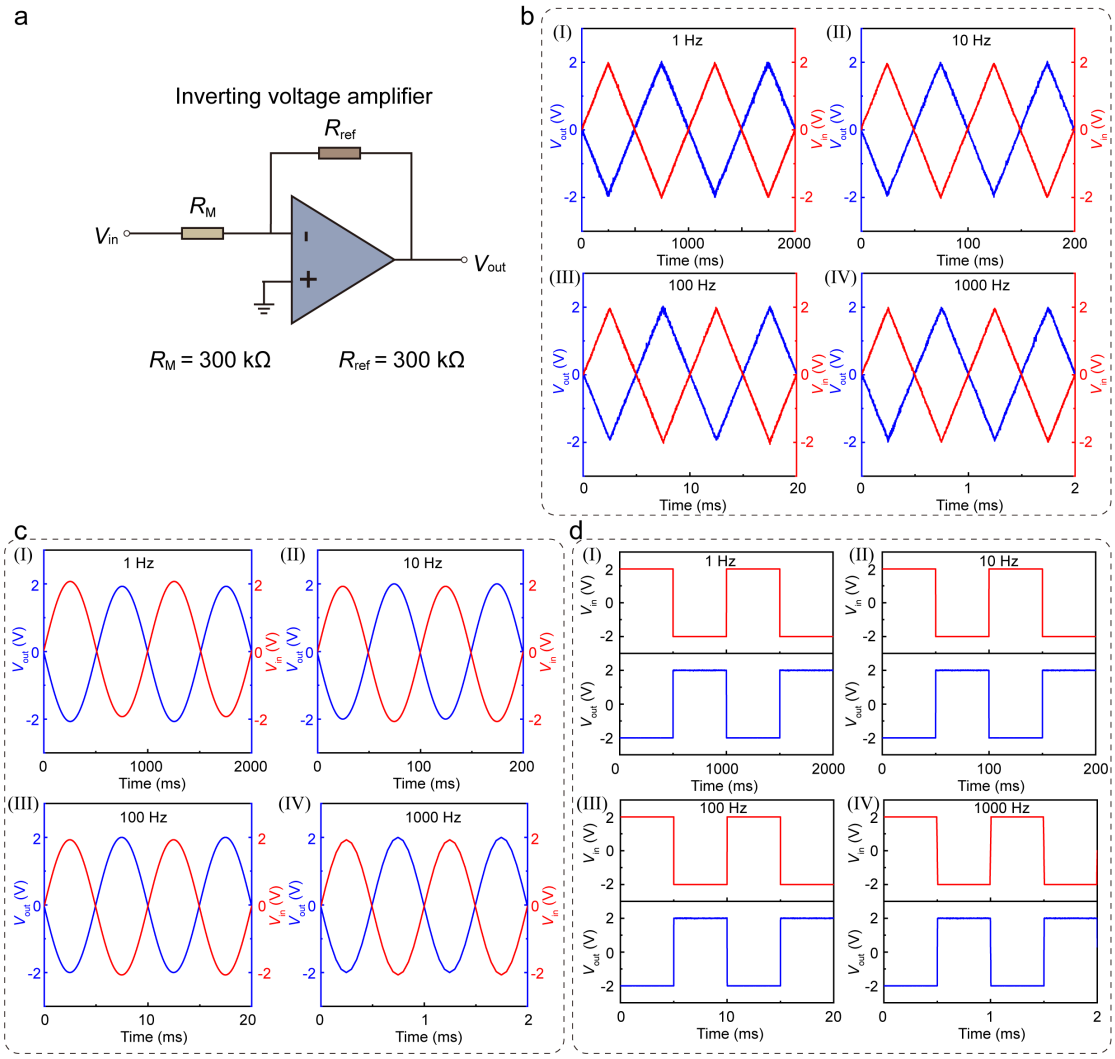


Supplementary Fig. 4 | The experimental MoS_2 transistor characteristics of OPA. Output characteristic curves and transfer characteristic curves of 12 transistors. For the output characteristics, V_{gs} ranges from -2.6 V to 3.8 V in steps of 0.8 V. The transfer curve is obtained at V_{ds}=0.5 V.

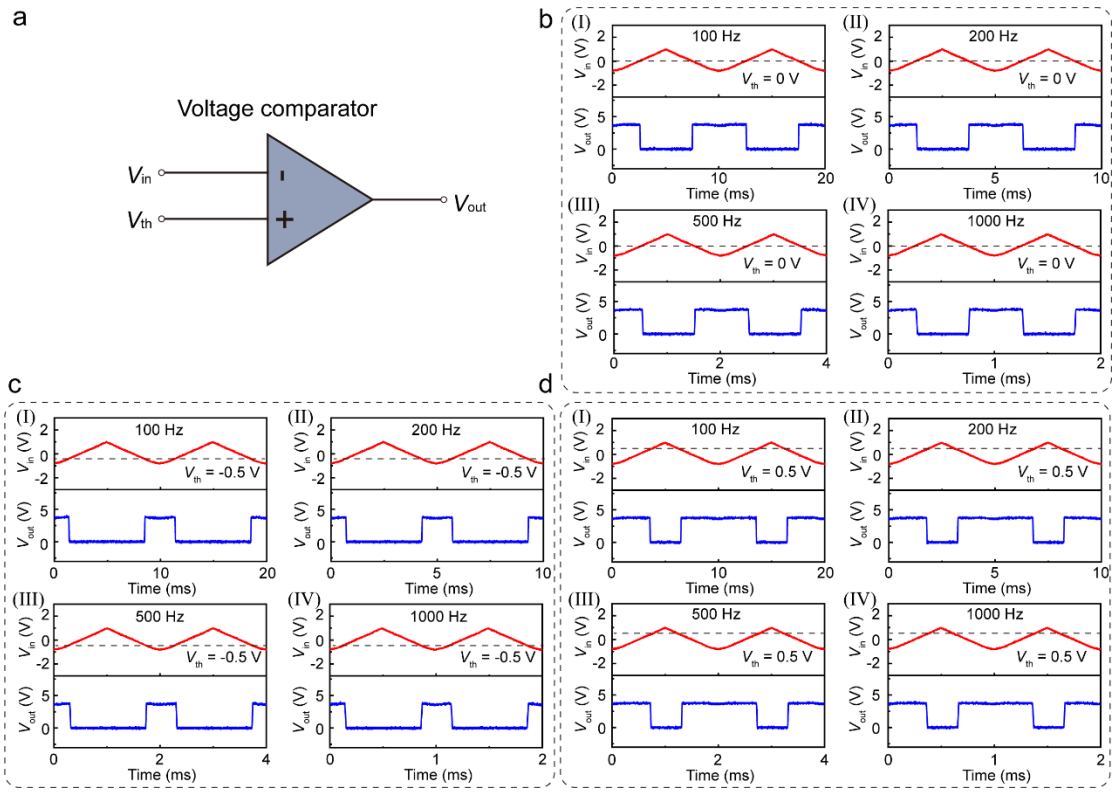


Transistors	W/L
M_1, M_2	0.5
$M_{3\text{-}6}$, M_8, M_{10}, M_{12}	40
M_7, M_9	0.25
M_{11}	6

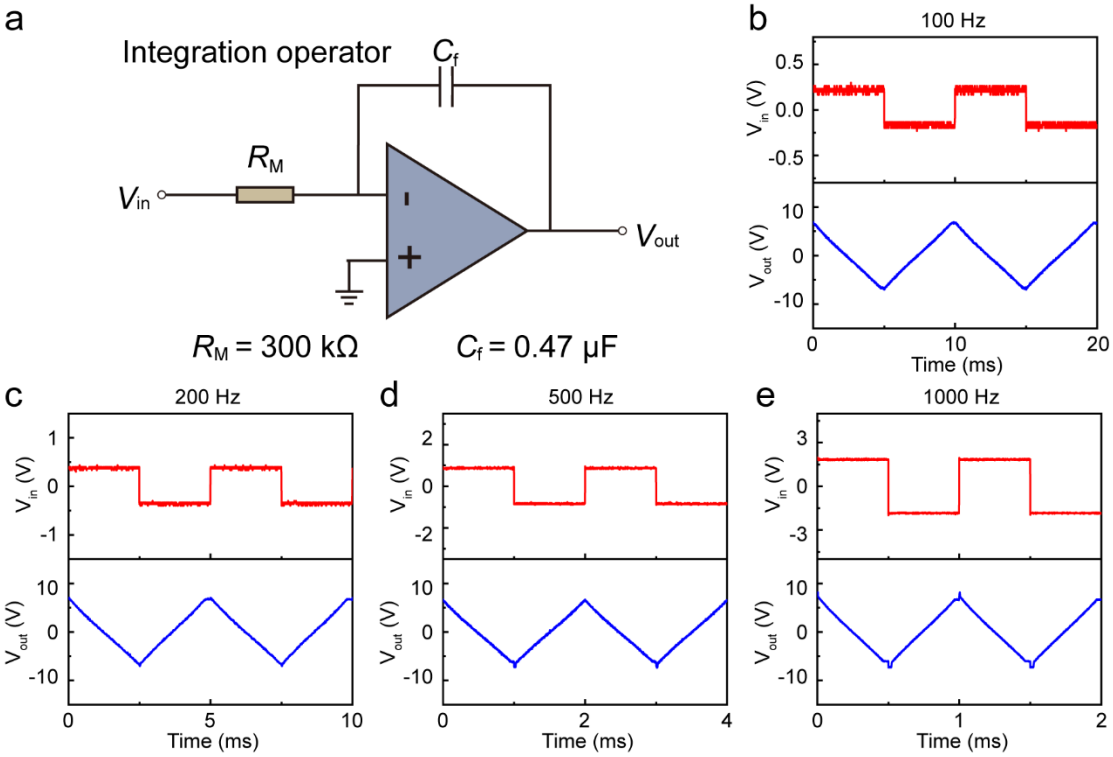
Supplementary Fig. 5 | The circuit connection diagram of OPA. The different stages of the OPA are highlighted: (I) differential input stage, (II) main gain stage with external capacitor used for phase-compensation and (III) output stage. The right panel is the W/L information of the corresponding device.



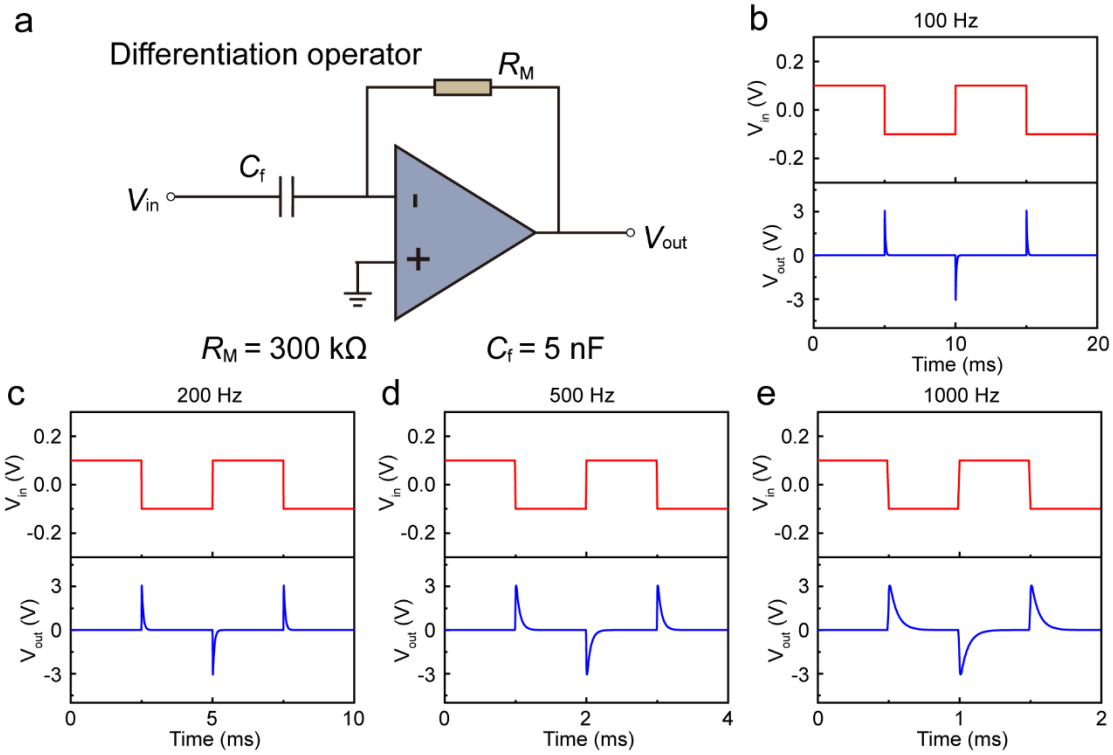
Supplementary Fig. 6 | The circuit and output characteristics of the inverting voltage amplifier. a, The circuits of the inverting voltage amplifier. **b-d,** Output characteristics of three waveforms, including triangle wave (b), sine wave (c), and square wave (d). Output characteristics of four frequencies, including 1Hz (b(I), c(I), and d(I)), 10Hz (b(II), c(II), and d(II)), 100Hz (b(III), c(III), and d(III)), and 1kHz (b(IV), c(IV), and d(IV)).



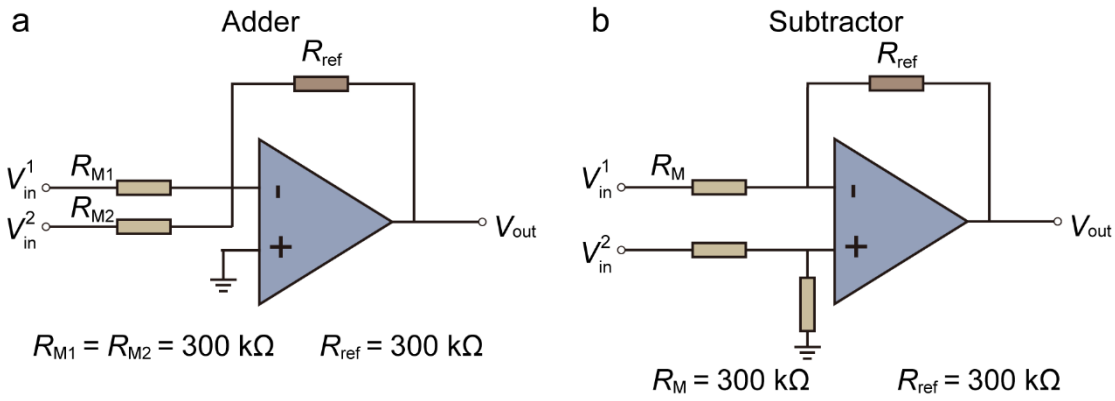
Supplementary Fig. 7 | The circuit and characteristics of the voltage comparator. **a,** The circuits of the voltage comparator. **b-d**, Output characteristics of three threshold voltages, including 0 V (b), -0.5 V (c), and 0.5 V (d). Output characteristics of four frequencies, including 100Hz (b(I), c(I), and d(I)), 200Hz (b(II), c(II), and d(II)), 500Hz (b(III), c(III), and d(III)), and 1kHz (b(IV), c(IV), and d(IV)).



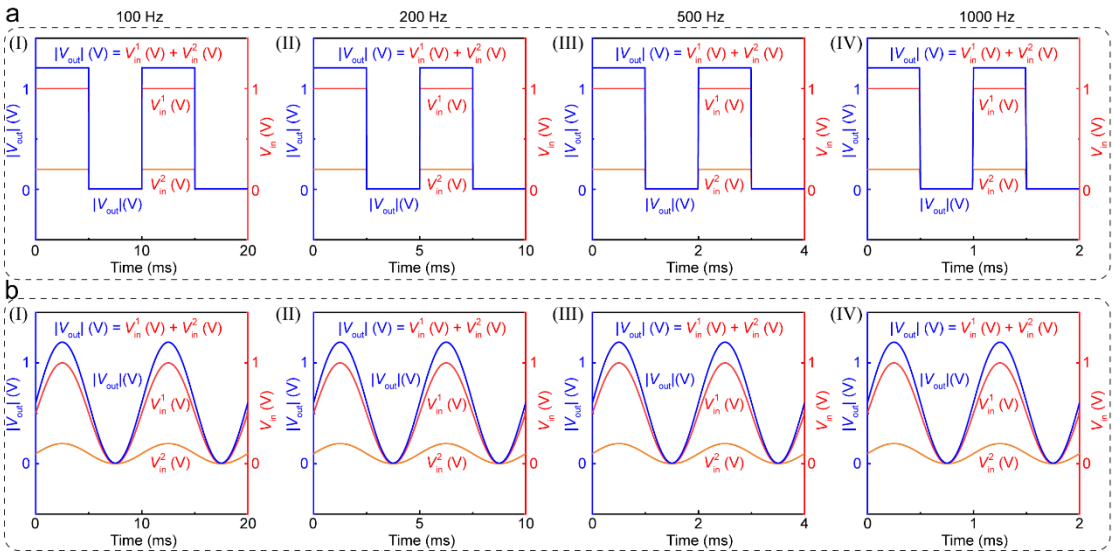
Supplementary Fig. 8 | The circuit and characteristics of the integration operator. **a,** The circuits of the integration operator. **b-e,** Output characteristics of four frequencies, including 100Hz (b), 200Hz (c), 500Hz (d), and 1kHz (e).



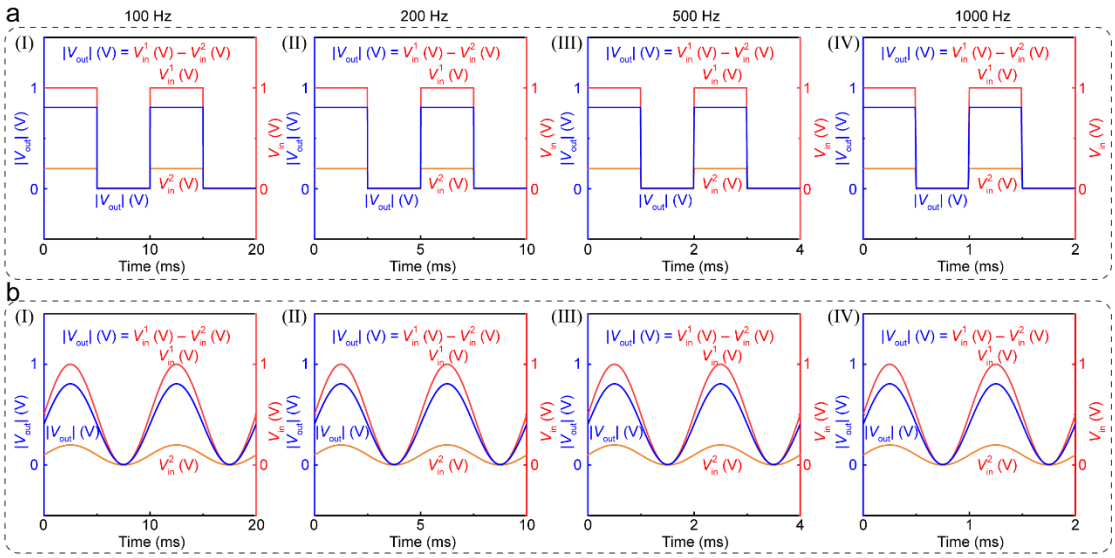
Supplementary Fig. 9 | The circuit and characteristics of the differentiation operator. a, The circuits of the differential operator. **b-e,** Output characteristics of four frequencies, including 100Hz (b), 200Hz (c), 500Hz (d), and 1kH (e).



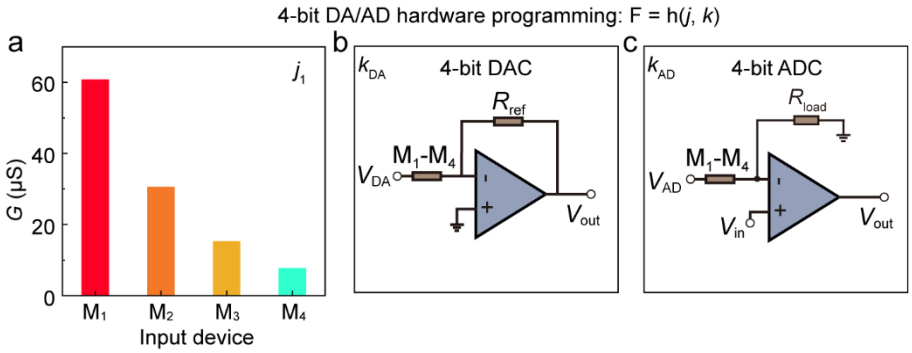
Supplementary Fig. 10 | Circuits configuration of adder and subtracter. a, The circuits of the adder. **b,** The circuits of the subtractor.



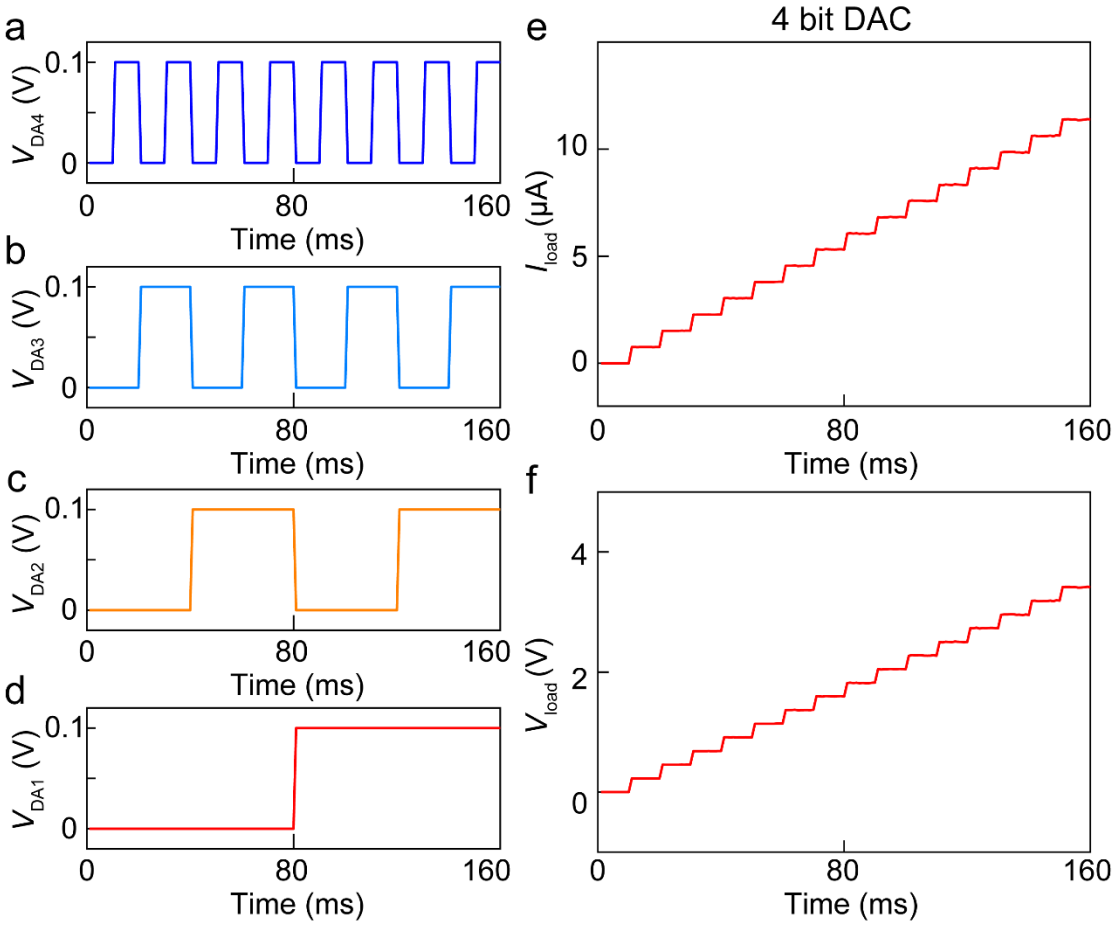
Supplementary Fig. 11 | Output characteristics of the adder. a and b, Output characteristics of two waveforms, including triangle wave (a) and sine wave (b). Output characteristics of four frequencies, including 100Hz (a(I) and b(I)), 200Hz (a(II) and b(II)), 500Hz (a(III) and b(III)), and 1kHz (a(IV) and b(IV)).



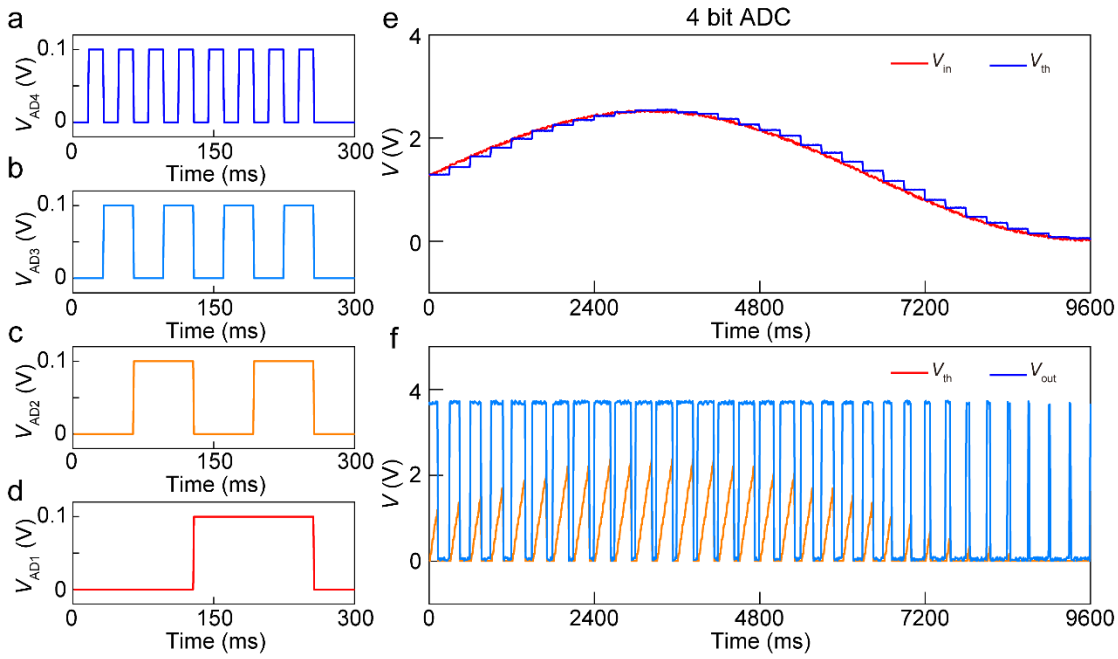
Supplementary Fig. 12 | Output characteristics of the subtracter. a and b, Output characteristics of two waveforms, including triangle wave (a) and sine wave (b). Output characteristics of four frequencies, including 100Hz (a(I) and b(I)), 200Hz (a(II) and b(II)), 500Hz (a(III) and b(III)), and 1kHz (a(IV) and b(IV)).



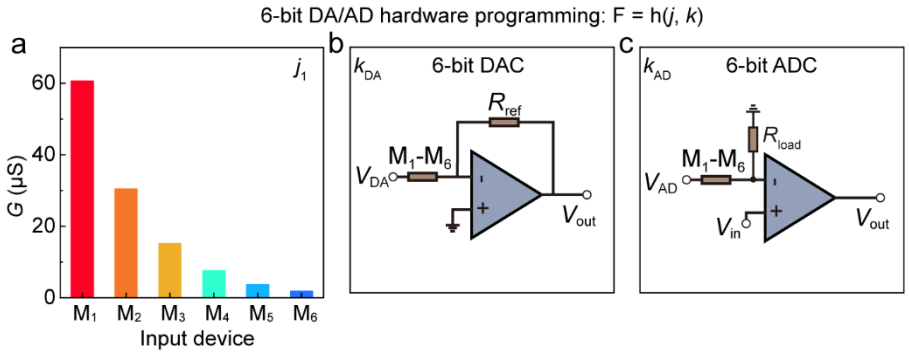
Supplementary Fig. 13 | Optimally configured circuit accuracy for 4-bit DAC/ADC hardware. a, A geometric sequence equation *j*: $G_n = G_1/2^{n-1}$ (n = 1-4) in the synapse module. **b,** A current-to-voltage conversion sub-function k_{DA} in the soma module to implement the 4-bit DAC. **c,** A voltage comparator sub-function k_{AD} in the soma module to implement the 4-bit ADC.



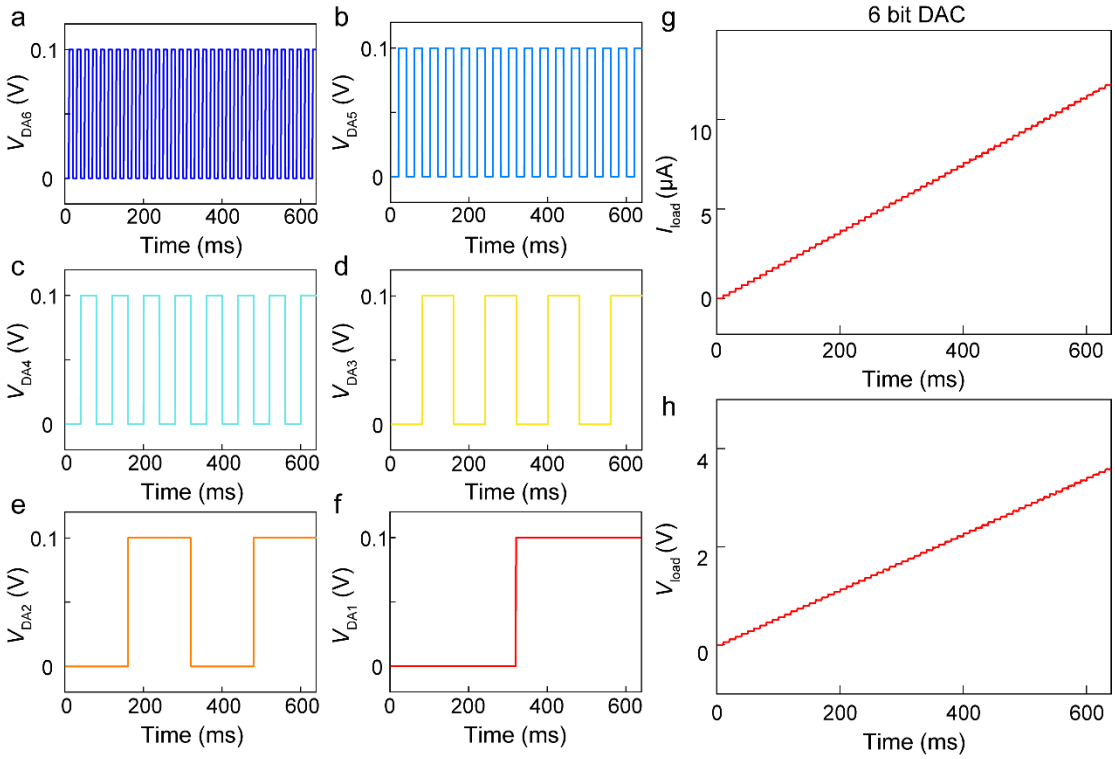
Supplementary Fig. 14 | Output characteristics of 4-bit DAC. Input signal (a-d), output current signal (e), and voltage signal (f) of 4-bit DAC.



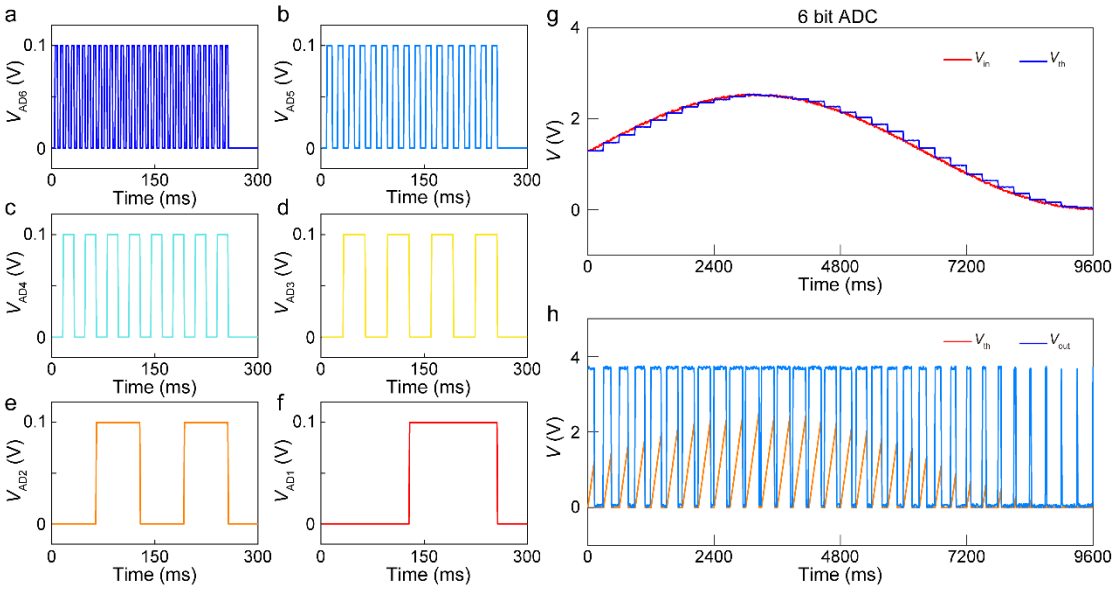
Supplementary Fig. 15 | Output characteristics of 4-bit ADC. a-d. The 4 ports connected to the inverting input of the ADC received square wave signals with exponentially increasing frequencies (peak voltage of 0.1V, duty cycle of 50%). **e.** Input signal (red curve) and sampled signal (blue curve) during 9600 ms of the 4-bit ADC. **f.** Output signal (blue curve) and threshold signal (orange curve) of the 4-bit ADC.



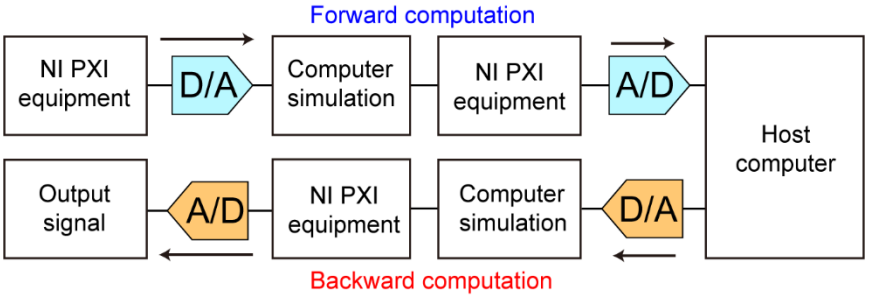
Supplementary Fig. 16 | Optimally configured circuit design for 6-bit DAC/ADC hardware. a, A geometric sequence equation *j*: $G_n = G_1/2^{n-1}$ (n = 1-6) in the synapse module. **b,** A current-to-voltage conversion sub-function k_{DA} in the soma module to implement the 6-bit DAC. **c,** A voltage comparator sub-function k_{AD} in the soma module to implement the 6-bit ADC.



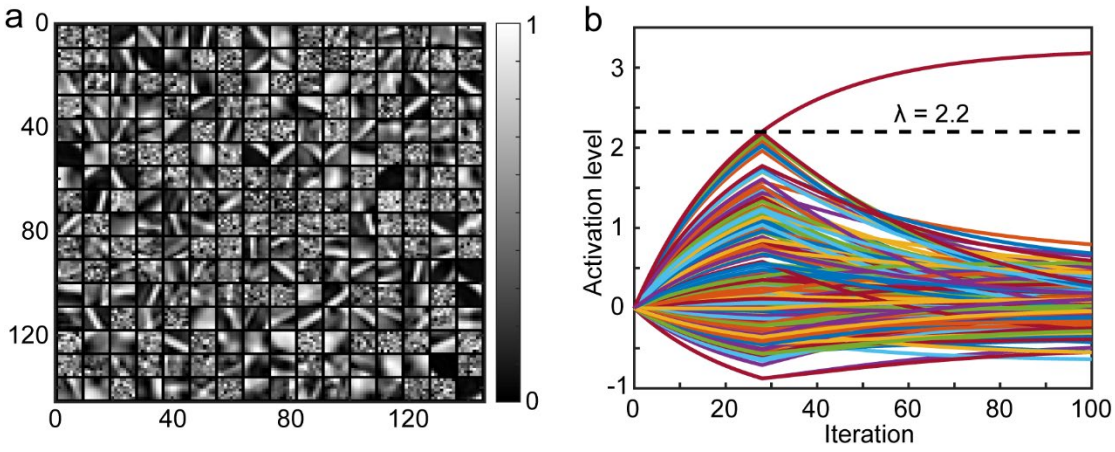
Supplementary Fig. 17 | Output characteristics of 6-bit DAC. Input signal (a-f), output current signal (g), and voltage signal (h) of the 6-bit DAC.



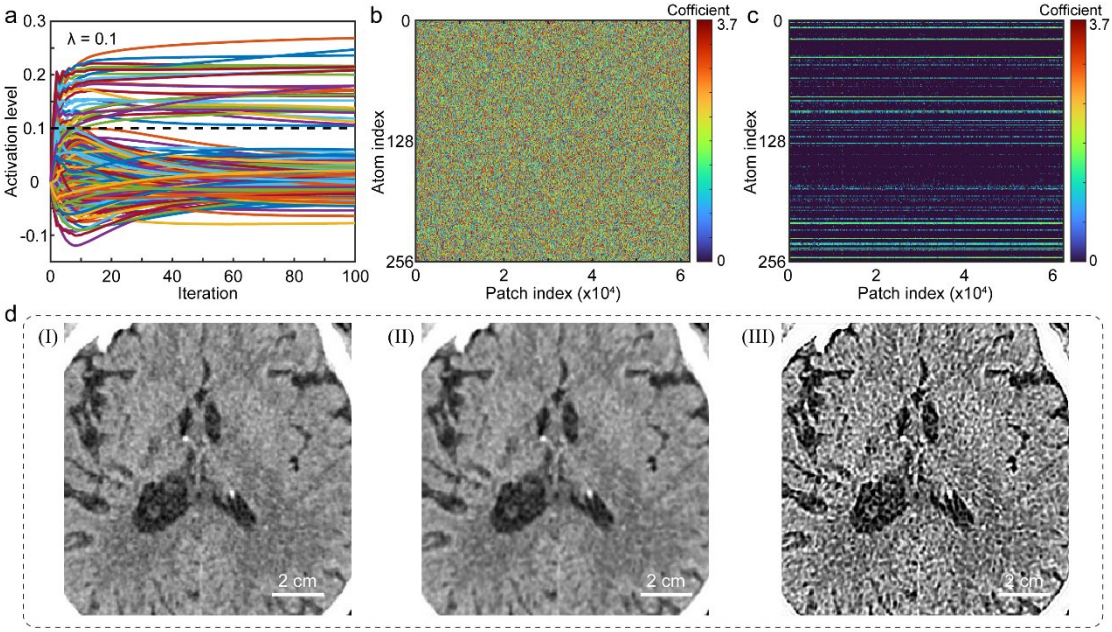
Supplementary Fig. 18 | Output characteristics of 6-bit ADC. a-f. The 6 ports connected to the inverting input of the ADC received square wave signals with exponentially increasing frequencies (peak voltage of 0.1V, duty cycle of 50%). **g.** Input signal (red curve) and sampled signal (blue curve) during 9600 ms of the 6-bit ADC. **h.** Output signal (blue curve) and threshold signal (orange curve) of the 6-bit ADC.



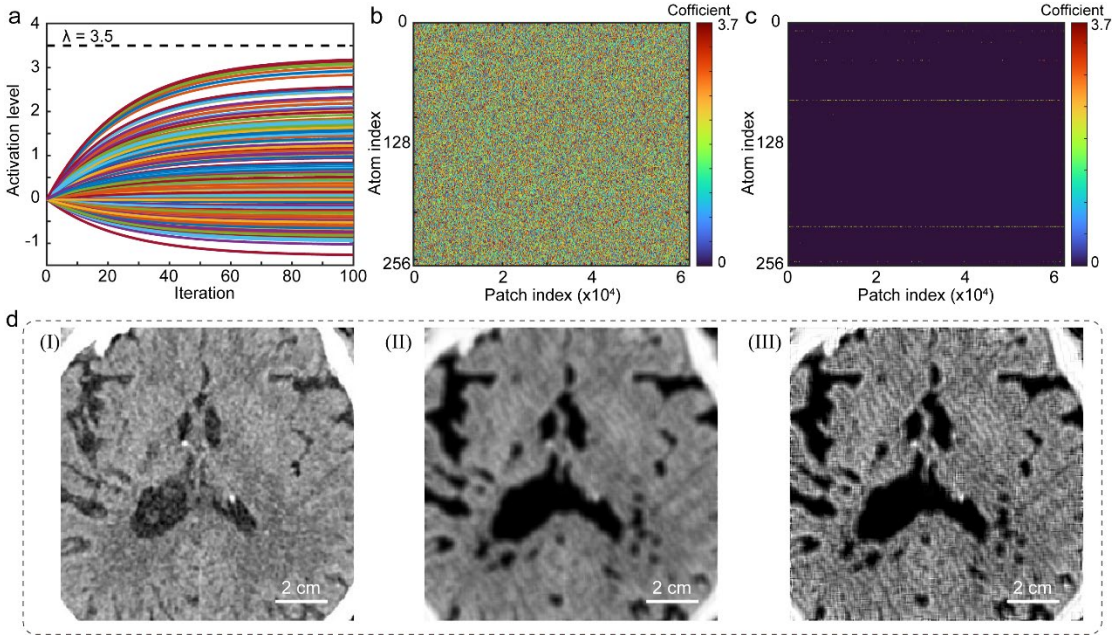
Supplementary Fig. 19 | Block diagram illustrating the forward and backward computation processes.



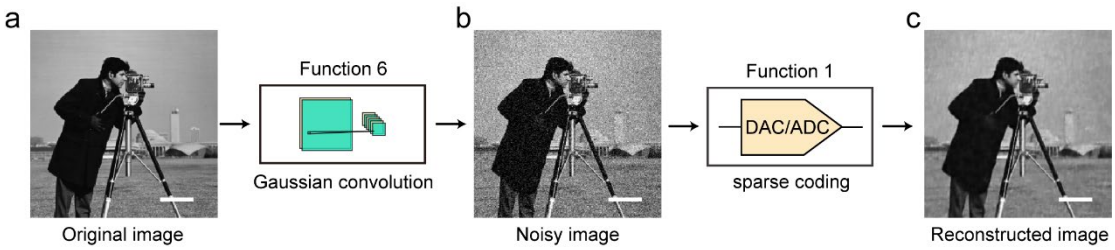
Supplementary Fig. 20 | Dictionary and activation levels of sparse encoding. a, Dictionary for sparse coding. Each column in the dictionary represents an atom or basis function that is used to represent a different feature of the input data. **b,** Activation levels of each basis function after 100 sparse coding iterations at $\lambda = 2.2$. These activation levels reflect the sparsity of the input data in the dictionary representation. The horizontal black dashed line represents the threshold parameter λ.



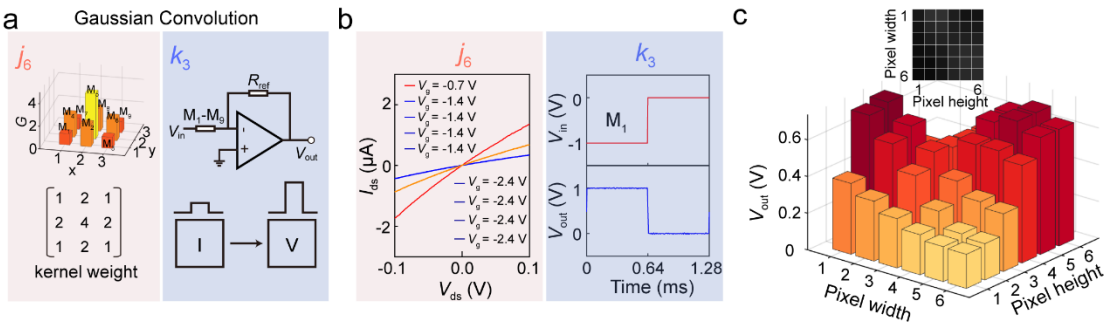
Supplementary Fig. 21 | The processing of input images by sparse coding at λ=0.1. **a,** Activation levels of each basis function after 100 sparse coding iterations at λ = 0.1. **b,** Original coefficients of input data. **c,** The coefficients of each basis function after sparse coding calculations. These coefficients reflect the sparsely encoded representation of the input data. **d,** The original image (I), the reconstructed image (II), and the feature extraction image (III) after sharpening convolution calculation. Each subfigure illustrates a different stage in the image processing pipeline.



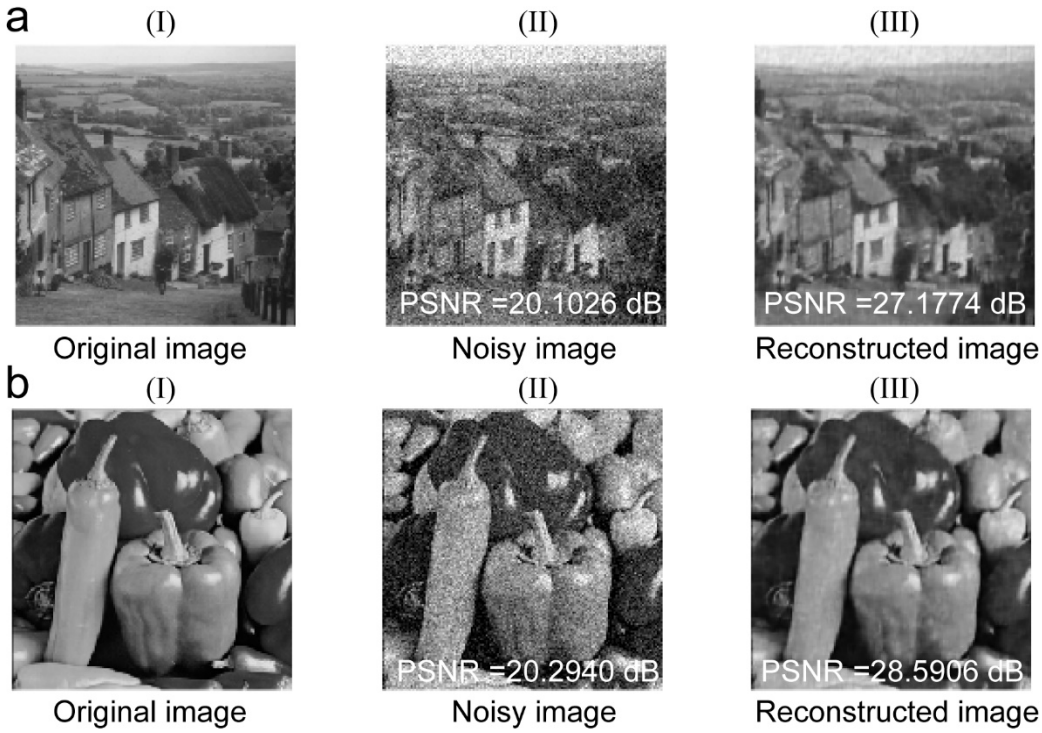
Supplementary Fig. 22 | The processing of input images by sparse coding at λ=3.5. **a,** Activation levels of each basis function after 100 sparse coding iterations at λ = 3.5. **b,** Original coefficients of input data. **c,** The coefficients of each basis function after sparse coding calculations. These coefficients reflect the sparsely encoded representation of the input data. **d,** The original image (I), the reconstructed image (II), and the feature extraction image (III) after sharpening convolution calculation. Each subfigure illustrates a different stage in the image processing pipeline.



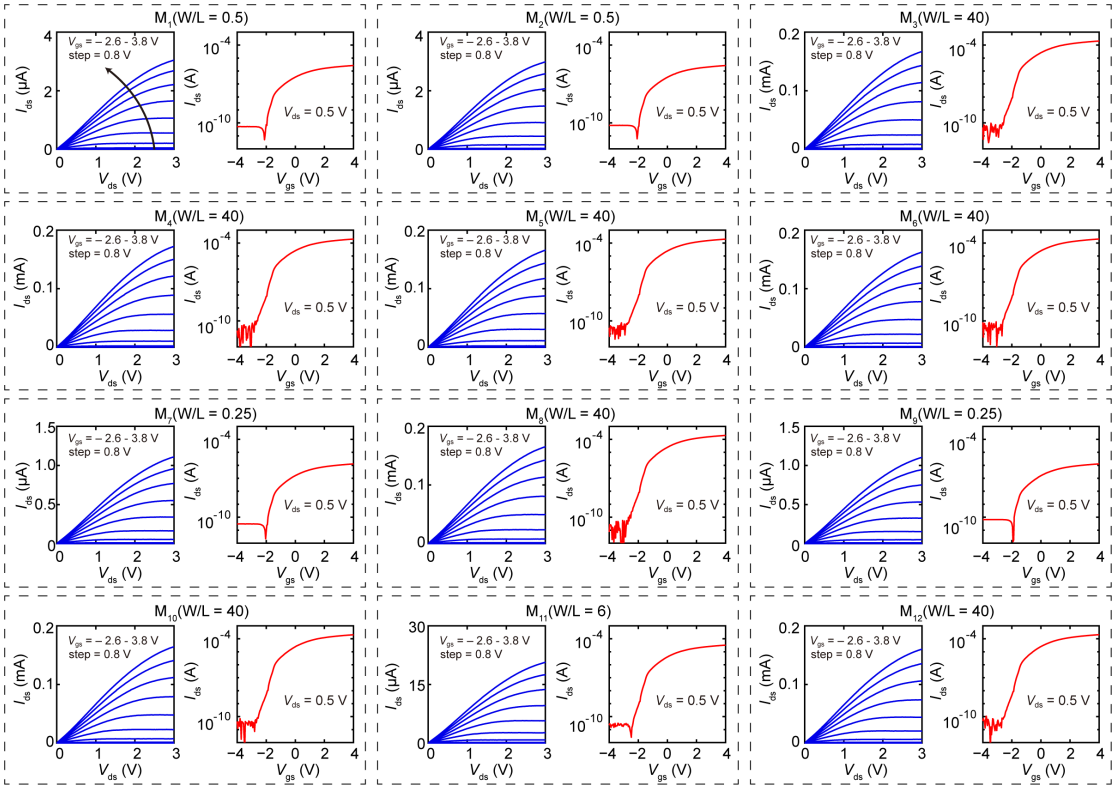
Supplementary Fig. 23 | The processing of input images by non-linear computing and sparse coding. a-c, Noise addition and reconstruction of original images using the gaussian convolution (function 6) and ADC/DAC (function 1). The gaussian convolution function is employed for image to add noise. The ADC/DAC function is used for image reconstruction in sparse coding.



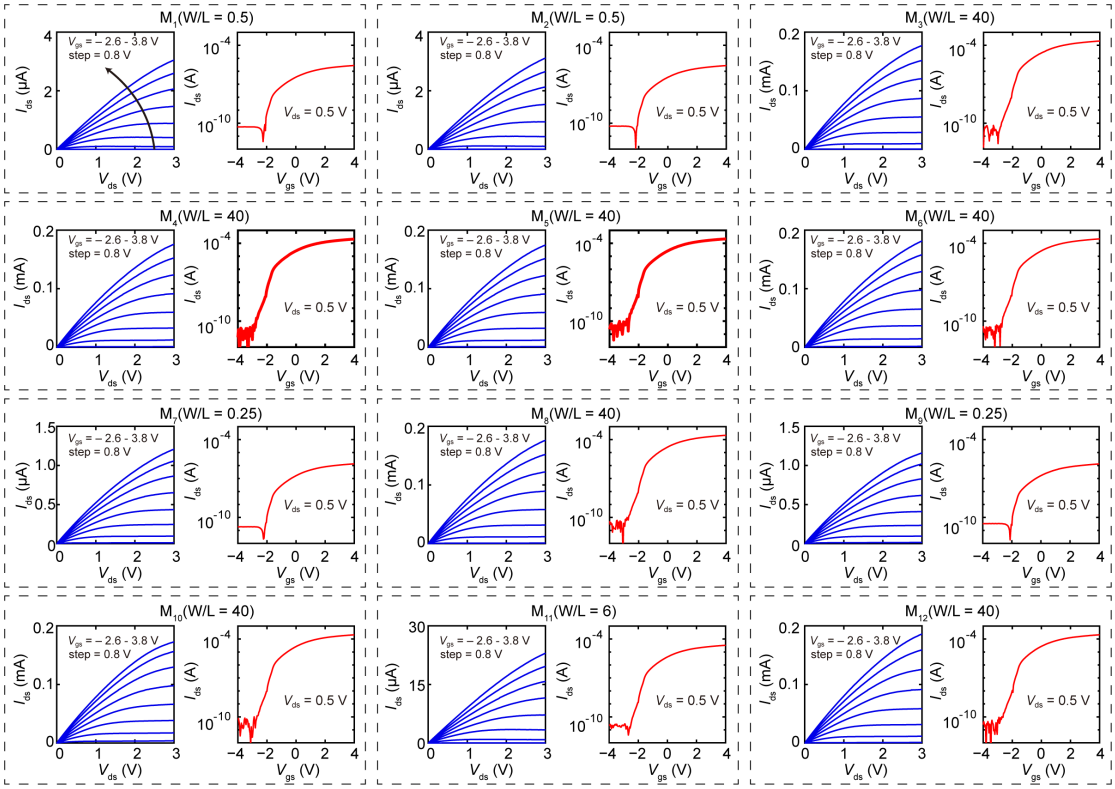
Supplementary Fig. 24 | The circuit configuration of Gaussian convolution. a, Configuration of the hardware for gaussian convolution (function 6), which consists of sub-function j_6 (convolutional kernel) and sub-function k_3 (trans-impedance amplifier). **b,** Experimental results of sub-function j_6 and sub-function k_3. **c,** Output current of a 6 × 6 patch from the CNN. The 2D grayscale image of the 6 × 6 patch was illustrated in the inset.



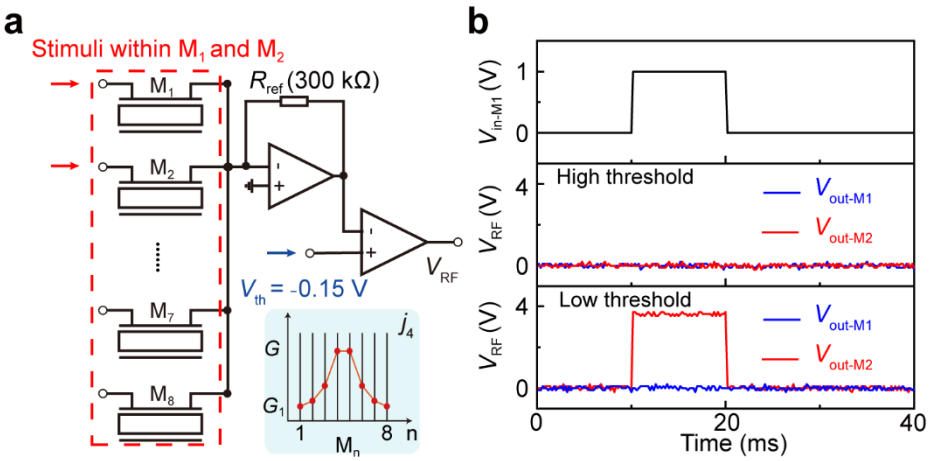
Supplementary Fig. 25 | Performance evaluation of sparse coding process and convolution calculation on images. a, Processing of building images, including original image (I), image after adding Gaussian filter noise (II), image restoration after sparse coding calculation and convolution calculation (III). Peak Signal-to-Noise Ratio (PSNR) of noisy image is 20.1026 dB, and PSNR of reconstructed image is 27.1774 dB. **b,** Processing of vegetable images, including original image (I), image after adding Gaussian filter noise (II), image restoration after sparse coding calculation and convolution calculation (III). PSNR of noisy image is 20.2940 dB, and PSNR of reconstructed image is 28.5906 dB.



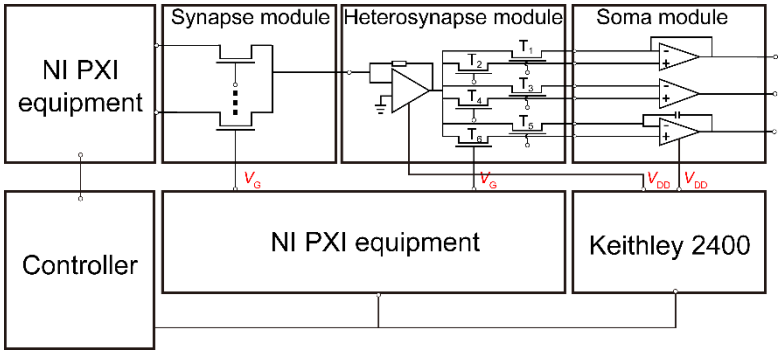
Supplementary Fig. 26 | The experimental MoS_2 transistor characteristics of the first-stage OPA. Output characteristic curves and transfer characteristic curves of 12 transistors. For the output characteristics, V_{gs} ranges from -2.6 V to 3.8 V in steps of 0.8 V. The transfer curve is obtained at V_{ds}=0.1 V.



Supplementary Fig. 27 | The experimental MoS_2 transistor characteristics of the second-stage OPA. Output characteristic curves and transfer characteristic curves of 12 transistors. For the output characteristics, V_{gs} ranges from -2.6 V to 3.8 V in steps of 0.8 V. The transfer curve is obtained at V_{ds}=0.1 V.



Supplementary Fig. 28 | Adjustable sensitivity of receptive fields. a, Circuit setup of the receptive fields. **b,** A high V_{th} (−0.3V) makes it hard to activate the receptive field by perceptron from M_1 or M_2. A lower V_{th} (−0.15V) can activate the receptive field by perceptron only from M_2 due to its higher conductance. Therefore, the threshold voltage simulated the sensitivity of the receptive field to external stimuli.



Supplementary Fig. 29 | Block diagram of the experimental setup for the hardware. The input signal is processed through the Synapse, Heterosynapse, and Soma modules. The NI PXI equipment controls the gate voltage for both the Synapse and Heterosynapse modules. The Keithley 2400 supplies the bias voltage to the Soma module. A controller coordinates the input signals and manages the operation of the NI PXI equipment and Keithley 2400 to ensure precise control of the system's voltage and signal processing.

Table S1 The connection encoding table of on/off status encoding for 6 MoS_2 FETs under different connection modes

	T_1	T_2	T_3	T_4	T_5	T_6
voltage follower	on	off	off	off	off	off
Voltage comparator	off	off	on/off	off/on	off	off
Integrator	off	off	off	off	on	off

Table S2 Functional circuit design of OPA

	Functions	Circuit design	Output characteristic
Inverting voltage amplifier	Convert input voltage to output voltage	Input resistance: R_M = 300 kΩ Feedback resistor: R_{ref} = 300 kΩ	Output signal: $V_{out} = -(R_{ref}/R_{ref})*V_{in}$
Voltage comparator	Compares two input voltages and generates a high/low level output	Input signal: differential voltage signal Input resistance: None Feedback resistor: None	Output signal: $V_{out} = \begin{cases} V_{high} & (V_{in} < V_{th}) \\ V_{low} & (V_{in} > V_{th}) \end{cases}$
Integrator	Integrate the input voltage into the output voltage	Input resistance: R_M = 300 kΩ Feedback capacitor: C_{ref} = 0.22 pF	Output signal: $V_{out} = -(1/RC)\int_{t0}^{t} V_{in}(t)dt+V_0$ V_0 is initial voltage
Differentiator	Differentiate the input voltage	Input capacitor: C_f = 10 nF Feedback resistor: R_{ref} = 300 kΩ	Output signal: $V_{out} = -RC(dV_{in}/dt)$
Adder	Add multiple input signals	Input signal: two voltage signal Input resistance: R_{M1} = R_{M2} = 300 kΩ Feedback resistor: R_{ref} = 300 kΩ	Output signal: $V_{out} = -R_{ref}*(V_{in}^1/R_{M1}+V_{in}^2/R_{M2})$
Subtractor	Subtract multiple input signals	Input signal: two voltage signal Input resistance: R_M = 300 kΩ Feedback resistor: R_{ref} = 300 kΩ	Output signal: $V_{out} = -R_{ref}/R_M*(V_{in}^1-V_{in}^2)$