nature portfolio

Peer Review File

2D MoS_2-based reconfigurable analog hardware

Corresponding Author: Professor Lei Ye

This file contains all reviewer reports in order by version, followed by all author rebuttals in order by version.

Version 0:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors have demonstrated neuromorphic hardware designed with MoS2 FETs to emulate the adaptability and flexibility of biological neural circuits. This hardware, referred to as neural circuit-mimicked hardware, integrates synapse, heterosynapse, and soma modules to perform a variety of computational functions, including analog-to-digital and digital-to-analog conversion, vector-matrix multiplication, and convolution. The authors also show practical applications, such as reconstructing and extracting features from medical images and enhancing visual processing for autonomous driving. This is a comprehensive manuscript worthy of publication in Nature Communications.

However, I disagree with the statement that current 2D materials-based neuromorphic hardware mainly focuses on individual devices. There are several examples where multiple MoS2 devices have been integrated for brain-like functionalities, such as those reported in Nature Communications 13 (1), 5578, 2022, and Advanced Materials, 2202535, 2022. Additionally, demonstrations integrating multiple sensor modalities based on various 2D materials for neural circuit-mimicked hardware have been presented in Nature Communications 14 (1), 6021, 2023, Nature Communications 14 (1), 5729, 2023, Advanced Materials 36 (13), 2307380, 2024, and Nano Letters 2024, 24 (23), 6948–6956, 2024. A discussion on these previous demonstrations is critical to poise the work properly.

Reviewer #2

(Remarks to the Author)
This manuscript reports on the use of MoS2 (N-channel) transistors to implement analogue circuits based on operational amplifiers. The authors convincingly display analogue circuit functionality with enough performance to implement fundamental circuit functions such as digital to analogue and analogue to digital conversion, and employ such circuits to replicate different brain functions by reconfiguring the interconnection of analogue circuit building blocks that mimic synapses, heterosynapses and soma from a biological neural system.

I found of great value in this work the high yield and low-enough variability in MoS2 transistors that enabled the authors to design and tailor custom analogue circuits to the specific desired functionalities (even though the performance of the transistors themselves is not extremely high, which I don't find to be an issue whatsoever). Aided with multiple external components, inputs and computing/external processing, the authors show the implementation of different applications in the domain of AI, such as image feature extraction or the basic principles required in receptive fields for autonomous navigation of vehicles.

However, there is a key aspect that should be clarified regarding the specific contribution and scope. Particularly, while obtaining functional circuit blocks with MoS2 FET is very challenging, the 2D material-based technology and its superior physical properties (as stated by the authors in line 85) provides no particular functionality or performance that cannot be achieved with standard, old/mature CMOS nodes even in the µm range.

Although I understand that the intended application of reconfigurable neural hardware is appealing as a case-study, using this platform provides no innovation towards that specific application, as it is suggested by the abstract and introduction of the manuscript. This is highlighted by statements such as "… we demonstrated a neural circuit-mimicked hardware whose synapse/heterosynapse/soma modules exhibited synergistically programmed inner-states and inter-connections, all achieved by the building blocks of MoS2 FETs". This is actually reconfigurable analogue hardware, which holds its own value without the need to incur into overcomplicated rephrasing.

In that sense, and from my understanding of the text, the manuscript seems to point towards a technology enabled through MoS2 devices, when the paper is reporting a test case study of reconfigurable analogue circuits based on MoS2 platforms. This makes this work a logical extension from previous literature, particularly of Polyushkin, D. K. et al. Analogue two-dimensional semiconductor electronics. Nat Electron 3, 486–491 (2020).

All in all, the overall results shown regarding analogue circuit applications with MoS2 FET for NHC could be worth of publishing in Nature Communications, but the scope of the paper should be thoroughly revised and clarified to reflect the key contributions of the paper and avoid any possible misleading. A title change and re-write of the introduction and abstract are necessary to that end.

Additionally, please consider the following list of points that, from my perspective, are worth revising.

1) The fabricated devices are back gated. However, the back-gate contact electrode was designed not to span the whole S/D contact regions, which is more typically seen in top-gated 2D FET. What is the reason behind this choice? Bottom electrodes overlapping the S/D regions generally result in increase current driving capability through modulation of the effective barrier at the contacts (depending on the metal of the S/D electrodes, but a higher carrier density in the MoS2 at the contact aids towards a more ideal ohmic contact). Please clarify the reasons behind this design choice.

2) It would be very interesting to show cross-sectional TEM and top-view SEM of the fabricated devices, to understand MoS2 layer quality, thickness/layer count and contact quality. If possible, include these, they can be of great interest to the materials community.

3) For SuppFig 3, 4, 24 and 25, providing transistor sizing (W and L or at leas aspect ratio W/L) for each device would be interesting for circuit designers to understand performance and compare/benchmark against other implementations or technologies.

4) In Fig. 1b, the heterosynapse module is preceded by a transimpedance amplifier? I'm a bit confused about the connection points in the schematic.

5) I found the description of the connectomic function in section S2 to be too general and vague. Moreover, it is not mentioned in the main text. Since it is a central point towards the reconfigurability of the hardware, I would expect a higher degree of detail in the description of this building block. Personally, I couldn't quite understand from the description which are the external signals that need to be applied to configure the hardware in each specific function.

6) In general, a block-level system description that clearly indicates the external signal sources and interconnection of blocks could help understand the complexity of the design and would be invaluable for reproducibility. Fig. 1b fails to provide a clear picture of this, from my perspective.

7) In general, synapses require some degree of long- (or at least short-term) memory. In this implementation, synapses are configured by an externally applied voltage to the gate of the synapse-mimicking transistor. This is an important drawback and is the reason why several approaches are followed in analogue neuromorphic hardware to represent this functon(floating gate transistors, charge-trapping transistors, memristors, SRAM memory cells). From my humble perspective, this should be clarified as a fundamental limitation of the proposed hardware.

8) In sparse coding (Section S7), a 256x64 memory array is mentioned. However, it is not clear how this was implemented. Is this memory array actually stored externally and later the signals are back-fed to the ADCs? Please, clarify how the whole test is diagrammed and what external instruments/processing are included in the loop.

9) In Fig. 1c, the circuit of the voltage follower in the soma module k1 picture is not correct (feedback should be inverting).

10) In Table S2, the function Inverting Amplifier is expressed as "converting input current to output voltage", but the design details suggest an inverting voltage amplifier, which is typically addressed with an input voltage (high input impedance). The I-to-V conversion, by definition, is that of a transimpedance amplifier, which is not described in Table S2.

11) BSH (mentioned for the first time in line 239) is not defined in the main text, and from context I honestly cannot tell what it represents. Maybe refers to a Bayesian ScatterNet Hybrid model adopted? If so, please, define it for clarity and state why it was chosen.

12) Please, note that in the Methods section, the subsection "Electrical measurements" is an almost exact copy of the one in Polyushkin, D. K. et al. Analogue two-dimensional semiconductor electronics. Nat Electron 3, 486–491 (2020). I find this a bit surprising, considering that there should be multiple control signals that are required for hardware configuration and synapse weight fixing in this work, according to some of the descriptions provided. Please, improve the Methods section and provide a full description of the experimental setup to perform each one of the experiments.

Version 1:

Reviewer comments:

Reviewer #1

(Remarks to the Author)
The authors have addressed my comments. I recommend the publication of this manuscript.

Reviewer #2

(Remarks to the Author)
I appreciate the efforts by the authors to reply to my concerns, correcting some specific errors, adding characterization data, and clarifying multiple aspects in the revised manuscript. The clarity of the article has much improved and I believe it is worthy of publication. However, I still humbly believe that there are still a couple of misleading sentences that can easily be avoided without hurting the contributions of the manuscript nor its impact.

1) The Authors state, in their revised version of the introduction:

“At the device level, synapse, heterosynapse, and soma modules were fabricated with MoS2 FETs (including cascaded MoS2 FETs and MoS2 FET-based operational amplifier (OPA) units32), and the electronic properties of MoS2 could precisely control their inner states. At the circuit level, the synapse, heterosynapse, and soma module wiring assembly was adjusted based on the task requirements to process the signal transmission.”

I still believe that no particular “electronic properties of MoS2” devices enable the specific “control of their inner states”, because the inner states are basically an externally set gate voltage and therefore could be replicated with any standard technology. MoS2 does not provide a particular “electronic property” to that end. Instead, I strongly suggest avoiding such phrasing.
This configuration via external gate voltages has been very well clarified by the Authors in the revised text provided in the Supplementary Note S2, so it is my humble belief that insisting on electronic properties of the MoS2 as enabler to any particular reconfiguration capabilities is misleading. The reconfiguration is the result of a transistor effect, and as such it can be obtained with a wide range of materials and technologies.

2) Related to (1), the authors mentioned in their response letter:

“In our work, we emphasize the unique advantages of using MoS_2 in creating reconfigurable circuits that can adapt to different functional demands with high efficiency. One of the key strengths of MoS_2 devices lies in their ability to reconfigure internal states and connections, enabling the design of different functional circuits using the same MoS_2 device. MoS_2 devices exhibit high tunability, making them versatile enough to fulfill the requirements for various components such as synapses, neurons, and connection modules within the same hardware architecture.”

Again, the “high tunability” is actually the ON/OFF ratio of the MoS2 FET, which can be obtained with a wide number of transistor technologies in the same (or more area-efficient) way. I believe that the platform is still valuable, but the unique role ascribed to MoS2 transistors I still cannot see and seems like an unnecessary overstretch.

3) Right at the end of the previous response in (2), the authors state:
“This adaptability reduces the need for different device structures, a challenge often faced with CMOS technology. In CMOS systems, achieving the same level of reconfigurability would require more complex hardware design.”

I’m not sure what the authors refer to when mentioning “different device structures, a challenge often faced with CMOS”. What kind of device structures are they referring to? On that note, if the authors can exemplify how a CMOS design would “require more complex hardware design”, that would be very important. As of now, by looking at the circuit architecture, I cannot see how a direct replacement of these transistors for standard CMOS could not result in (at least) the same functionality and performance.

4) Finally, in the response letter the authors mentioned regarding the volatile nature of synapses in this work:
“From the aspect of our work, using MoS_2 FETs to fabricate the prototype and present the applicability can adequately address the concept of the reconfigurability of inner-states and inter-connections in hardware design. Besides, memory components are also applicable in our proposed concept, by just replacing the MoS2 FETs with floating gate transistors, charge-trapping transistors, or memristors. The modulation strategy of gate voltages and the hardware’s inner-states and inter-connections keep the same. Therefore, this limitation is solvable.”

I agree that there are alternatives to implement the non-volatility, even specifically with 2D materials based devices, as the authors clearly stated. From my humble perspective, this should be mentioned in the text in a short statement, with references accordingly.

Migliato Marega, G. et al. A large-scale integrated vector–matrix multiplication processor based on monolayer molybdenum disulfide memories. Nat Electron 6, 991–998 (2023).

Zhu, K. et al. Hybrid 2D–CMOS microchips for memristive applications. Nature 618, 57–62 (2023).

Again, I want to clarify that this does not diminish the value of the work: the challenge of showing complex, reconfigurable analogue hardware based on MoS2 FET for mimicking neuro-synaptic functions up to the proof-of-concept neuromorphic application demonstrations is very valuable by itself. That being said, the MoS2 FET itself does not provide any particular electronic property for that purpose (as far as I can understand), so it is better to avoid such claims in such general terms. If I'm mistaken, please provide specific arguments highlighting what I'm missing, as I would find it very enriching.

One small detail: in Supp Fig. 4, if the transistors M1-M12 are those from the circuit in Supp Fig. 5 (which I'm pretty sure it is the case), please indicate it, so that the curves are also related to device sizing. If not, please include device sizing in each case.

Version 2:

Reviewer comments:

Reviewer #2

(Remarks to the Author)
I'd like to thank the authors for the positive reception of my suggestions and appreciate their efforts to clearly convey the contributions of their work, avoiding any unnecessary stretch-out of the claims.

I believe this work is valuable and is suitable for publication in Nature Communications in its current form.

Response Letter

Reviewer #1

The authors have demonstrated neuromorphic hardware designed with MoS2 FETs to emulate the adaptability and flexibility of biological neural circuits. This hardware, referred to as neural circuit-mimicked hardware, integrates synapse, heterosynapse, and soma modules to perform a variety of computational functions, including analog-to-digital and digital-to-analog conversion, vector-matrix multiplication, and convolution. The authors also show practical applications, such as reconstructing and extracting features from medical images and enhancing visual processing for autonomous driving. This is a comprehensive manuscript worthy of publication in Nature Communications.

Response: We are grateful for your comments and appreciation for our work. It is encouraging to know that you acknowledge the functionality of our MoS_2 transistor-based analog circuits and their applications in AI. We are committed to further advancing this research.

However, I disagree with the statement that current 2D materials-based neuromorphic hardware mainly focuses on individual devices. There are several examples where multiple MoS2 devices have been integrated for brain-like functionalities, such as those reported in Nature Communications 13 (1), 5578, 2022, and Advanced Materials, 2202535, 2022. Additionally, demonstrations integrating multiple sensor modalities based on various 2D materials for neural circuit-mimicked hardware have been presented in Nature Communications 14 (1), 6021, 2023, Nature Communications 14 (1), 5729, 2023, Advanced Materials 36 (13), 2307380, 2024, and Nano Letters 2024, 24 (23), 6948 − 6956, 2024. A discussion on these previous demonstrations is critical to poise the work properly.

Response: We appreciate your valuable comments. We have paid careful attention to the above works, the contents of which provide important guidance and reference for our work. We have revised our claims more clearly and cited these references in the revised manuscript, as highlighted in blue and shown below.

The revised contents in the manuscript are listed below:

(1) Page 2, lines 2-11;

Biological neural circuits demonstrate exceptional adaptability to diverse tasks by dynamically adjusting neural connections to efficiently process information. However, current 2D materials-based neuromorphic hardware mainly focuses on specific devices to individually mimic artificial synapse or heterosynapse or soma and encoding the inner neural states to realize corresponding mock object function. Recent advancements suggest that integrating multiple 2D material devices to realize brain-like functions including the inter-mutual connecting assembly engineering has become a new research

trend. In this work, we demonstrated a 2D MoS_2-based reconfigurable analog hardware that emulate synaptic, heterosynaptic, and somatic functionalities.

(2) Page 3, lines 26-37;

Neuromorphic hardware based on 2D materials respectively adopts transistors, logic gates, and memory to construct synapses, heterosynapse, and soma components, which is optimized for a specific individual function[15–17]. Recent advancements have demonstrated the integration of multiple 2D material devices and multiple sensor modalities to achieve brain-like functionalities[18-22]. However, despite these advancements, limitations remain in fully emulating the computational flexibility of brain neural circuits, especially when efficient multitasking is required in dynamic environments[23, 24]. This limitation results in resource waste in lightweight settings, specifically, excessive driving signals and device redundancy, because computational tasks of varying information content require different device quantities[25–27]. Moreover, this limited adaptability may yield suboptimal outcomes because different linear and nonlinear computational processes are required to match different tasks by circuit assembly[28–31].

References

18 Ghosh, S. et al. An all 2D bio-inspired gustatory circuit for mimicking physiology and psychology of feeding behavior. *Nat. Commun.* **14**, 6021 (2023).

19 Sadaf, M. U. K., Sakib, N. U., Pannone, A., Ravichandran, H. & Das, S. A bio-inspired visuotactile neuron for multisensory integration. *Nat. Commun.* **14**, 5729 (2023).

20 Subbulakshmi Radhakrishnan, S. et al. A Sparse and Spike-Timing-Based Adaptive Photoencoder for Augmenting Machine Vision for Spiking Neural Networks. *Adv. Mater.* **34**, e2202535 (2022).

21 Zheng, Y., Ghosh, S. & Das, S. A Butterfly-Inspired Multisensory Neuromorphic Platform for Integration of Visual and Chemical Cues. *Adv. Mater.* **36**, e2307380 (2024).

22 Zheng, Y. et al. Hardware implementation of Bayesian network based on two-dimensional memtransistors. *Nat. Commun.* **13**, 5578 (2022).

Reviewer #2

This manuscript reports on the use of MoS2 (N-channel) transistors to implement analogue circuits based on operational amplifiers. The authors convincingly display analogue circuit functionality with enough performance to implement fundamental circuit functions such as digital to analogue and analogue to digital conversion, and employ such circuits to replicate different brain functions by reconfiguring the interconnection of analogue circuit building blocks that mimic synapses, heterosynapses and soma from a biological neural system.

I found of great value in this work the high yield and low-enough variability in MoS2 transistors that enabled the authors to design and tailor custom analogue circuits to the specific desired functionalities (even though the performance of the transistors themselves is not extremely high, which I don't find to be an issue whatsoever). Aided with multiple external components, inputs and computing/external processing, the authors show the implementation of different applications in the domain of AI, such as image feature extraction or the basic principles required in receptive fields for autonomous navigation of vehicles.

Response: We appreciate your recognition of our work, and we have improved the manuscript based on your comments below.

However, there is a key aspect that should be clarified regarding the specific contribution and scope. Particularly, while obtaining functional circuit blocks with MoS2 FET is very challenging, the 2D material-based technology and its superior physical properties (as stated by the authors in line 85) provides no particular functionality or performance that cannot be achieved with standard, old/mature CMOS nodes even in the μm range.

Although I understand that the intended application of reconfigurable neural hardware is appealing as a case-study, using this platform provides no innovation towards that specific application, as it is suggested by the abstract and introduction of the manuscript. This is highlighted by statements such as "…we demonstrated a neural circuit-mimicked hardware whose synapse/heterosynapse/soma modules exhibited synergistically programmed inner-states and inter-connections, all achieved by the building blocks of MoS2 FETs". This is actually reconfigurable analogue hardware, which holds its own value without the need to incur into overcomplicated rephrasing.

In that sense, and from my understanding of the text, the manuscript seems to point towards a technology enabled through MoS2 devices, when the paper is reporting a test case study of reconfigurable analogue circuits based on MoS2 platforms. This makes this work a logical extension from previous literature, particularly of Polyushkin, D. K. et al. Analogue two-dimensional semiconductor electronics. Nat Electron 3, 486–491 (2020).

All in all, the overall results shown regarding analogue circuit applications with MoS2 FET for NHC could be worth of publishing in Nature Communications, but the scope of the paper should be thoroughly revised and clarified to reflect the key contributions of the paper and avoid any possible misleading. A title change and re-write of the introduction and abstract are necessary to that end.

Response: We sincerely thank you for the valuable suggestions, which assist to improve our manuscript. We agree that standard CMOS technology is well-established and capable of achieving many of the functionalities demonstrated in our work. In our work, we emphasize the unique advantages of using MoS_2 in creating reconfigurable circuits that can adapt to different functional demands with high efficiency. One of the key strengths of MoS_2 devices lies in their ability to reconfigure internal states and connections, enabling the design of different functional circuits using the same MoS_2 device. MoS_2 devices exhibit high tunability, making them versatile enough to fulfill the requirements for various components such as synapses, neurons, and connection modules within the same hardware architecture. This adaptability reduces the need for different device structures, a challenge often faced with CMOS technology. In CMOS systems, achieving the same level of reconfigurability would require more complex hardware design.

In addition, unlike Nat Electron 3, 486–491 (2020), which focused only on 2D material-based operational amplifiers, our work not only implements op-amps as sub-modules but also integrates multiple other functional modules. We demonstrate the reconfigurability of circuit connections and consider the internal states of neurons and their interconnections, enabling more complex computations. This significantly extends the previous work's scope and highlights different innovations, particularly in hardware-level reconfigurability and modular functionality.

Finally, based on your feedback, we have rewritten the abstract and introduction to more clearly highlight the unique contributions of this study. The title is also revised. These revisions are highlighted in blue in the revised abstract and introduction, as detailed below.

The revised contents in the manuscript are listed below:

(3) Page 1, lines 1;

2D MoS_2-based reconfigurable analog hardware

(4) Page 2, lines 1-19;

Abstract

Biological neural circuits demonstrate exceptional adaptability to diverse tasks by dynamically adjusting neural connections to efficiently process information. However, current 2D materials-based neuromorphic hardware mainly focuses on specific devices to individually mimic artificial synapse or heterosynapse or soma and encoding the inner neural states to realize corresponding mock object function. Recent advancements suggest that integrating multiple 2D material devices to realize brain-like functions

including the inter-mutual connecting assembly engineering has become a new research trend. In this work, we demonstrated a 2D MoS_2-based reconfigurable analog hardware that emulate synaptic, heterosynaptic, and somatic functionalities. The inner-states and inter-connections of all modules co-encoded versatile functions such as analog-to-digital/digital-to-analog conversion, and linear/nonlinear computations including integration, vector-matrix multiplication, convolution, to name a few. By assembling the functions to fit with different environment-interactive demanding tasks, this hardware experimentally achieved the reconstruction and image sharpening of medical images for diagnosis as well as circuit-level imitation of attention-switching and visual residual mechanisms for smart perception. This innovative hardware promotes the development of future general-purpose computing machines with high adaptability and flexibility to multiple tasks.

(5) Page 3, lines 24-50;

2D materials, which possess superior physical properties[11], can overcome the limitations of traditional silicon-based electronics and provide novel neuromorphic computing hardware[12–14]. Neuromorphic hardware based on 2D materials respectively adopts transistors, logic gates, and memory to construct synapses, heterosynapse, and soma components, which is optimized for a specific individual function[15–17]. Recent advancements have demonstrated the integration of multiple 2D material devices and multiple sensor modalities to achieve brain-like functionalities[18-22]. However, despite these advancements, limitations remain in fully emulating the computational flexibility of brain neural circuits, especially when efficient multitasking is required in dynamic environments[23, 24]. This limitation results in resource waste in lightweight settings, specifically, excessive driving signals and device redundancy, because computational tasks of varying information content require different device quantities[25–27]. Moreover, this limited adaptability may yield suboptimal outcomes because different linear and nonlinear computational processes are required to match different tasks by circuit assembly[28–31]. Therefore, the development of 2D material-based reconfigurable analog hardware is the key to truly emulate the computational flexibility of brain neural circuits for multitasking demands in dynamic environments.

In this work, motivated by biological principles, we developed an 2D MoS_2-based reconfigurable analog hardware (RAH) that included synapse, heterosynapse, and soma modules (Fig. 1b, (I)) and demonstrated its reconfigurable multiple functions and potential as a solution for general-purpose machines with rich dynamics. At the device level, synapse, heterosynapse, and soma modules were fabricated with MoS_2 FETs (including cascaded MoS_2 FETs and MoS_2 FET-based operational amplifier (OPA) units[32]), and the electronic properties of MoS_2 could precisely control their inner states. At the circuit level, the synapse, heterosynapse, and soma module wiring assembly was adjusted based on the task requirements to process the signal transmission. By co-encoding the inner-states and inter-connections of all modules, the high adaptability and plasticity of RAH allowed the realization of diverse linear and nonlinear computing

functions and effective handling of varying task requirements.

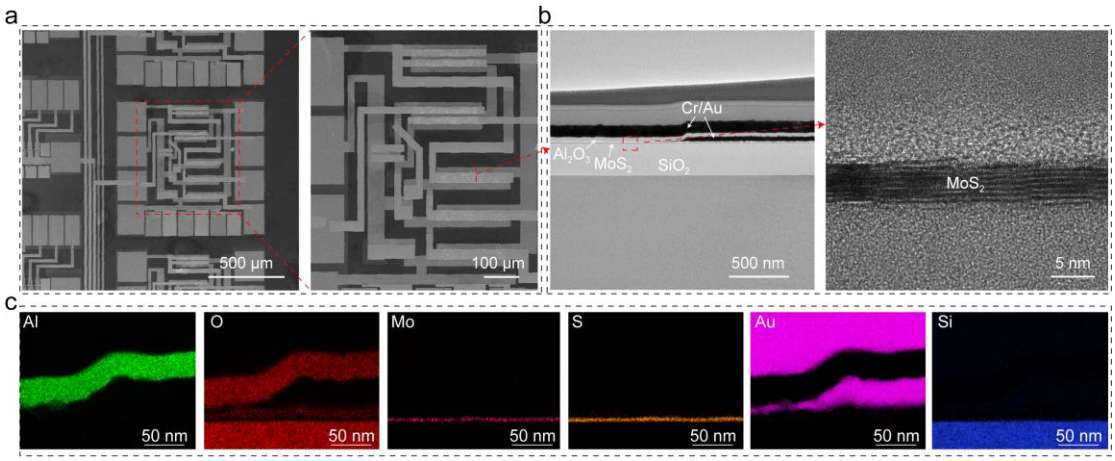
1) The fabricated devices are back gated. However, the back-gate contact electrode was designed not to span the whole S/D contact regions, which is more typically seen in top-gated 2D FET. What is the reason behind this choice? Bottom electrodes overlapping the S/D regions generally result in increase current driving capability through modulation of the effective barrier at the contacts (depending on the metal of the S/D electrodes, but a higher carrier density in the MoS2 at the contact aids towards a more ideal ohmic contact). Please clarify the reasons behind this design choice.

Response: We acknowledge your insightful comments. We apologize for any confusion caused by the schematic diagram. As detailed in the supplementary materials, our fabricated devices are top-gated. The schematic was intended to illustrate the device structure but may not have accurately depicted the gate configuration. We have corrected this in the revised manuscript.

The design choice to have the gate electrode not to span the entire source/drain (S/D) contact regions was made to reduce parasitic capacitance and optimize the electric field distribution within the device. Additionally, avoiding overlap helps prevent the occurrence of leakage currents as much as possible, leading to better control over the device's electrical characteristics.

2) It would be very interesting to show cross-sectional TEM and top-view SEM of the fabricated devices, to understand MoS2 layer quality, thickness/layer count and contact quality. If possible, include these, they can be of great interest to the materials community.

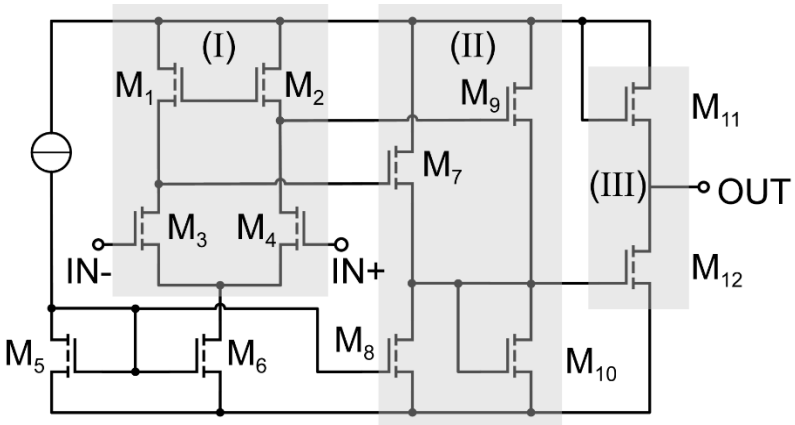
Response: We gratefully appreciate your comments. We have performed additional characterizations including the cross-sectional TEM and top-view SEM images in the revised manuscript (see Supplementary Figure 2). The TEM images reveal the high-quality crystalline structure of the MoS_2 layers and confirm the layer thickness as intended. The SEM images provide detailed views of the device morphology and the contact regions. These images confirm the uniform quality of the MoS_2 layers and contacts. The elemental mapping highlights the precise distribution of materials, further supporting the reliability of our fabrication process.



Supplementary Fig. 2 | SEM, STEM, and EDS Analysis of RAH. (a) Scanning electron microscope (SEM) images of the device, with the left panel depicting the overall structure and the right panel presenting a magnified view, respectively. **(b)** Scanning transmission electron microscope (STEM) cross-sectional images. **(c)** Energy-dispersive X-ray spectroscopy (EDS) elemental mapping, showing the distribution of Al, O, Mo, S, Au, and Si across the cross-section of device.

3) For Supp Fig 3, 4, 24 and 25, providing transistor sizing (W and L or at leas aspect ratio W/L) for each device would be interesting for circuit designers to understand performance and compare/benchmark against other implementations or technologies.

Response: Thanks for your valuable comments. We agree with the reviewer's opinion that transistor sizing helps circuit designers understand performance. Therefore, we have added the W/L ratio information in the structural schematic diagram of Supplementary Figure 5 (previously Supplementary Figure 4). Supplementary Figures 3, 24, and 25 correspond to the information in Supplementary Figure 5. The revised figure is included in the revised Supplementary Information.

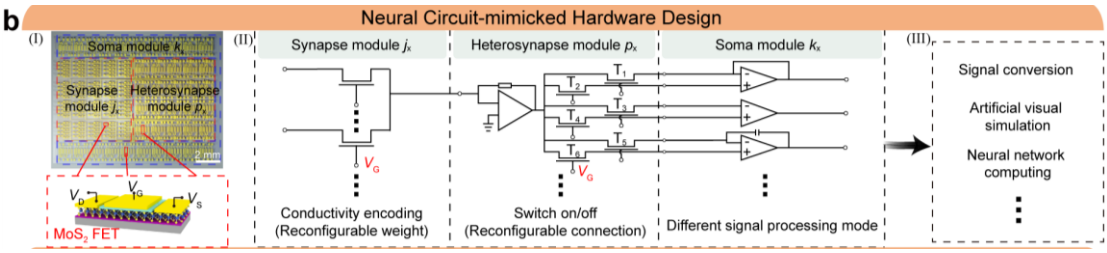


Transistors	W/L
M_1, M_2	0.5
$M_{3\text{-}6}$, M_8, M_{10}, M_{12}	40
M_7, M_9	0.25
M_{11}	6

Supplementary Fig. 5 | The circuit connection diagram of OPA. The different stages of the OPA are highlighted: (I) differential input stage, (II) main gain stage with external capacitor used for phase-compensation and (III) output stage. The right panel is the W/L information of the corresponding device.

4) In Fig. 1b, the heterosynapse module is preceded by a transimpedance amplifier? I'm a bit confused about the connection points in the schematic.

Response: We gratefully appreciate your comments. The heterosynapse module is preceded by a transimpedance amplifier. To clarify the connection points in the schematic, we have redrawn Figure 1b to better illustrate the connections between different components in the revised manuscript. In our design, the transimpedance amplifier is followed by an FET, whose on/off state is controlled by the gate voltage. This configuration determines whether the synapse at the front end is connected to the subsequent soma module based on the FET's state. This ensures dynamic control over the synaptic connections, providing reconfigurability in the circuit connections.



5) I found the description of the connectomic function in section S2 to be too general and vague. Moreover, it is not mentioned in the main text. Since it is a central point towards the reconfigurability of the hardware, I would expect a higher degree of detail in the description of this building block. Personally, I couldn't quite understand from the description which are the external signals that need to be applied to configure the hardware in each specific function.

Response: We acknowledge your insightful comments. The connectomic module function refers to the heterosynaptic module. To avoid any potential misunderstandings, we updated the terminology throughout the revised manuscript and Supplementary Information, replacing connectomic function with heterosynaptic module for consistency.

To provide a clearer description of the reconfigurability of three modules and external signal configuration, we added more details in the revised Supplementary Information, as highlighted in blue and shown below. This will help to better illustrate the critical role of the module in supporting the system's multi-tasking reconfigurability.

Page 3 in Section S2 of the revised Supplementary Information

Reconfigurable functionality is a crucial aspect of modern neuromorphic computing systems, enabling adaptability to various tasks and scenarios. Here, we detail the methodology employed to achieve reconfigurable functionality using synapse, heterosynapse, and soma modules.

Synapse module:

The reconfigurability of the synapse module is achieved by controlling external signals

to modulate the gate voltage of multiple cascade MoS_2 FETs. This modulation simulates synaptic plasticity by allowing dynamic tuning of the conductance states of cascade FETs under different gate voltages. The conductance state of each FET operates based on a customizable discrete function denoted, enabling the system to emulate various synaptic behaviors and learning rules. This capability enhances the hardware's adaptability in signal processing within the neuromorphic architecture.

Heterosynapse module:

The heterosynapse module is designed to facilitate dynamic connections between different components of the neural circuit-mimicked hardware. It comprises operational amplifiers (OPAs) and multiple MoS_2 FETs (T1–T6). The OPAs serve to isolate the influence of the heterosynapse module on the FETs within the synapse module. The reconfigurability of the heterosynapse module hinges on precise gate control of the MoS_2 FETs in different pathways, enabling the switching among distinct neural pathways. By meticulously adjusting the gate voltages of the FETs, we can selectively activate or deactivate specific connections, thereby altering the behavior of the whole hardware. This capability allows for the establishment or disruption of connections between the synapse module and the soma module. By dynamically configuring these connections, multitasking functionality is achieved, allowing the system to adapt to different tasks by facilitating the flow of information through various pathways within the neuromorphic architecture.

Soma module:

The soma module integrates signals transmitted from the front-end circuits—the synapse and heterosynapse modules—and generates a soma-like response, which serves as the output of the neural circuit. It consists of MoS_2 FET-based OPAs and feedback loops that are pivotal in signal processing. By varying the feedback circuit, we can achieve different operational states of the soma module, altering how incoming signals are processed and integrated. This allows for the execution of diverse computational functions, enhancing the system's adaptability to various computational tasks.

External signals configuring the hardware:

Gate voltage: The gate voltage is the primary external signal controlling the state of the FETs in the heterosynaptic module. By adjusting the gate voltage, each FET’s conduction state can be modulated, enabling or interrupting synaptic connections between neurons. This allows dynamic control over signal transmission within the neural network.

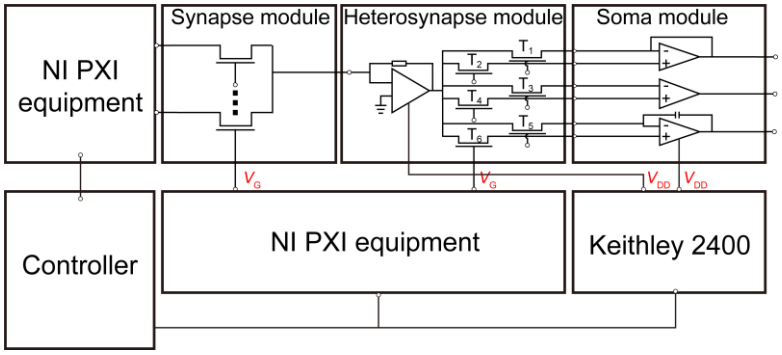
Feedback loops and paths: These gate voltages also regulate the selection of feedback loops within the system. By controlling which feedback loops are activated or deactivated, the heterosynaptic module can dynamically adjust the flow of information through the hardware, simulating various neural processing functions.

Power supply for OPA Structures: In addition to controlling the FETs, the module’s

operational amplifier (OPA) structures also require a dedicated power supply. This power supply ensures stable operation and supports the amplification and signal processing tasks within the heterosynaptic module.

6) In general, a block-level system description that clearly indicates the external signal sources and interconnection of blocks could help understand the complexity of the design and would be invaluable for reproducibility. Fig. 1b fails to provide a clear picture of this, from my perspective.

Response: Thanks for your valuable comments. To enhance the understanding of the experimental design, we have provided a more detailed schematic (Supplementary Fig. 29) in the revised Supplementary Information. The updated diagram provides clear labeling of all input/output connections, signal sources, and the path of the external signals, including the controller, NI PXI equipment, and Keithley 2400, which are used for biasing and gate voltage control. Each module (Synapse module, Heterosynapse module, and Soma module) is clearly labeled with their respective input connections, signal paths, and supply voltage sources.



Supplementary Fig. 29 | Block diagram of the experimental setup for the hardware. The input signal is processed through the Synapse, Heterosynapse, and Soma modules. The NI PXI equipment controls the gate voltage for both the Synapse and Heterosynapse modules. The Keithley 2400 supplies the bias voltage to the Soma module. A controller coordinates the input signals and manages the operation of the NI PXI equipment and Keithley 2400 to ensure precise control of the system's voltage and signal processing.

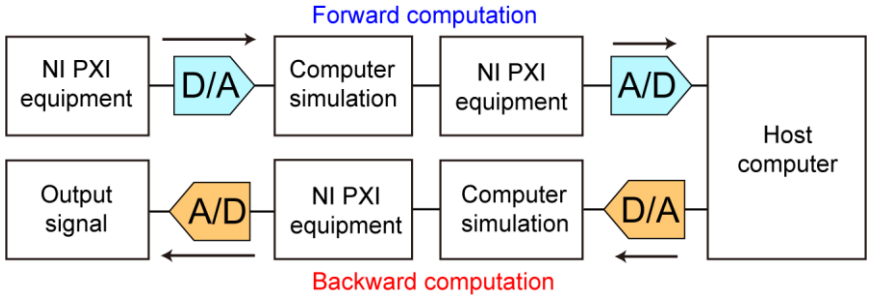
7) In general, synapses require some degree of long- (or at least short-term) memory. In this implementation, synapses are configured by an externally applied voltage to the gate of the synapse-mimicking transistor. This is an important drawback and is the reason why several approaches are followed in analogue neuromorphic hardware to represent this functon (floating gate transistors, charge-trapping transistors, memristors, SRAM memory cells). From my humble perspective, this should be clarified as a fundamental limitation of the proposed hardware.

Response: Thanks for your valuable comments. We acknowledge that integrating some

form of long-term or short-term memory is essential for practical neuromorphic systems that require learning and adaptation over time. But from the aspect of nonvolatility, this is a drawback. From the aspect of our work, using MoS_2 FETs to fabricate the prototype and present the applicability can adequately address the concept of the reconfigurability of inner-states and inter-connections in hardware design. Besides, memory components are also applicable in our proposed concept, by just replacing the MoS2 FETs with floating gate transistors, charge-trapping transistors, or memristors. The modulation strategy of gate voltages and the hardware's inner-states and inter-connections keep the same. Therefore, this limitation is solvable.

8) In sparse coding (Section S7), a 256x64 memory array is mentioned. However, it is not clear how this was implemented. Is this memory array actually stored externally and later the signals are back-fed to the ADCs? Please, clarify how the whole test is diagrammed and what external instruments/processing are included in the loop.

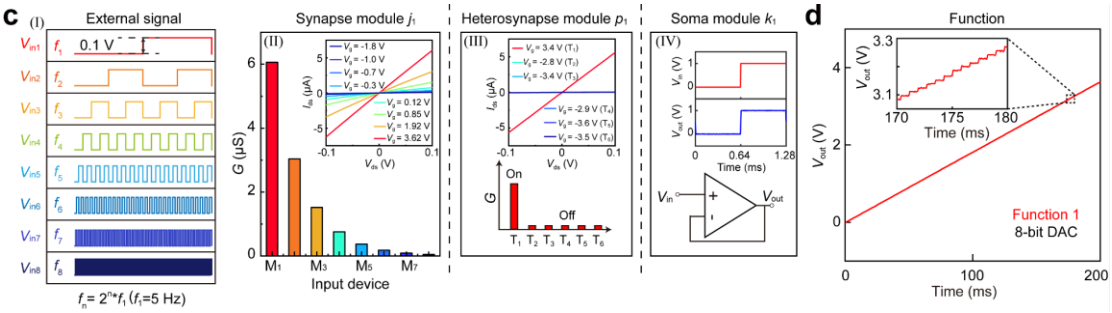
Response: We appreciate your comments. The 256×64 memory array mentioned in Section S7 was performed using external memory computations. This was connected to our hardware to realize the whole forward and backward computations in the study. Specifically, the DAC and ADC operations were completed by the devices developed in our work. In the forward process, signals are sent to the external memory after DAC conversion, and the output signals are recorded and encoded by the NI equipment before being input to the ADC. Further calculations are performed by the host computer. The backward process follows a similar path. For clarity illustrating the complete testing loop, we have provided a diagram (Supplementary Fig. 19) in the revised supplementary materials.



Supplementary Fig. 19 | Block diagram illustrating the forward and backward computation processes.

9) In Fig. 1c, the circuit of the voltage follower in the soma module k1 picture is not correct (feedback should be inverting).

Response: We gratefully appreciate your valuable comments. The feedback schematic of the voltage follower in the soma module k_1 should indeed be inverting in Fig. 1c. We have made the necessary corrections and have redrawn Fig. 1c to avoid possible misunderstanding in the revised manuscript.



10) In Table S2, the function Inverting Amplifier is expressed as "converting input current to output voltage", but the design details suggest an inverting voltage amplifier, which is typically addressed with an input voltage (high input impedance). The I-to-V conversion, by definition, is that of a transimpedance amplifier, which is not described in Table S2.

Response: We thank you for bringing this to our attention. You are right, in our design, the inverting amplifier is intended to function as an inverting voltage amplifier. To prevent any misunderstanding, we revised Table S2 in the updated supplementary information to accurately reflect the role of the inverting voltage amplifier, specifically amplifying input voltage signals. Furthermore, we ensured that the design details and descriptions throughout the manuscript are consistent with this correction.

11) BSH (mentioned for the first time in line 239) is not defined in the main text, and from context I honestly cannot tell what it represents. Maybe refers to a Bayesian ScatterNet Hybrid model adopted? If so, please, define it for clarity and state why it was chosen.

Response: We thank you for your comments. We apologize for the confusion caused by the typographical error in our manuscript. The abbreviation BSH (used in our unsubmitted version) mentioned in line 239 should be NCH, which stands for 2D MoS_2-based neural circuit-mimicked hardware. In the revised version, to ensure consistency throughout the article, we have replaced 2D MoS_2-based neural circuit-mimicked hardware (NCH) with 2D reconfigurable analog hardware (RAH), as highlighted in blue and shown below. Thank you for your careful review and valuable feedback.

The revised contents in the manuscript are listed below:

Page 6, lines 239

Thus, RAH can provide robust support for future medical research and clinical applications. Additionally, image reconstruction with additional noise was implemented using RAH (Figs. S21 and S22). The peak signal-to-noise ratios of the noisy and reconstructed images are 20.1026 and 27.1774 dB, respectively, in Fig. S23a (20.2940 and 28.5906 dB in Fig. S23b), confirming the high-quality reconstruction under additional noise.

12) Please, note that in the Methods section, the subsection "Electrical measurements" is an almost exact copy of the one in Polyushkin, D. K. et al. Analogue two-dimensional semiconductor electronics. Nat Electron 3, 486–491 (2020). I find this a bit surprising, considering that there should be multiple control signals that are required for hardware configuration and synapse weight fixing in this work, according to some of the descriptions provided. Please, improve the Methods section and provide a full description of the experimental setup to perform each one of the experiments.

Response: Thank you for pointing out this shortcoming of our manuscript and for your valuable comments. To provide a comprehensive description of our experiments, we have supplemented this section in the revised manuscript by describing the setup for each experiment, as highlighted in blue and shown below.

The revised contents in the manuscript are listed below:

Page 8-9, lines 49-50

Electrical measurements.

MoS_2 FETs: The electrical characteristics of the MoS_2 FETs are measured in a cryogenic probe station at room temperature. The Agilent B1500 source measurement unit (SMU) was used to apply gate and drain voltages and to measure the drain current as a function of gate voltage and drain voltage. The testing evaluates key parameters such as transfer and output characteristics and threshold voltage. For the MoS_2 FET-based operational amplifier (OPA) circuits, the measurements of individual FET were performed using a B1500 semiconductor analyzer in conjunction with a cryogenic probe station. For integrated device measurements, bias voltages were supplied by the B1500 semiconductor analyzer and source meter. Input and output signals were generated and measured using an Agilent 33220A function generator and a Keysight Infiniivision oscilloscope, respectively. This setup ensures precise control of the device conditions and accurate characterization of the amplifier's performance.

For the digital-to-analog conversion (DAC) functionality testing, encoded digital signals (square waves with varying frequencies) are applied across multiple input channels. The conductance values of these channels are programmed by the NI PXI equipment according to the required formula. The output analog signals are then measured using a Keysight Infiniivision oscilloscope to verify the accuracy of the digital-to-analog conversion. For analog-to-digital conversion (ADC) functionality testing, an Agilent 33220A function generator provides an analog signal to one input of the operational amplifier, while reference conductance channels receive periodic square waves. The analog signal is compared to the reference voltages, and the digital output is monitored with a Keysight Infiniivision oscilloscope.

For Convolutional Kernel testing, a convolution kernel was programmed by adjusting the conductance values of the transistors using an external controller (NI PXI system). The central FET is set to a conductance of $9 \times G_0$, while the surrounding FETs are set to G_0. The resulting output was recorded using a Keysight oscilloscope. The

convolution process is applied to extract key features from the reconstructed image, enabling image sharpening and enhancing the clarity of important details.

Response Letter

Reviewer #1

The authors have addressed my comments. I recommend the publication of this manuscript.

Response: We are grateful for your comments and appreciation for our work.

Reviewer #2

I appreciate the efforts by the authors to reply to my concerns, correcting some specific errors, adding characterization data, and clarifying multiple aspects in the revised manuscript. The clarity of the article has much improved and I believe it is worthy of publication. However, I still humbly believe that there are still a couple of misleading sentences that can easily be avoided without hurting the contributions of the manuscript nor its impact.

Response: We appreciate your valuable comments.

1) The Authors state, in their revised version of the introduction:"At the device level, synapse, heterosynapse, and soma modules were fabricated with MoS2 FETs (including cascaded MoS2 FETs and MoS2 FET-based operational amplifier (OPA) units32), and the electronic properties of MoS2 could precisely control their inner states. At the circuit level, the synapse, heterosynapse, and soma module wiring assembly was adjusted based on the task requirements to process the signal transmission."

I still believe that no particular "electronic properties of MoS2" devices enable the specific "control of their inner states", because the inner states are basically an externally set gate voltage and therefore could be replicated with any standard technology. MoS2 does not provide a particular "electronic property" to that end. Instead, I strongly suggest avoiding such phrasing.

This configuration via external gate voltages has been very well clarified by the Authors in the revised text provided in the Supplementary Note S2, so it is my humble belief that insisting on electronic properties of the MoS2 as enabler to any particular reconfiguration capabilities is misleading. The reconfiguration is the result of a transistor effect, and as such it can be obtained with a wide range of materials and technologies.

Response: We sincerely thank you for the valuable suggestions. We agree with your assessment on the control of the inner states. To avoid any misunderstanding, we revised the introduction to clarify this point and prevent any misleading statements about the role of MoS_2 in the revised manuscript, as highlighted in blue and shown below. We appreciate your insightful comments, which have helped us improve the clarity of our manuscript.

The revised contents in the manuscript are listed below:

Page 3, lines 24-25:

2D materials, which possess superior physical properties[11], can support novel neuromorphic computing hardware[12–14].

Page 3, lines 40-48:

In this work, motivated by biological principles, we developed an 2D MoS_2-based reconfigurable analog hardware (RAH) that included synapse, heterosynapse, and soma modules (Fig. 1b, (I)) and demonstrated its reconfigurable multiple functions and potential as a solution for general-purpose machines with rich dynamics. At the device level, synapse, heterosynapse, and soma modules were fabricated with MoS_2 FETs (including cascaded MoS_2 FETs and MoS_2 FET-based operational amplifier (OPA) units[32]). At the circuit level, the synapse, heterosynapse, and soma module wiring assembly was adjusted based on the task requirements to process the signal transmission.

2) Related to (1), the authors mentioned in their response letter:

In our work, we emphasize the unique advantages of using MoS_2 in creating reconfigurable circuits that can adapt to different functional demands with high efficiency. One of the key strengths of MoS_2 devices lies in their ability to reconfigure internal states and connections, enabling the design of different functional circuits using the same MoS_2 device. MoS_2 devices exhibit high tunability, making them versatile enough to fulfill the requirements for various components such as synapses, neurons, and connection modules within the same hardware architecture."

Again, the "high tunability" is actually the ON/OFF ratio of the MoS2 FET, which can be obtained with a wide number of transistor technologies in the same (or more area-efficient) way. I believe that the platform is still valuable, but the unique role ascribed to MoS2 transistors I still cannot see and seems like an unnecessary overstretch.

Response: We gratefully appreciate your valuable comments and agree with the assessment on the "high tunability" issue. Our intention was to highlight MoS_2 as an effective material choice for reconfigurable neuromorphic circuit designs rather than to suggest it as the only viable or superior option for achieving reconfigurability. We appreciate your constructive comments, and we have revised the manuscript to avoid the unnecessary overstretch.

3) Right at the end of the previous response in (2), the authors state:"This adaptability reduces the need for different device structures, a challenge often faced with CMOS technology. In CMOS systems, achieving the same level of reconfigurability would require more complex hardware design."

I'm not sure what the authors refer to when mentioning "different device structures, a

challenge often faced with CMOS". What kind of device structures are they referring to? On that note, if the authors can exemplify how a CMOS design would "require more complex hardware design", that would be very important. As of now, by looking at the circuit architecture, I cannot see how a direct replacement of these transistors for standard CMOS could not result in (at least) the same functionality and performance.

Response: Thank you for your insightful comments. We sincerely apologize for any confusion our previous statements may have caused. We believe that standard CMOS technology can achieve similar functionalities in this work. Additionally, our previous statement was intended to highlight that 2D materials like MoS_2 can enable an "all-in-one" approach with the same device structure, which aids hardware design [1-3]. For example, the same MoS_2-based device design can achieve multiple functional modules, such as photodetectors, memristors, logic circuits, and flexible electronic devices, which often face challenges in functionality integration within CMOS. However, this argument is not directly relevant to the content of this paper. To avoid this misunderstanding, we have revised our previous response. We sincerely appreciate your constructive feedback, which has helped us improve the clarity of the paper.

References

1. Dodda, A. et al. All-in-one, bio-inspired, and low-power crypto engines for near-sensor security based on two-dimensional memtransistors. *Nat. Commun.* **13**, 3587 (2022).
2. Subbulakshmi Radhakrishnan, S. et al. A biomimetic neural encoder for spiking neural network. *Nat. Commun.* **12**, 2143 (2021).
3. Feixia Tan et al. Multifunctional broadband artificial visual system using all-in-one two-dimensional optoelectronic transistors. *Materials Today* (2024).

4) Finally, in the response letter the authors mentioned regarding the volatile nature of synapses in this work:

"From the aspect of our work, using MoS_2 FETs to fabricate the prototype and present the applicability can adequately address the concept of the reconfigurability of inner-states and inter-connections in hardware design. Besides, memory components are also applicable in our proposed concept, by just replacing the MoS2 FETs with floating gate transistors, charge-trapping transistors, or memristors. The modulation strategy of gate voltages and the hardware's inner-states and inter-connections keep the same. Therefore, this limitation is solvable."

I agree that there are alternatives to implement the non-volatility, even specifically with 2D materials based devices, as the authors clearly stated. From my humble perspective, this should be mentioned in the text in a short statement, with references accordingly.

Migliato Marega, G. et al. A large-scale integrated vector–matrix multiplication processor based on monolayer molybdenum disulfide memories. Nat Electron 6, 991–

998 (2023).

Zhu, K. et al. Hybrid 2D–CMOS microchips for memristive applications. Nature 618, 57–62 (2023).

Again, I want to clarify that this does not diminish the value of the work: the challenge of showing complex, reconfigurable analogue hardware based on MoS2 FET for mimicking neuro-synaptic functions up to the proof-of-concept neuromorphic application demonstrations is very valuable by itself. That being said, the MoS2 FET itself does not provide any particular electronic property for that purpose (as far as I can understand), so it is better to avoid such claims in such general terms. If I'm mistaken, please provide specific arguments highlighting what I'm missing, as I would find it very enriching.

One small detail: in Supp Fig. 4, if the transistors M1-M12 are those from the circuit in Supp Fig. 5 (which I'm pretty sure it is the case), please indicate it, so that the curves are also related to device sizing. If not, please include device sizing in each case.

Response: We sincerely thank you for your thoughtful and constructive comments. We have included a statement in the revised manuscript acknowledging these alternatives and citing the relevant literature to inform readers about potential pathways to implement non-volatile synaptic functionalities in 2D material-based devices, as highlighted in blue and shown below.

We appreciate your understanding of the value of our work, and we agree with your comment. Our work mainly shows that building neural circuit-mimicked hardware is considerable to promote neuromorphic applications, proved by a MoS_2 FET-based hardware prototype. The uniqueness of MoS_2 is not our purpose, on the contrary, we are confident that this concept is also applicable to CMOS and other emerging new materials beyond MoS_2. To avoid pervertible claims, we have revised the manuscript to accurately reflect our perspective and avoid implying that MoS_2 FETs have exclusive electronic properties in neuromorphic applications.

We confirm that transistors M1 – M12 in Supplementary Figure 4 correspond to those in the circuit shown in Supplementary Figure 5. We have updated the figure captions to indicate this connection clearly. The revised figure is included in the revised Supplementary Information.

Page 8, lines 21-25

Notably, the MoS_2 FETs used in this work could be replaced with floating gate transistors, charge-trapping transistors, or memristors to achieve a non-volatile hardware structure and reducing reliance on gate control strategies[48, 49].

References

48. Migliato Marega, G. et al. A large-scale integrated vector–matrix multiplication processor based on monolayer molybdenum disulfide memories. *Nat. Electron.* **6**, 991–998 (2023).

49. Zhu, K. et al. Hybrid 2D–CMOS microchips for memristive applications. *Nature*

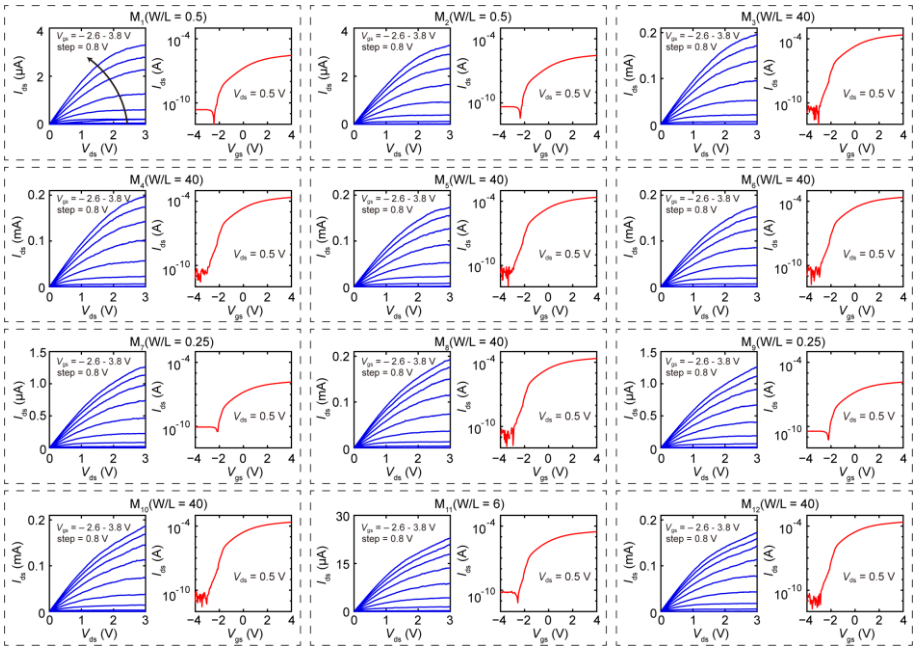
618, 57–62 (2023)

Page 3, lines 24-25:

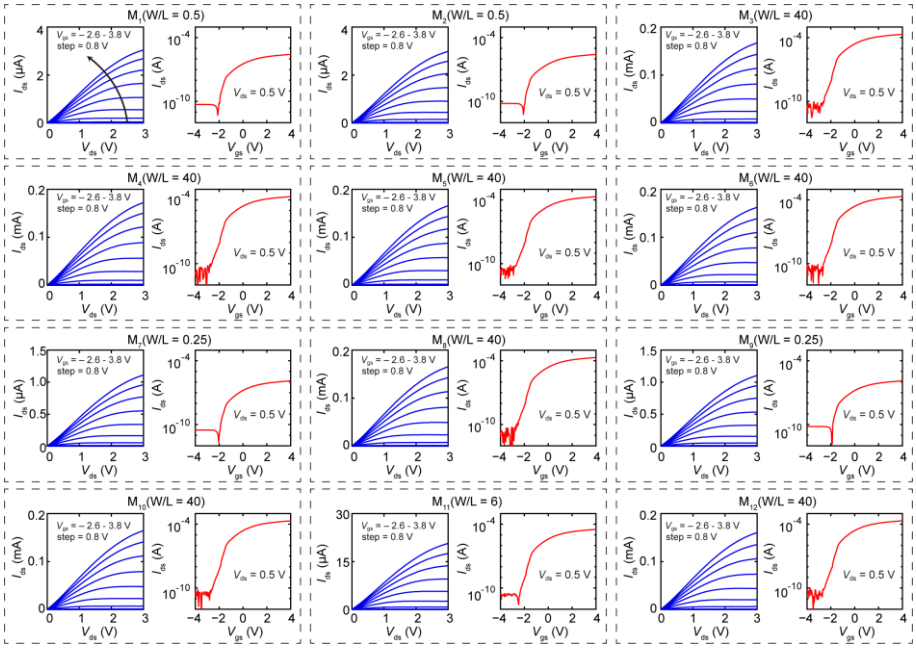
2D materials, which possess superior physical properties[11], can support novel neuromorphic computing hardware[12–14].

Page 3, lines 40-48:

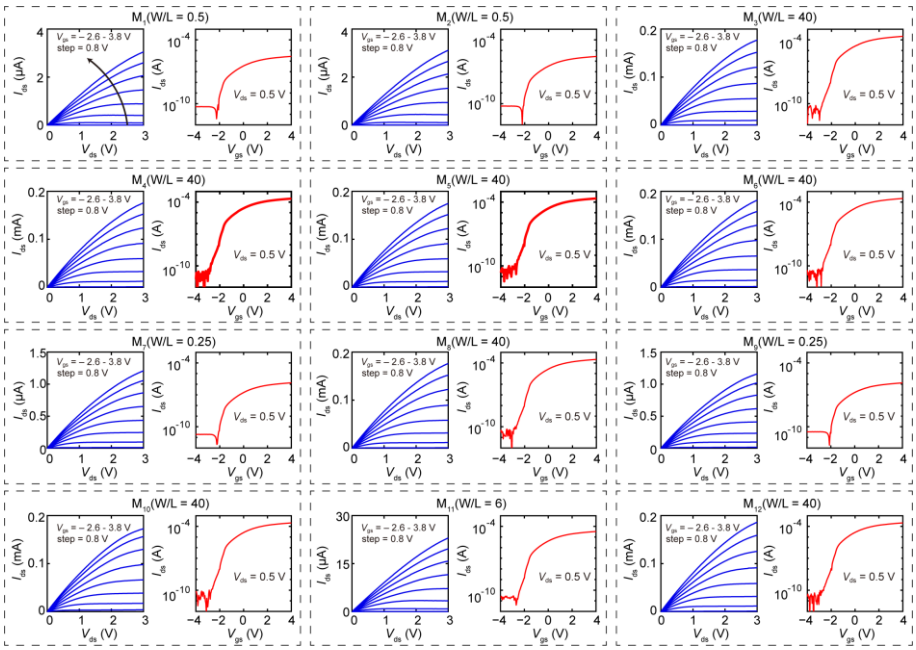
In this work, motivated by biological principles, we developed an 2D MoS_2-based reconfigurable analog hardware (RAH) that included synapse, heterosynapse, and soma modules (Fig. 1b, (I)) and demonstrated its reconfigurable multiple functions and potential as a solution for general-purpose machines with rich dynamics. At the device level, synapse, heterosynapse, and soma modules were fabricated with MoS2 FETs (including cascaded MoS_2 FETs and MoS_2 FET-based operational amplifier (OPA) units[32]). At the circuit level, the synapse, heterosynapse, and soma module wiring assembly was adjusted based on the task requirements to process the signal transmission.



Supplementary Fig. 4 | The experimental MoS_2 transistor characteristics of OPA. Output characteristic curves and transfer characteristic curves of 12 transistors. For the output characteristics, V_{gs} ranges from -2.6 V to 3.8 V in steps of 0.8 V. The transfer curve is obtained at V_{ds}=0.5 V.



Supplementary Fig. 26 | The experimental MoS_2 transistor characteristics of the first-stage OPA. Output characteristic curves and transfer characteristic curves of 12 transistors. For the output characteristics, V_{gs} ranges from -2.6 V to 3.8 V in steps of 0.8 V. The transfer curve is obtained at V_{ds}=0.1 V.



Supplementary Fig. 27 | The experimental MoS_2 transistor characteristics of the second-stage OPA. Output characteristic curves and transfer characteristic curves of 12 transistors. For the output characteristics, V_{gs} ranges from -2.6 V to 3.8 V in steps of 0.8 V. The transfer curve is obtained at V_{ds}=0.1 V.

Response Letter

Reviewer #2

I'd like to thank the authors for the positive reception of my suggestions and appreciate their efforts to clearly convey the contributions of their work, avoiding any unnecessary stretch-out of the claims.

I believe this work is valuable and is suitable for publication in Nature Communications in its current form.

Response: We are grateful for your comments and appreciation for our work.