Supporting Information

Fan *et al*. 10.1073/pnas.0801994105

SI Text

Polarization-Dependent Photoconduction. Because of the 1D feature of semiconductor nanowires, they demonstrate unique polarized photoconduction properties as reported for single NW devices (1). In this work, polarization-dependent photoconduction was measured for contact-printed (highly aligned) and drop-casted (random orientation) CdSe nanowires in both single NW and parallel array configurations. A randomly polarized 10 mW He-Ne ($\lambda = 633$ nm) laser was used as the light source in conjunction with a linear polarizer. By rotating the polarizer, the polarization angle of the incident light was tuned from 0 to 180° with respect to the edge of the source/drain electrodes. Supporting information (SI) Fig. S2 *A* and *B* shows the polarized photoconduction of single CdSe NW devices made by contact printing and drop casting of NWs, respectively. Although the contact-printed NW devices exhibit near-identical response with the photocurrent minimum at 90° and maxima at 0 and 180° polarization (angle in respect to the normal of S/D electrodes), the drop-casted (random orientation) NW devices exhibit a nonuniform response with a large device-to-device variation in their minima and maxima polarization angles. This result illustrates the highly oriented nanowire assembly achieved by the contact-printing process, in clear contrast to the random alignment obtained from drop casting of nanowires on substrates. Furthermore, polarized photoconduction measurements were conducted on parallel arrays of nanowires assembled by contact printing. As shown in Fig. S2*C*, the devices exhibit a minimum photocurrent at 90° and maxima at 0 and 180°, once again illustrating the high degree of alignment attained by the contact printing process.

Electrical Characterization of Ge/Si NW FETs. Low- and high-bias transfer characteristics of a single Ge/Si NW FET (top gated, 8–9 nm HfO_2 gate dielectric, $d \approx 30$ nm, $L \approx 3$ μm) is shown in Fig. S3 *A* and *B* for backward and forward gate voltage-sweeping directions. The transistors exhibit minimal hysteresis. From the transfer characteristics, the field-effect mobility of holes was obtained by using the square law model. The gate capacitance, $C = 3.2 \times 10^{-15}$ F, was obtained from simulation by using version 4.0.1 of Finite Element Method Magnetics software. In the low-bias linear-triode region (i.e., $V_{DS} = 10$ mV) the hole mobility, μ_h can be deduced from

$$\mu_h = \frac{g_m L^2}{V_{DS} C},$$

where g_m is the transconductance, $g_m = dI/dV_{GS}|_{V_{DS}}$. A plot of mobility as a function of gate voltage is shown in Fig. S3*D*, illustrating a peak mobility of $\approx$100 cm^2/V·s for this device. The mobility range for the studied NW devices was 30–120 cm^2/V·s with a peak transconductance range (normalized by diameter) of 100–400 S/m. In the future, key transistor metrics, such as transconductance, can be improved by downscaling of the channel length and gate dielectric thickness (2–4).

SPICE Modeling. After single-device component measurements, Pspice (OrCAD Version 9.1) modeling was carried out to simulate the circuit output performance (Fig. S5). The simulation used the previously mentioned values (in the text) for resistance of NS and T1. For T2, PMOS model 1 was used with $K_p = 1.235 \times 10^{-4}$ F·cm^{-2}·(V·s)$^{-1}$ and $V_T = 1.13$ V. The simulation output is shown in Fig. S5*B*. Interestingly, the simulation results match well with the experimental data.

Sensor Circuitry with Parallel Arrays of CdSe NWs. To improve the uniformity, parallel arrays of CdSe NWs (5–10 NWs) were printed as light sensor elements for the large matrix fabrication as shown in Fig. S6*A*. Fig. S6*B* represents the time domain photoresponse of the CdSe NWs, demonstrating $\approx$100 pA dark current and $\approx$8 nA photocurrent with an illumination intensity of 4.4 mW/cm^2 and $V_{DS} = 3$V. The output current of the circuit is shown in Fig. S6*C*, showing $\approx$5 orders of magnitude current amplification by the all-NW circuitry.

Image Construction with Sensor Circuit Array. To demonstrate the image-sensing function with the nanowire circuit array, a halogen light spot (diameter: $\approx$6 mm, peak intensity at the center: $\approx$4 mW/cm^2) from a microscope on the probe station was projected at the center of the circuit array and the current output (I_{out}) from each circuit was measured pixel by pixel.

The measured current from each circuit pixel was digitized to an integer (Z) between 0 and 100 according the following equation:

$$Z = \text{Integer}\left(100 \times \frac{I_{out} - I_{min}}{I_{max} - I_{min}}\right)$$

where I_{max} and I_{min} correspond to the light current at 4 mW/cm^2 illumination and the dark current, respectively, which were measured for each circuit during a calibration step before the image-sensing experiment. Eventually, a 13×20 intensity matrix was formed from the Z values with each circuit corresponding to a single pixel (Fig. 4*D*).

1. Wang J, Gudiksen MS, Duan X, Cui Y, Lieber CM (2001) Highly polarized photoluminescence and photodetection from single indium phosphide nanowires. *Science* 293:1455–1457.
2. Xiang J, *et al.* (2006) Ge/Si nanowire heterostructures on high-performance field-effect transistors. *Nature* 441:489–493.
3. Hu Y, Xiang J, Liang G, Yan H, Lieber CM (2008) Sub-100 nanometer channel length Ge/Si nanowire transistors with potential for 2 THz switching speed. *Nano Lett* 8:925–930.
4. Javey A, *et al.* (2002) High-k dielectrics for advanced carbon nanotube transistors and logic. *Nat Mater* 1:241–246.

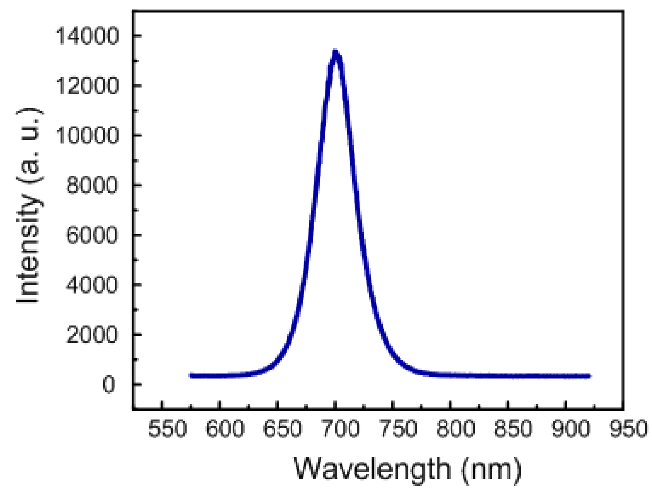

Fig. S1. A representative photoluminescence of a single CdSe NW ($d \approx 60$ nm), excited with a 1-mW green laser (532 nm) at room temperature. The extracted band gap is ≈1.76 eV (peak intensity ≈704 nm) which is consistent with the reported bulk value.

Fig. S2. Polarization-dependent photoconduction measurement for five single CdSe nanowires assembled by contact printing (*A*), five randomly orientated single CdSe nanowires assembled by drop casting (*B*), and parallel arrays of aligned CdSe NWs (≈40 NW) assembled by contact printing (*C*). (*Insets*) Optical images of representative devices. The curves in *A* and *B* have been shifted by units of 1 in the normalized photocurrent axis for clarity.

Fig. S3. Electrical characterization of a single Ge/Si NW FET. (*A* and *B*) Double-sweep transfer characteristics with $V_{DS} = -10$ mV and -1 V, respectively. (*C*) Output characteristics. (*D*) Extracted filed-effect mobility as a function of top gate voltage obtained from $V_{DS} = 10$ mV (low-bias regime).

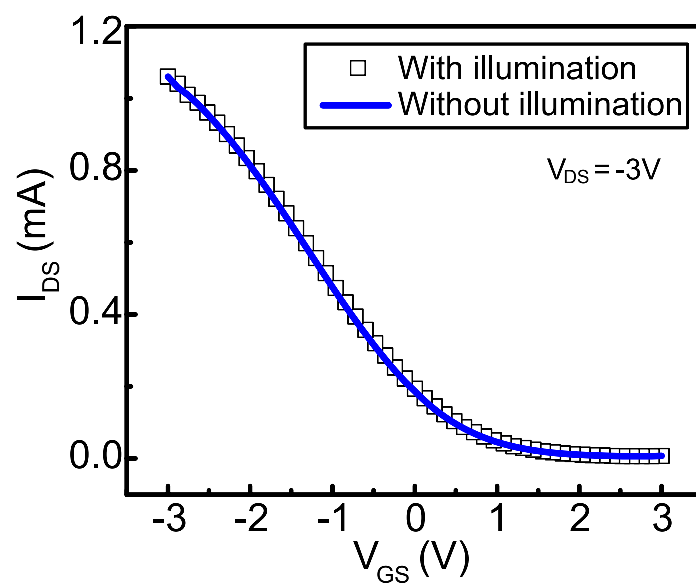

Fig. S4. Transfer characteristics of a parallel array Ge/Si nanowire transistor T2 obtained with and without illumination (4 mW/cm^2). It can be clearly seen that Ge/Si nanowire FETs do not respond to the visible light, which confirms that the photoresponse of the circuits originates from CdSe NS elements.

Fig. S5. PSpice modeling for curcuit level performance evaluation. (*A*) Equivalent circuit used for PSpice modeling. (*B*) Modeled output current versus CdSe NW sensor resistance.

Fig. S6. SEM image of a parallel array CdSe NW device used for light sensing of the image sensor array (*A*) (Fig. 4), and its time domain photoresponse (*B*). (*C*) Output current (blue curve) and voltage divider output voltage (green curve) dynamic response to visible light illumination.