Supporting Information

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SI Text

Additional Dielectric Properties. Fig. S1*A* shows the AFM of a 22-nm PVP-HDA film. Transfer characteristics (I_{DS} vs. V_G) hysteresis with the organic semiconductor DDFTTF are shown in Fig. S1*B*. The capacitance vs. frequency for 22-nm PVP-HDA films is shown in Fig. S1*C* for various top electrode areas of the sandwich electrode structure. Fig. S1*D* shows the capacitance versus inverse thickness (PVP-HDA) equivalent to Fig. 1*C* from which the dielectric constant was determined. Equivalent information for the PVP-SC dielectric layer is shown in Fig. S1 *E* and *F*, respectively.

Fig. S2 shows the hysteresis of an OTFT with a DDFTTF semiconductor layer with a 22-nm PVP-HDA film. The forward and reverse I_{DS}–V_G measurements are offset by an order of magnitude for clarity. The time value given in the caption refers to the sweep delay between each V_G measurement point.

Additional OTFT Characteristics. Fig. S3 shows additional output and transfer characteristics for vacuum-deposited FCuPc (*A* and *B*), and solution-deposited 4TTMS (*C* and *D*) and CH4T (*E* and *F*).

OTS Treatment of Dielectric Surface. PVP-HDA substrates were placed in a glass dessicator with 50 μl of octadecyltriethoxysilane (OTS), evacuated to 30 mTorr, and heated to 100°C for 48 h. The substrates were cured at 100°C for 10 min and then rinsed with toluene, acetone, and ethanol. An increase in thickness of 2 nm was observed by using ellipsometry.

OTFTs on Flexible Substrates. Flexible OTFTs were demonstrated on aluminum foil (Reynolds) substrates, which also served as the gate electrodes, with an 80-nm PVP-HDA. A slight decrease in the source-drain current was observed when the substrate was rolled around a 3.5-mm-radius glass rod, as shown in Fig. S4 *Left*, with the channel direction oriented parallel to the bending direction. Fig. S4 *Right* shows the transfer characteristics at the different bending radii with an *Inset* of output characteristics measured after the bending sequence.

Additional OTFT Characteristics Under Aqueous Conditions. The thickness of the DDFTTF semiconductor layer could be reduced to as thin as 25 nm, retaining stable transistor operation and adequate performance. For 10-nm DDFTTF film, however, we still observed a clear field-effect, but the performance was insufficient for sensor use. Fig. S5 shows the output characteristics of a 10-nm DDFTTF semiconductor layer on 22-nm PVP-HDA after device fabrication (*A*) and under aqueous conditions (*B*).

OTFTs fabricated with pentacene, FCuPc, CuPc, and CH4T were tested in static aqueous conditions. Immediately after the addition of water, the OTFTs with pentacene active layers showed adequate semiconductor characteristics, which rapidly degraded within minutes, as shown in Fig. S6. Surprisingly, we observed a field-effect with the n-channel material, FCuPc, but with a very low on/off ratio of <2. Solution-processed OTFTs of 4TTMS and CH4T also functioned under aqueous conditions; however, long-term stability is limited by a gradual delamination of the crystalline film while undergoing V_G cycles (0.3–1 V). Fig. S7 shows the output characteristics of CuPc, FCuPc, and 4TTMS before and after immersion in water. The effect of bias under aqueous conditions on the film morphology is shown in Fig. S8 for pentacene, FCuPc, and 4TTMS.

Fig. S9 below shows the first and final V_G cycles to emphasize the stability shown in Fig. 3*F*. Although there is a slight increase in the current in the on and off state, the characteristics are nearly identical. The cycle tests were performed on a freshly prepared sample. Before the electrical measurements, the PDMS flow cell was laminated on the OTFT surface and water was cycled through the cell. After setting the flow and ensuring that the system was leak-proof, the electrical cycles were initiated. Although a fresh sample was used, there was sufficient time before the measurement for water to saturate the channel.

Additional Sensing Information: Sensor Measurements. A poly(dimethylsiloxane) (PDMS) block (3 cm × 1 cm × 8 mm) with a flow channel (2 cm × 4 mm × 500 μm) and 1-mm vertical ports was laminated on the surface of a top-contact OTFT with the transistor channel region aligned perpendicular to the flow direction in the flow channel. An aluminum substrate holder was used to secure the PDMS block to the OTFT substrate. The solution flow was driven by a peristaltic pump (VWR Scientific variable-flow pump) equipped with a manual flow switch for solution exchanges with a rate of ≈1 ml/min. The measurement series for each analyte was performed on a freshly prepared sample. Between measurements (analyte concentrations), the device was refreshed with a reverse bias of 1 V for 30 s under a flow of water.

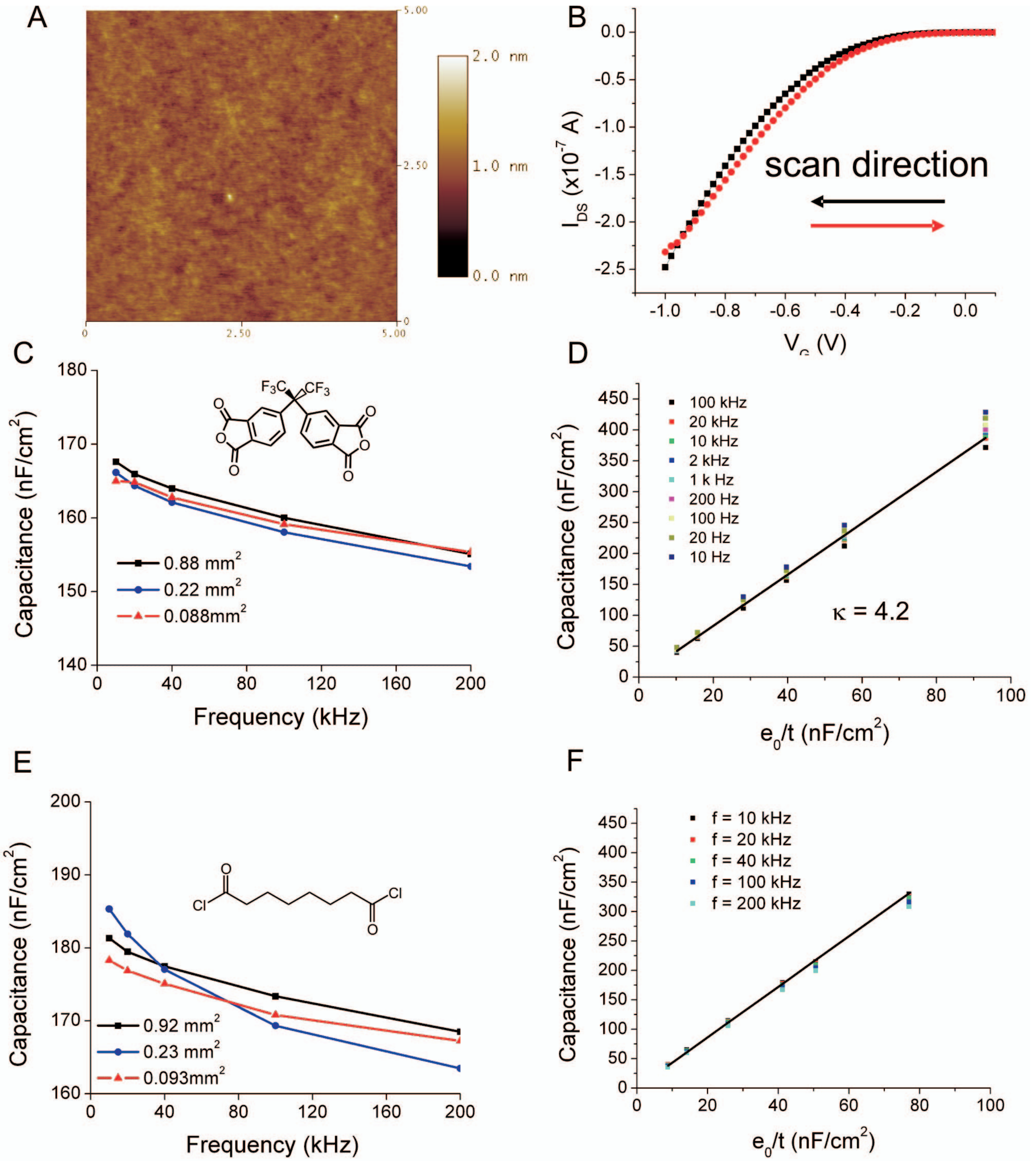

Fig. S1. Characterization data of dielectric layer. (*A*) Atomic force microscopy (AFM) for 22-nm PVP-HDA dielectric layer with an RMS of 0.2 nm. (*B*) Drain current vs. gate voltage for an OTFT with 40-nm DDFTTF and 22-nm PVP-HDA with positive-to-negative and negative-to-positive gate voltage sweeps showing little hysteresis. (*C*) Capacitance vs. frequency for 22-nm PVP-HDA films with electrode pad sizes of 0.88, 0.22, and 0.088 mm^2. (*D*) Capacitance vs. inverse thickness at various multiple measurement frequencies for PVP-HDA films. (*E*) Capacitance vs. frequency for 21-nm PVP-SC films with electrode pad sizes of 0.92, 0.23, and 0.093 mm^2. (*F*) Capacitance vs. inverse thickness at various multiple measurement frequencies for PVP-SC films.

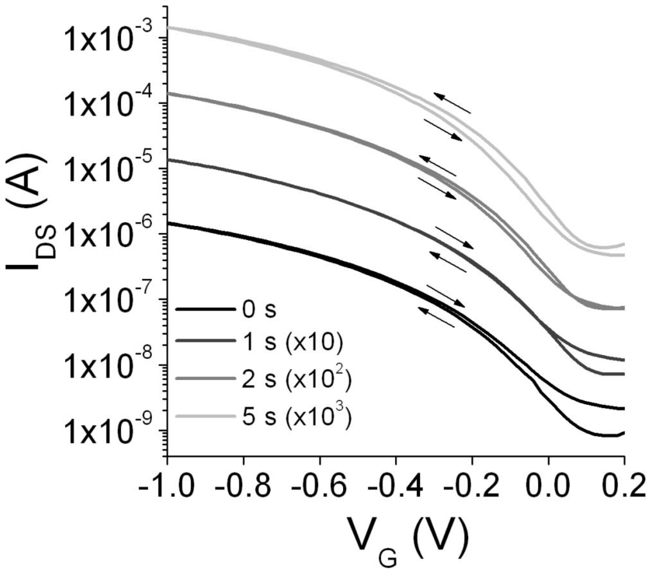

Fig. S2. Transfer characteristics hysteresis at different sweep hold time. Each measurement consists of 122 data points for the forward and reverse scan. With a sweep hold time of zero (0 s), the measurement takes 27 s with the appropriate sensitivity settings. The numerical value in the key is the gate bias sweep delay (the time the measurement is held at each given voltage) for each voltage in the measurement. For clarity, the curves are offset by an order of magnitude, as indicated in the key.

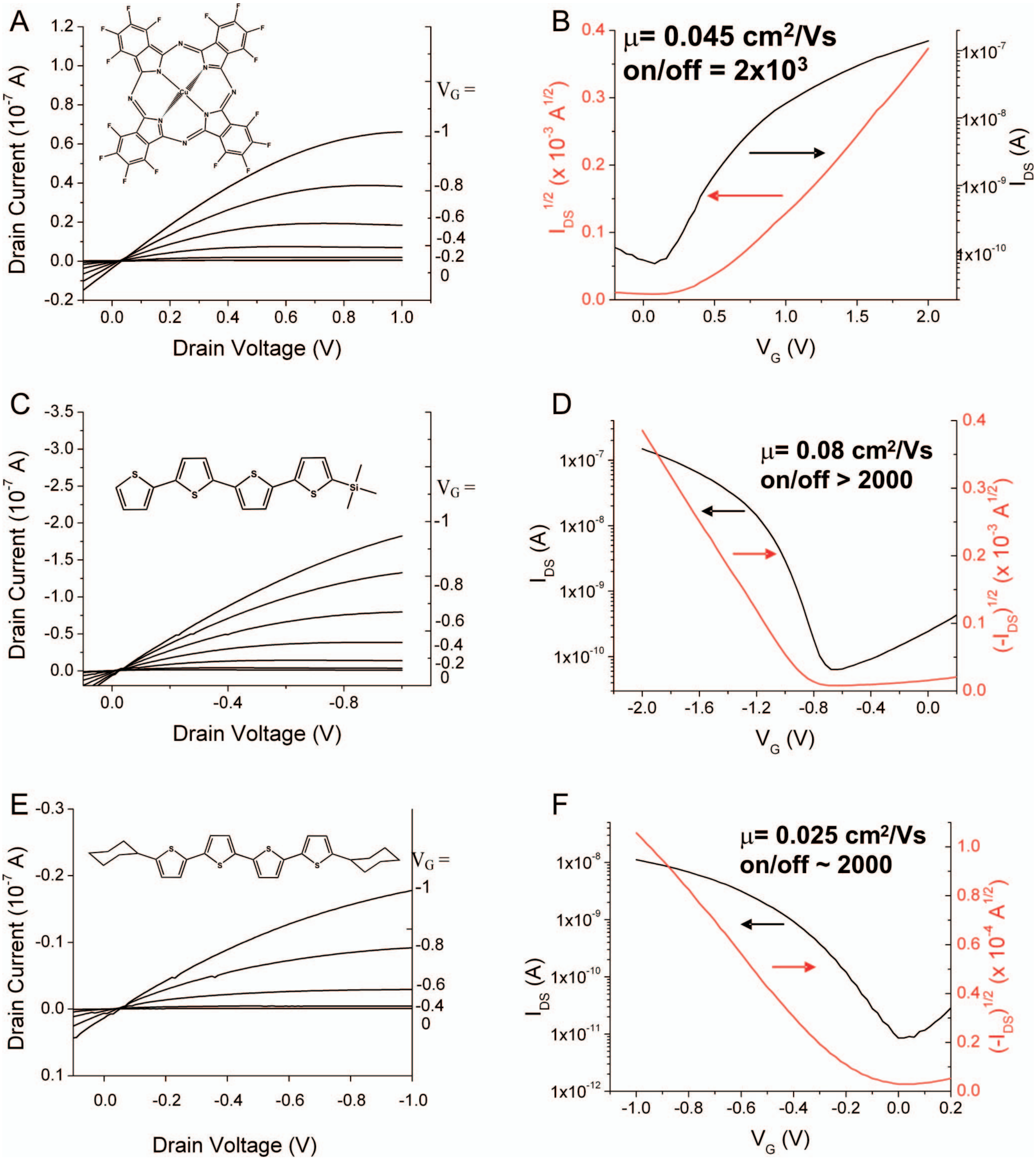

Fig. S3. OTFT performance of various organic semiconductors on PVP-HDA dielectric layer. Shown are output and transfer characteristics for FCuPc (*A* and *B*), 4TTMS (*C* and *D*), and CH4T (*E* and *F*).

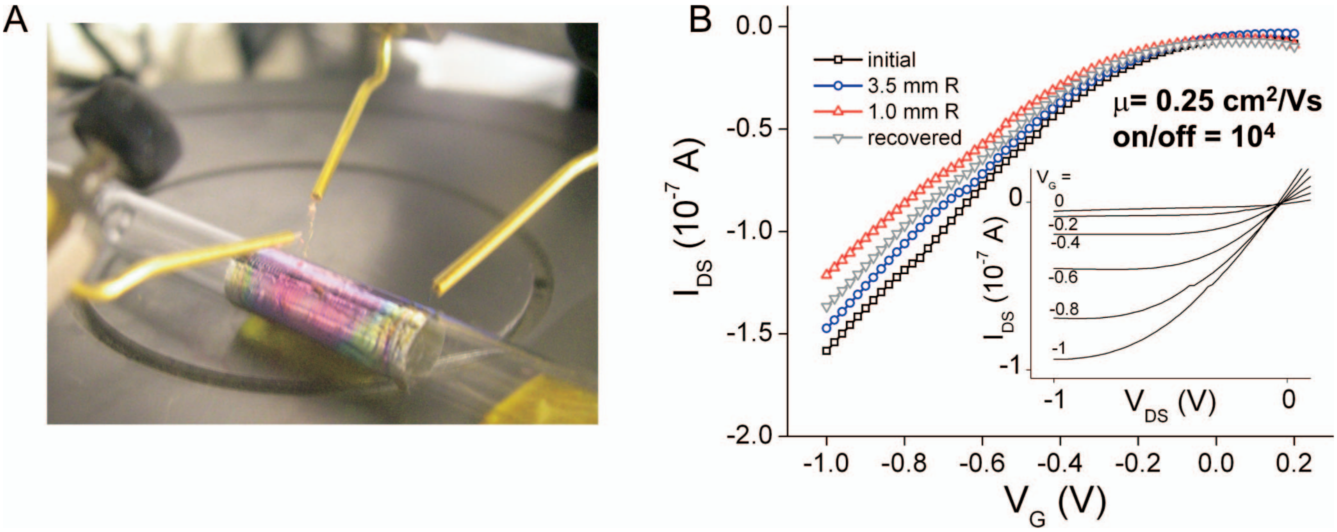

Fig. S4. (*A*) Photograph of pentacene OTFT with an 80-nm PVP-HDA dielectric layer rolled around a glass rod with a 3.5-mm radius. (*B*) Transfer characteristics of the OTFT after fabrication (black), bent to 3.5 mm (blue) and 1 mm (red) radii of curvature, and after unrolling (gray). The device performance remained reasonably stable with $\mu \sim 0.2$–0.25 cm^2/Vs and an on/off ratio of 6×10^3 to 1.1×10^4. (*Inset*) Output characteristics after bending sequence, still exhibiting nearly ideal transistor behavior.

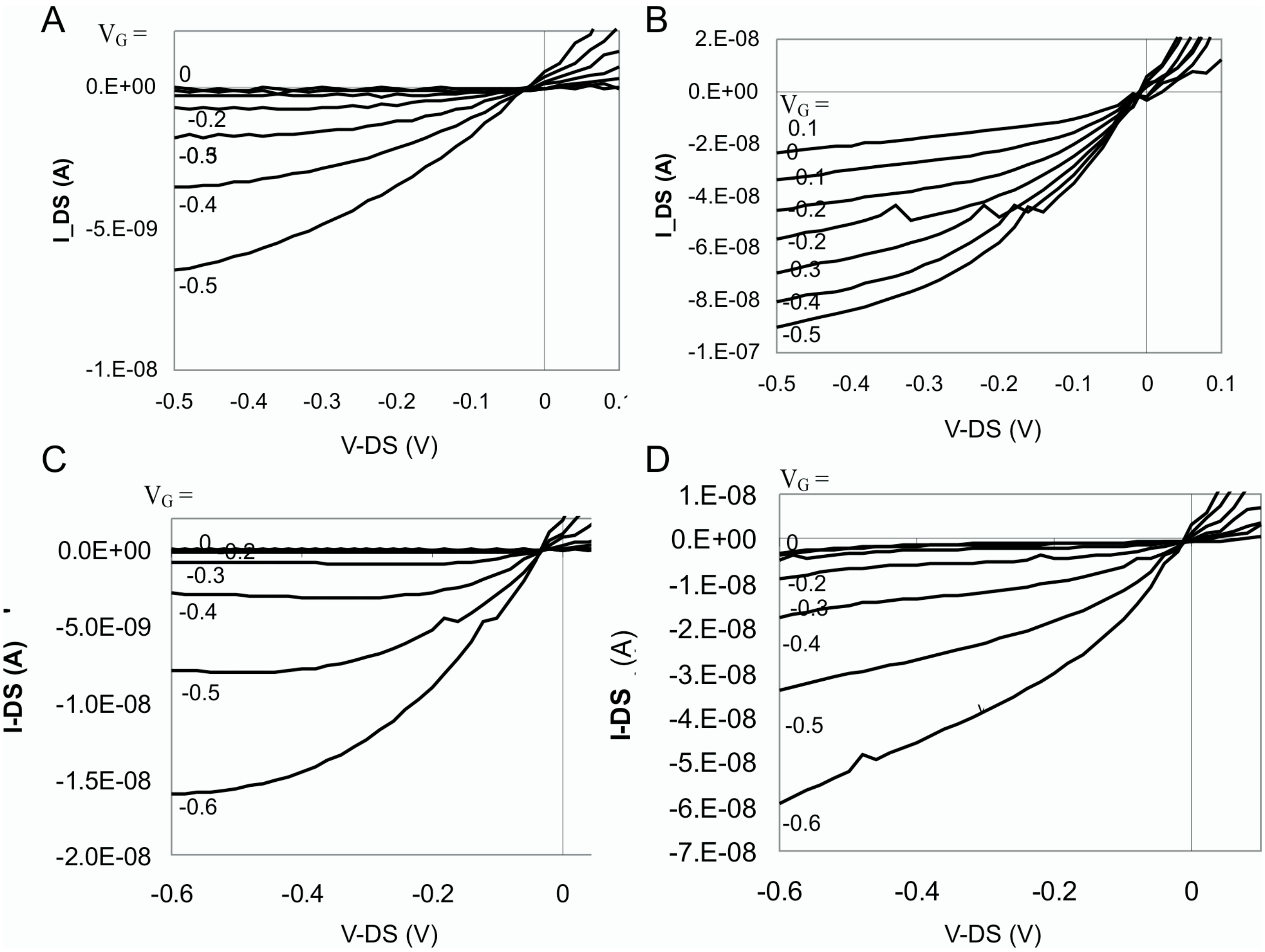

Fig. S5. Transistor characteristics of an OTFT with 10- and 25-nm DDFTTF. Shown are output characteristics of an OTFT with 10-nm DDFTTF on 22-nm PVP-HDA as deposited (*A*) and while immersed in water (*B*), and 25-nm DDFTTF as deposited (*C*) and while immersed in water (*D*).

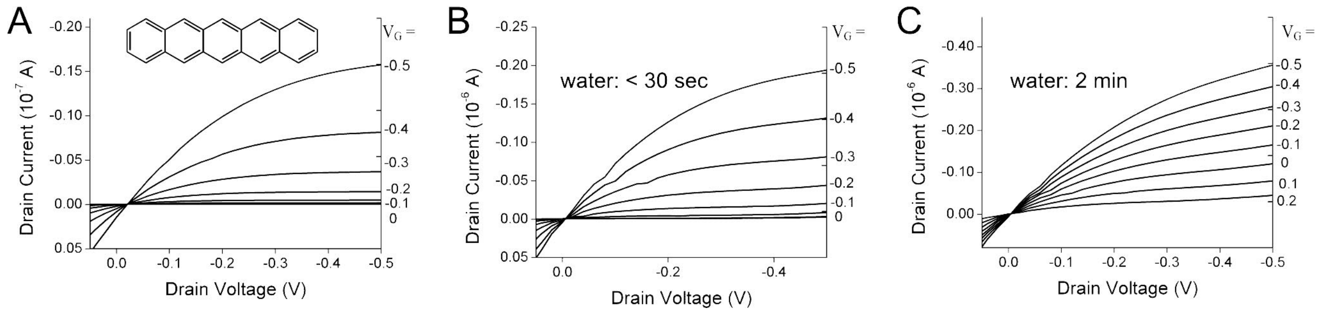

Fig. S6. Pentacene output characteristics under aqueous conditions. (*A*) Pentacene OTFT with 22-nm PVP-HDA. (*B*) Device from *A* measured immediately after immersion in water. (*C*) Output characteristics of device in *B* measured after immersion in water for 2 min.

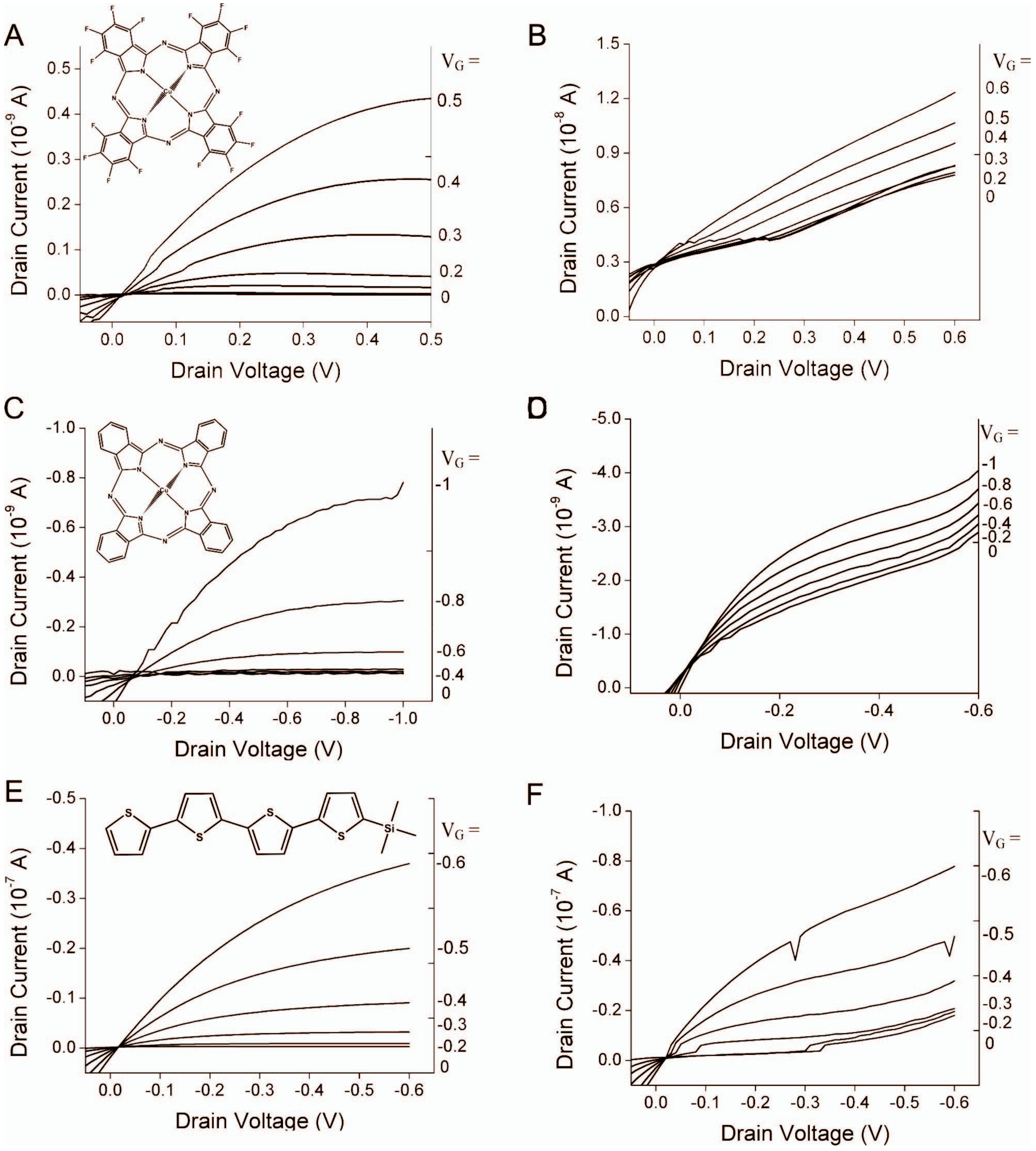

Fig. S7. Output characteristics under aqueous conditions. Shown are output characteristics of FCuPc (40 nm) on PVP-HDA (22 nm) as deposited (*A*), FCuPc (40 nm) on PVP-HDA (22 nm) under aqueous conditions (*B*), CuPc (40 nm) on PVP-HDA (22 nm) as deposited (*C*), CuPc (40 nm) on PVP-HDA (22 nm) under aqueous conditions (*D*), solution-deposited 4TTMS on PVP-HDA (22 nm) as deposited (*E*), and solution-deposited 4TTMS on PVP-HDA (22 nm) under aqueous conditions (*F*).

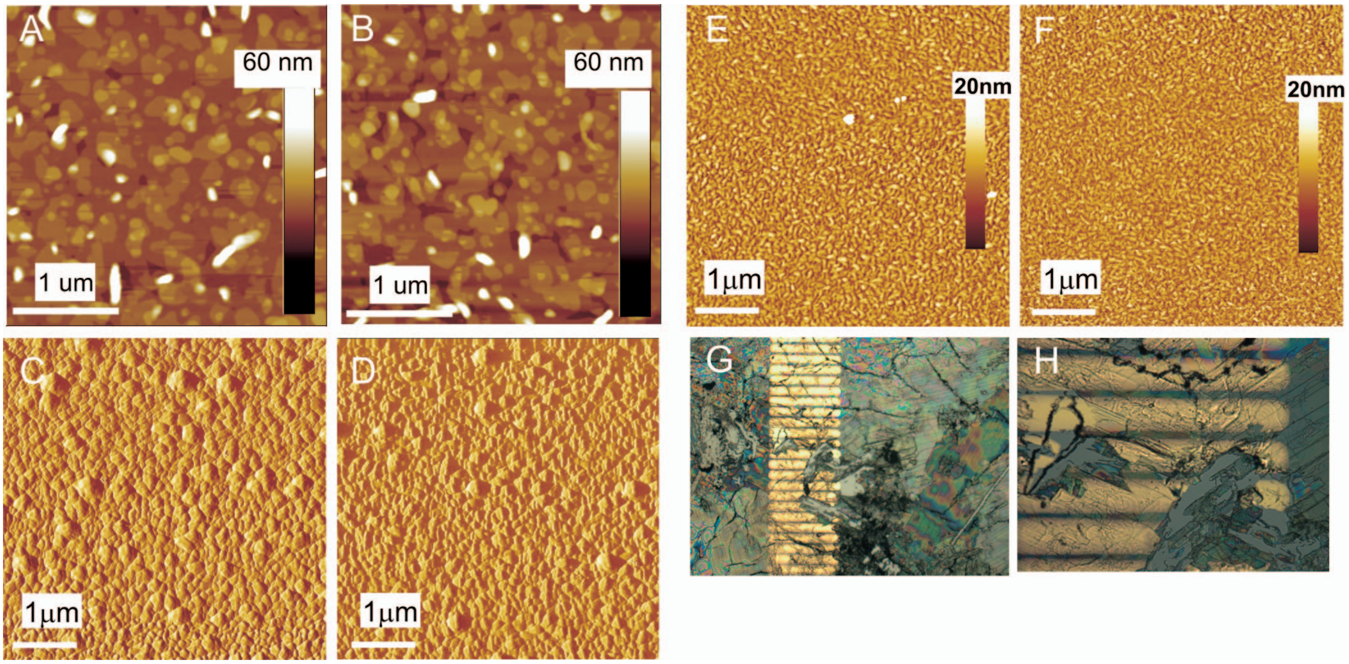

Fig. S8. Influence of water and electrical bias on film morphology. (*A*) AFM height images of at 30-nm DDFTTF ($T_{\text{substrate}} = 105°\text{C}$) on PVP-HDA as deposited. (*B*) The DDFTTF device shown in A after gate bias cycling (0.6 to -0.6 V) with $V_{\text{DS}} = -0.6$ V underwater. (*C*) AFM phase image of a 40-nm pentacene film ($T_{\text{substrate}} = 65°\text{C}$) on PVP-HDA as deposited. (*D*) The pentacene device shown in *A* after a constant source-drain bias of −1 V and a constant gate bias of −1 V under water. (*E*) AFM height images of at 40-nm FCuPc ($T_{\text{substrate}} = 105°\text{C}$) on PVP-HDA as deposited. (*F*) The FCuPc device shown in *E* after a constant source-drain bias of −1 V and a constant gate bias of −1 V underwater. (*G*) Optical micrograph (×2.5 magnification) of 4TTMS after bias under water ($V_{\text{DS}} = -1$ V, $V_{\text{G}} = -1$ V). The droplet was placed in the lower half of the electrode array. (*H*) Optical micrograph (×10 magnification) of 4TTMS from *G* expanded to clearly show the crystal delamination.

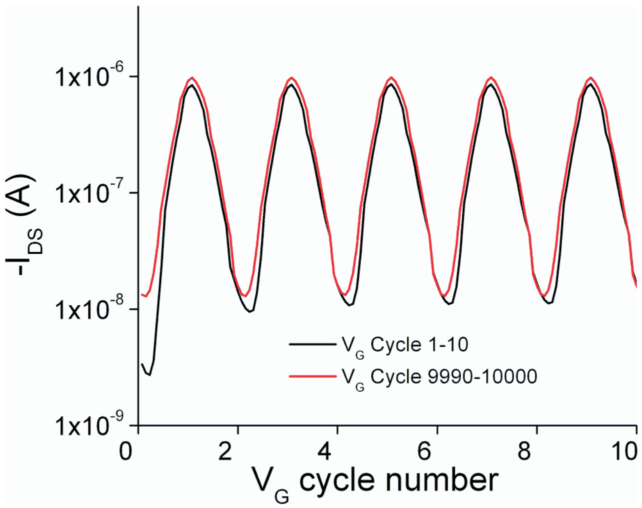

Fig. S9. I_{DS}–V_G cycle stability. Initial 10-V_G cycles (black) and final 10-V_G cycles after 10^4 electrical cycles taken from the data shown in Fig. 3*F*.

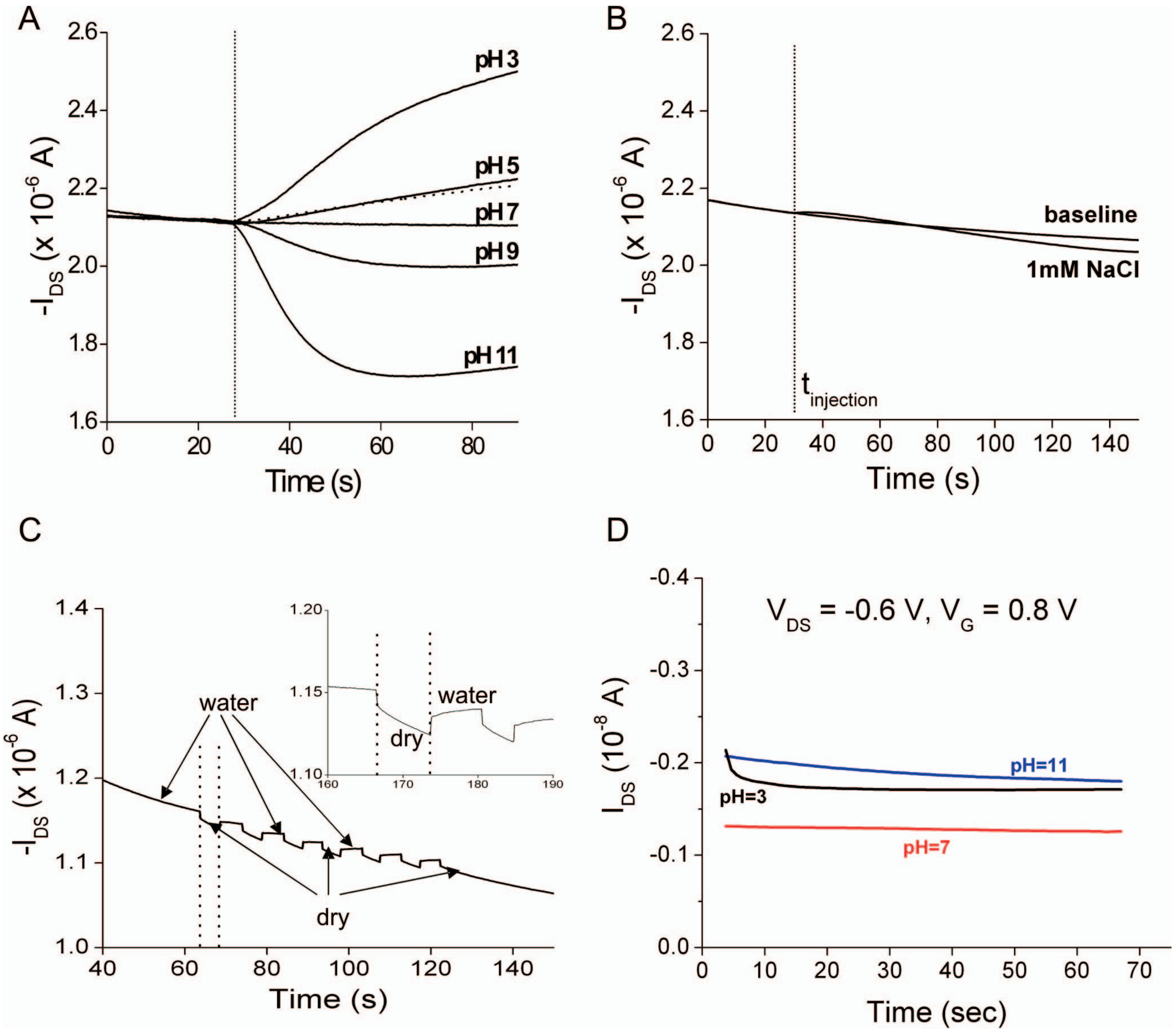

Fig. S10. pH sensor control experiments with $V_G = -1$ V and $V_{DS} = -0.6$ V. (*A*) Source-drain current response to solution of pH ranging frm 3 to 11. (*B*) Source-drain current change with 1 mM NaCl solution of similar ionic strength to pH 3 and pH 11 solutions. (*C*) Drain current steps from introducing multiple air bubbles in the flow channel. (*D*) Drain current change for pH 3 solution with $V_G = 0$. No change in current was observed.