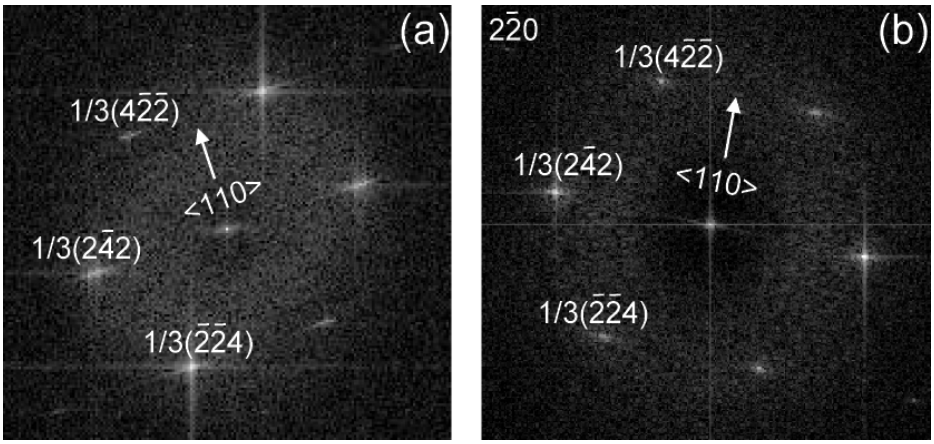

Figure S1. Two-dimensional Fourier transforms of the lattice images in Fig. 2b (a) and in Fig. 2c (b) depicting the [111] zone axis of the SiNWs show that the growth axes of the SiNWs are <110> growth direction. The six inner peaks, 1/3{422}, are forbidden in bulk silicon, but arise from the finite thickness of the nanowires with non-planar surface.[1]

1. Gibson, J. M.; Lanzerotti, M. Y.; Elser V. *Appl. Phys. Lett.* **2003**, *5*, 1710.

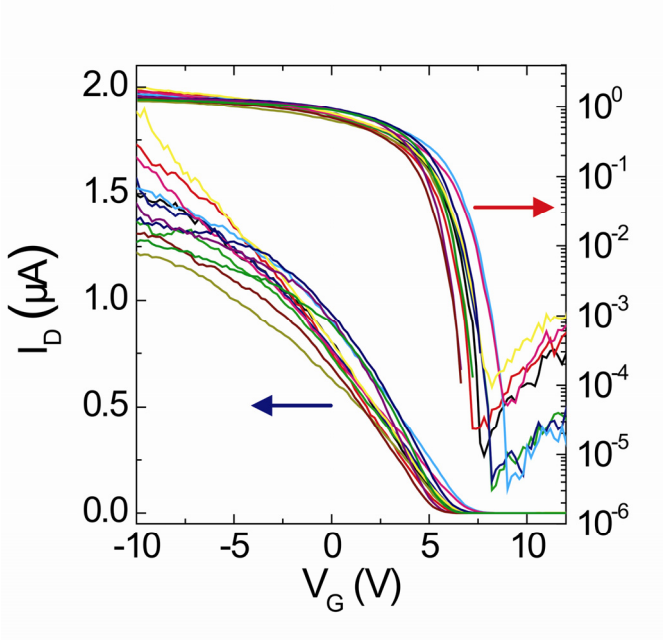

Figure S2. Source-drain current versus gate voltage (I_D–V_G) curves at a source-drain voltage (V_D) of 1 V for a sampling of devices from the single-NW multiple FETs. The devices operate in a depletion (normally on) mode with a threshold voltage (V_{th}) of 5–7 V. In addition, peak transconductance ($G_M = dI_D/dV_G$) is ca. 160–270 nS with a maximum value of 360 nS. From the logarithmic plot of I_D–V_G, the current on/off ratio and subthreshold slop are estimated at ca. 10^4–10^6 and 200–500 mV/decade, respectively.