High speed graphene transistors with a self-aligned nanowire gate

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1. Methods

Synthesis and characterization. Co_2Si nanowires were synthesized through a chemical vapour deposition process at 850 ºC. To grow Co_2Si nanowires, $CoCl_2$ powder were used as the starting materials. A ceramic boat with the $CoCl_2$ powder was placed at the upstream of a horizontal tube furnace, a silicon substrate in another ceramic boat was placed at the center as silicon source, and a SiO_2/Si substrate was placed on the silicon substrate as the deposition substrate. The temperature was raised to the target temperature with a flow of 200 sccm Ar as the protecting medium and carrying gas. The temperature was maintained for 30 min and then naturally cooled to the room temperature to obtain Co_2Si nanowires. To grow Co_2Si/Al_2O_3 core/shell nanowires, the Co_2Si nanowires were immediately transferred into atomic layer

deposition (ALD) chamber to grow Al_2O_3 shell with controlled thickness at 250 ºC using trimethylaluminum and water as the precursor and oxidant, respectively. The microstructures and morphologies of the nanostructures were characterized by a JEOL 6700 scanning electron microscope (SEM). The TEM image of the Co_2Si nanowires was obtained with an FEI Titan high-resolution transmission electron microscope (HRTEM).

Contact printing of nanowires on graphene. The overall process involves physical transfer of nanowires directly from a Co_2Si nanowire growth substrate to a graphene substrate via contact printing. Specifically, mechanically peeled graphene flakes on silicon substrate were used as the starting materials. The graphene device substrate is first firmly attached to a benchtop, and the Co_2Si nanowire growth substrate is placed upside down on top of the graphene substrate such that the Co_2Si nanowires are in contact with the graphene. A gentle manual pressure is then applied from the top followed by a slightly slide of the growth substrate. The Co_2Si nanowires are well-aligned by shear forces during the sliding process. The sliding process results in the direct and dry transfer of Co_2Si nanowires from the growth substrate to the graphene substrate. The sample is then rinsed with acetone followed by nitrogen blow-dry, in which the capillary drying process near the nanowire-graphene interface can help the Co_2Si nanowires to be firmly attached to graphene surface.

Device measurement. The DC electrical transport measurements were conducted with a Lakeshore probe station (Model CRX-4K) under ambient conditions and a computer-controlled analogue-to-digital converter (National Instruments model 6030E). The DC measurements were conducted under light illumincation to avoid deep depletion in the highly resistive silicon substrate. The on-chip microwave measurements were carried out in the range of 50 MHz to 30 GHz using Cascade RF probes and an Agilent 8722ES network analyzer under ambient conditions. The measured S-parameters were de-embedded using specific “short” and “open” structures with identical layouts, excluding the graphene channel, to remove the

effects of the parasitic capacitance and resistance associated with the pads and connections. The “through” calibration was done with exact pad layout with gate shorted to drain, and the “load” calibration was done with standard calibration pad. To achieve high fidelity in the de-embedding process, the layouts of these “open”, “short”, and “through” structures are strictly identical with that of the active device except the graphene channel.

For “open” structure, the Co_2Si/Al_2O_3 core/shell nanowires were aligned on SiO_2/Si, followed by e-beam lithography, buffered oxide etching to remove the Al_2O_3 shell and expose the Co_2Si core, and metallization (Ti/Au, 70/50 nm) process to define the source, drain and gate electrodes without graphene. A thin layer of Pt metal with the same area as that of the actual device was then deposited across the Co_2Si/Al_2O_3 core/shell nanowire, in which the Co_2Si/Al_2O_3 core/shell nanowire separates the Pt thin film into two isolated regions that form the self-aligned source and drain electrodes precisely positioned in close proximity to the nanowire gate.

For “short” structure, the Co_2Si/Al_2O_3 core/shell nanowires were aligned on SiO_2/Si, buffered oxide etching to remove the Al_2O_3 shell and expose the Co_2Si core, and metallization (Ti/Au, 70/50 nm) process to define the source, drain and gate electrodes without graphene A thin layer of Pt metal with the same area as that of the actual device was then deposited across the Co_2Si/Al_2O_3 core/shell nanowire. The Co_2Si gate NW and Pt thin film source drain electrodes were shorted together with narrow strip of Ti/Au thin film electrode.

For “through” pad, the exact GSG layout was fabricated with the gate pad directly shorted to drain pad with a 10 μm wide Ti/Au lead[1,2].

Determination of microwave device parameters. The two port S parameters can be converted to other two port parameters such as admittance parameters (Y parameters) and impedance parameters (Z parameters) using the following formula. Note that the

systems transmission line impedance (Z_0) is required for the conversion. The Y and Z parameters are complex numbers with real and imaginary parts.

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \frac{1}{Z_0} \begin{bmatrix} \dfrac{1 - s_{11} + s_{22} - \Delta s}{1 + s_{11} + s_{22} + \Delta s} & \dfrac{-2 s_{12}}{1 + s_{11} + s_{22} + \Delta s} \\ \dfrac{-2 s_{21}}{1 + s_{11} + s_{22} + \Delta s} & \dfrac{1 + s_{11} - s_{22} - \Delta s}{1 + s_{11} + s_{22} + \Delta s} \end{bmatrix} \qquad \Delta s = s_{11} s_{22} - s_{12} s_{21}$$

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = Z_0 \begin{bmatrix} \dfrac{1 + s_{11} - s_{22} - \Delta s}{1 - s_{11} - s_{22} + \Delta s} & \dfrac{2 s_{12}}{1 - s_{11} - s_{22} + \Delta s} \\ \dfrac{2 s_{21}}{1 - s_{11} - s_{22} + \Delta s} & \dfrac{1 - s_{11} + s_{22} - \Delta s}{1 - s_{11} - s_{22} + \Delta s} \end{bmatrix}.$$

2. Energy dispersive X-ray spectroscopy of the Co_2Si nanowires.

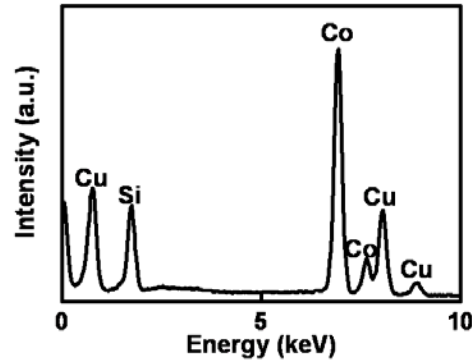

Fig. S1| Energy dispersive x-ray spectroscopy of the Co_2Si nanowire, in which the atomic ratio between Co and Si is about 2:1.

3. High resolution TEM image of the Co_2Si/Al_2O_3 core/shell nanowire.

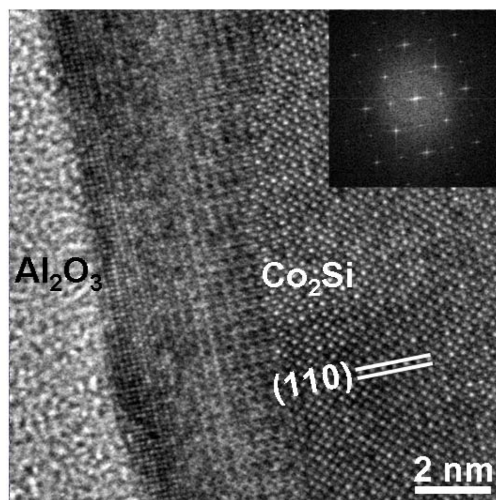

Fig. S2| High resolution TEM image of a Co_2Si/Al_2O_3 core/shell nanowire, which shows the single crystalline Co_2Si core with amorphous Al_2O_3 shell of lighter contrast, the inset shows the FFT pattern.

4. Gate-leakage current of the self-aligned device.

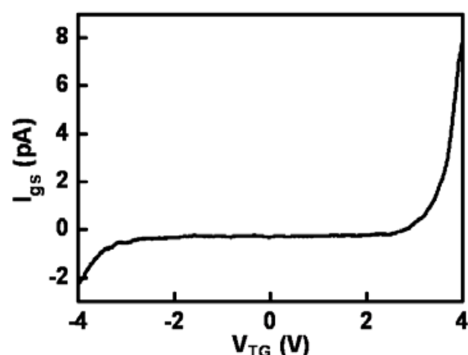

Fig. S3| Gate-leakage current versus top-gate voltage (I_{gs} - V_{TG}). With the self-aligned Pt source drain electrodes, the gate-source leakage remain small compared to the channel current in the range of V_{TG} = -4 to 4 V, and therefore would not significant affect the transistor characteristics.

5. The hysteresis of I_{ds} - V_{TG} curves.

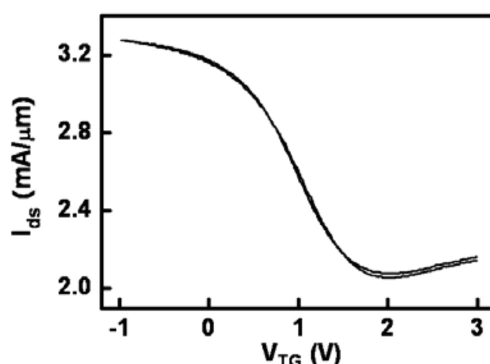

Fig. S4| The back and forth sweep of I_{ds} - V_{TG} curves shows a small hysteresis < 0.02 V under the ambient conditions at V_{ds} = 1 V.

6. The electrostatic capacitance between the nanowire gate and graphene.

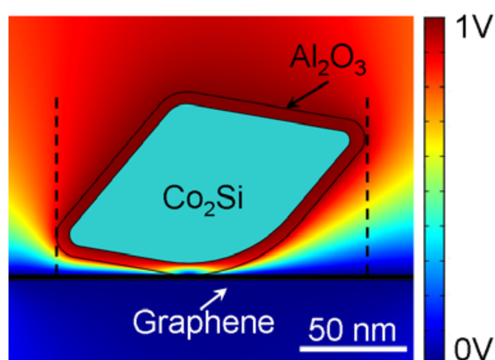

Fig. S5| The finite element simulation of the electrostatic capacitance between Co_2Si/Al_2O_3 nanowires and graphene. The total top-gate capacitance (including simulated electrostatic capacitance and quantum capacitance) normalized by graphene channel area is about 394 nF/cm^2.

7. The |h21| of devices without de-embedding.

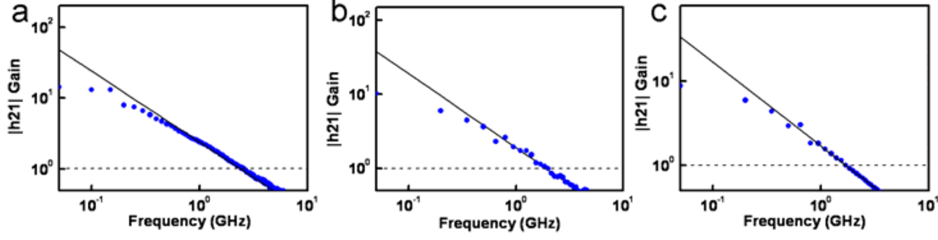

Fig. S6| The current gain |h21| of the three devices without de-embedding procedures. (a) The |h21| of the device with 144 nm gate length, indicating the uncorrected f_T of 2.4 GHz. (b) The |h21| of the device with 182 nm gate length, indicating the uncorrected f_T of 1.9 GHz. (c) The |h21| of the device with 210 nm gate length, indicating the uncorrected f_T of 1.6 GHz. The solid line corresponds to the ideal 1/f dependence of the current gain.

8. The equivalent circuit topology and component value extraction.

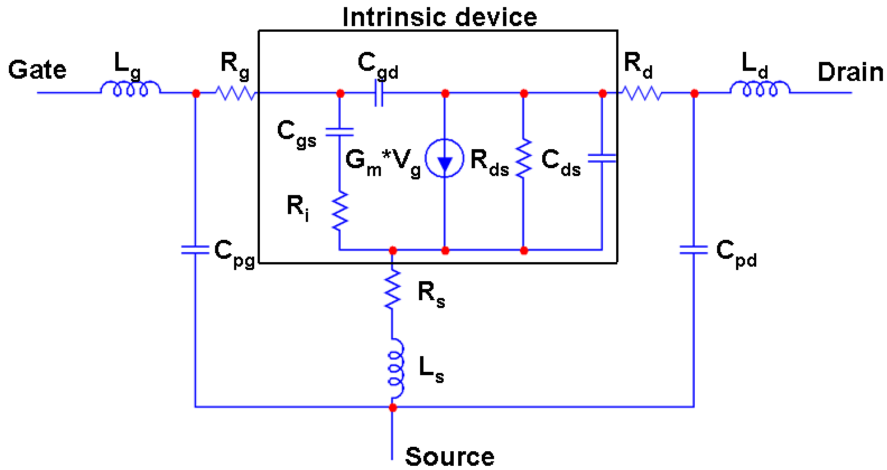

Fig. S7| The equivalent circuit topology and component value extraction. The C_{pg} and C_{pd} is gate and drain parasitic capacitance, R_s, R_d, and R_g is the resistance of source, drain and gate electrodes. L_s, L_d, and L_g is the inductance of source, drain and gate electrodes. C_{gs}, C_{gd} is the top-gate to source and top-gate to drain capacitance, C_{ds} and R_{ds} is the capacitance and resistance between drain and source. R_i is the resistance of dielectrics. All the device component values can be derived from S-parameter measurement using the following microwave formula. Here Y and y, Z and z are respective parameters of the device before and after de-embedding process[3-5], which can be used to extract all device component values.

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} y_{11} + j\omega C_{pg} & y_{12} \\ y_{21} & y_{22} + j\omega C_{pd} \end{bmatrix}$$

$$y_{intrinsic} = \left[\left(Y_{DUT} - Y_{open} \right)^{-1} + \left(Y_{short} - Y_{open} \right)^{-1} \right]^{-1}$$

$$y_{11} = \frac{R_i \omega^2 C_{gs}^2}{1 + R_i \omega^2 C_{gs}^2} + j\omega \left(\frac{C_{gs}}{1 + R_i \omega^2 C_{gs}^2} + C_{gd} \right)$$

$$\mathrm{Im}(y_{12}) = -\omega(C_{gd})$$

$$\mathrm{Im}(y_{11} + y_{12}) \approx \omega(C_{gs})$$

$$\mathrm{Im}(y_{22} + Y_{12}) \approx \omega(C_{ds})$$

$$g_m = g_{mo} \exp(-jw\tau)$$

$$\mathrm{Re}(y_{21}) \approx \frac{g_{mo}}{\sqrt{1 + (R_i 2\pi f C_{gs})^2}} \approx g_{mo}$$

$$\mathrm{Re}(y_{11}) \approx R_i \omega^2 C_{gs}^2 \approx R_i (2\pi f)^2 C_{gs}^2$$

$$\mathrm{Re}\,al(y_{22}) \approx g_{ds}$$

$$Z_{12} - z_{12} = R_s + jwL_s$$

$$Z_{11} - z_{11} = R_s + R_g + jw(L_s + L_g)$$

$$Z_{22} - z_{22} = R_s + R_d + jw(L_s + L_d)$$

9. The component parameter values for the second device.

Device No.	C_{pg} (pF)	C_{pd} (pF)	R_g (ohm)	R_{ds} (ohm)	g_{mo} (mS)	τ (ps)	R_i (ohm)	C_{ds} (fF)	C_{gs} (fF)	C_{gd} (fF)	L_d (pH)	L_g (pH)	L_s (pH)	R_s (ohm)	R_d (ohm)
3	0.22	0.23	180	157	2.6	0.8	250	0.2	2.2	0.2	66	140	12	2.4	13.9

Table S1| The component parameter values for the second device.

Device No.	W_g (µm)	l_g (nm)	G_m (mS)	C_{gs} (fF)	C_{gd} (fF)	C_{pg} (pF)	Projected f_T' (GHz)	f_T' (GHz)	Projected f_T (GHz)	f_T (GHz)
3	3.32	182	2.6	2.2	0.2	0.22	2.0	1.9	177	168

Table S2| The performance parameters for the third device. Here f_T' is the cutoff frequency without de-embedding, and f_T is the cutoff frequency with de-embedding. The projected f_T values for all devices with and without de-embedding process can be determined based on DC device parameters. Importantly, the critical device parameters (including C_{pg}, C_{gs}, C_{gd}, g_m, f_T' and f_T) derived from S-parameters are consistent with the values determined from DC measurements or electrostatic simulations (the parasitic pad capacitance was simulated using Comsol Multiphysics

program), demonstrating the validity of the RF measurements and the de-embedding procedures. The value of the projected f_T' can be determined by[6]:

$$f_T' = \frac{g_m}{2\pi\left[\left(C_{gs} + C_{gd}\right)\left(1 + \frac{R_d + R_s}{R_{ds}}\right) + C_{gd} g_m \left(R_d + R_s\right) + C_{pg}\right]},$$

And the value of the projected f_T can be determined by:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}.$$

10. The |h21| of additional devices with smaller parasitic capacitance.

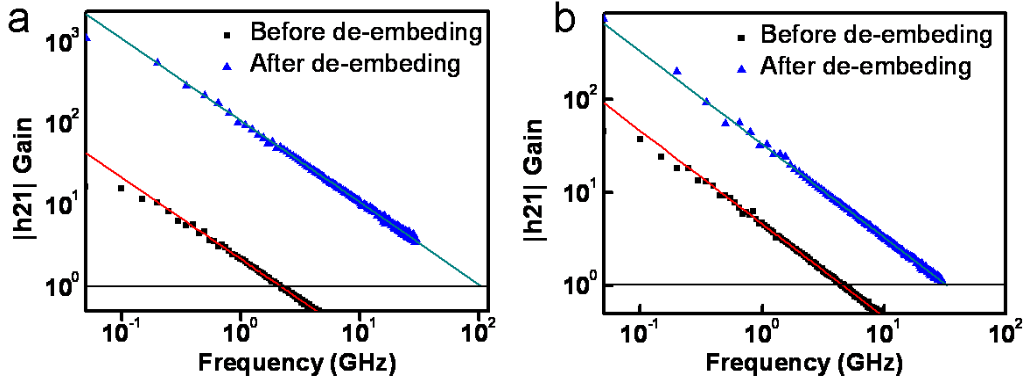

Fig. S8| The current gain |h21| of two additional devices before and after de-embedding. (a) The |h21| of the device with smaller gate pad on 300 nm SiO_2/Si substrate. The device has a channel length of 243 nm and width of 3.1 μm, and biased at V_{ds}= -1 V and V_{TG}= 0.8 V. (b) The |h21| of the device with smaller gate pad on 870 nm SiO_2/Si substrate. The device has a channel length of 215 nm and width of 7.2 μm, and biased at V_{ds}=-1 V and V_{TG}=1.15 V. To further validate our de-embedding procedures, we have used two methods to re-design the device layout to reduce the parasitic capacitance. In the first approach (***a***), we simply reduced the signal-pad area on 300 nm SiO_2/Si substrate, in which we have reduced the parasitic pad capacitance by ~37 % (from 0.23 pF for device #1-3 to 0.145 pF for this device) obtained a much smaller ratio (~48) between intrinsic and extrinsic f_T (105 GHz vs. 2.2 GHz). In a second approach (***b***), we fabricated the devices on 870 nm SiO_2/Si substrate. We used CVD graphene in this case because of the difficulties in locating graphene flakes on 870 nm SiO_2/Si substrate. With thicker SiO_2, we can substantially reduce the parasitic pad capacitance by ~78 % (to 0.051 pF) and obtain a ratio between intrinsic and extrinsic f_T as small as ~ 7.2 (33 GHz vs. 4.6 GHz). The lower intrinsic f_T achieved here is due to other issues related to the less than ideal quality of the CVD graphene and the contact to CVD graphene.

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