Supporting Information

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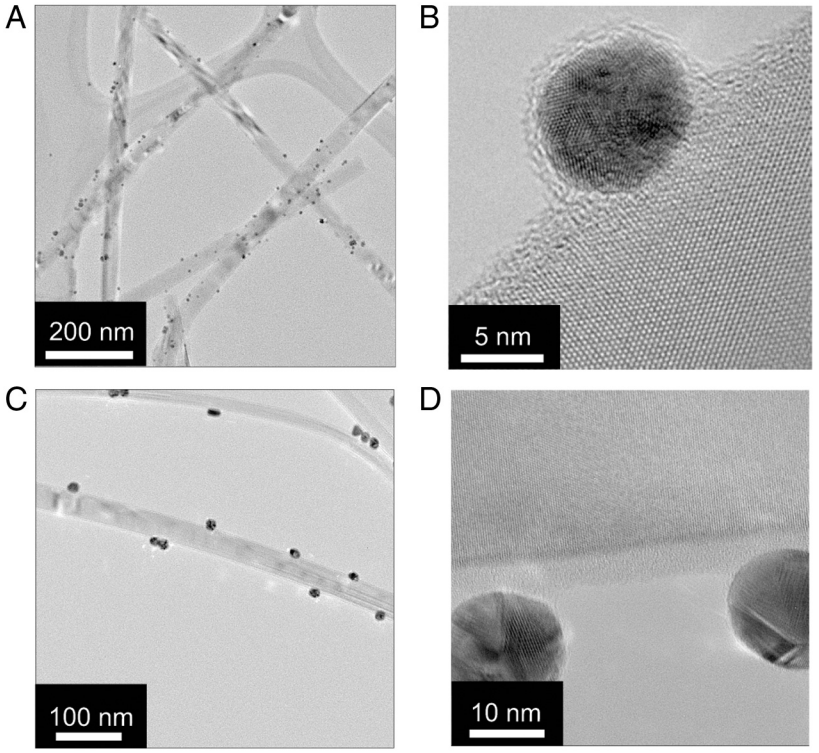


Fig. S1. Preparation of gold nanoparticles (Au-NPs) on Si and Si/SiO_2 nanowire (NW) backbones. (*A* and *B*) Low- (*A*) and high-resolution (*B*) transmission electron microscopy (TEM) images of Si NWs with Au-NPs on their surfaces. The selective deposition of Au-NPs on bare Si NW backbones was achieved via galvanic surface reduction (see *Materials and Methods*), in which hydrogen-terminated Si NW surfaces induced the in situ reduction of $HAuCl_4$ and formation of Au-NPs on the backbone. The Au-NPs prepared in this manner are well-dispersed along the Si NW surfaces. For $HAuCl_4$ concentration of 10^{-5} M and reaction time of 5 min, the NP diameters were 10 ± 2 nm. (*C* and *D*) Low- (*C*) and high-resolution (*D*) TEM images of Si/SiO_2 core/shell NWs with Au-NPs. The Si/SiO_2 NWs were first functionalized with polylysine, and then citrate stabilized Au-NPs (Ted Pella) were adsorbed onto the NW surfaces (see *Materials and Methods*). The high-resolution image (*D*) shows clearly the SiO_2 thickness of approximately 3 nm and Au-NP diameters of approximately 15 nm.

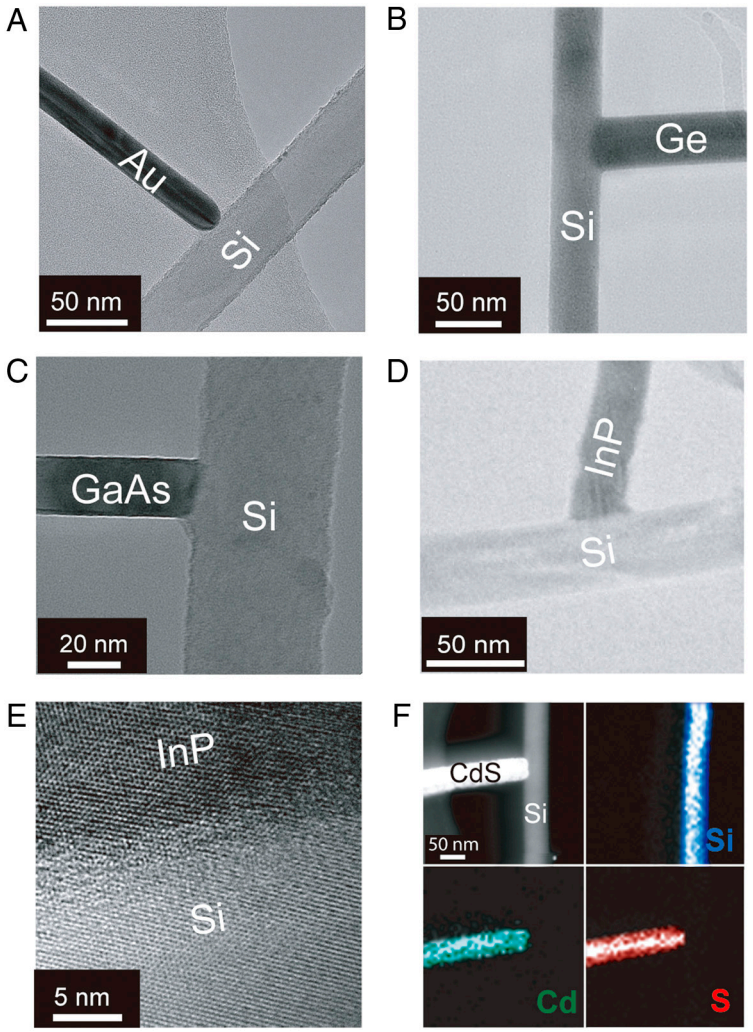


Fig. S2. Structural characterization of type I branched NWs. (*A*–*D*) TEM images of Si/Au (*A*), Si/Ge (*B*), Si/GaAs (*C*), and Si/InP (*D*) branched NWs. (*E*) High-resolution TEM image of a representative Si/InP branch junction. The Si/InP interface remains structurally coherent despite the large lattice mismatch (8.1%). (*F*) Scanning TEM image (*Upper Left*) and corresponding energy-dispersive X-ray elemental mapping from a Si/CdS branched NWs. The maps for Si, S, and Cd are shown (*Upper Right*, *Lower Right*, and *Lower Left*, respectively). Data demonstrate the spatially controlled distributions of Si, Cd, and S in the backbone and branch. We note that the Si backbone is free of CdS homogenous shell coating or islands formation due to the well-controlled branch synthesis. All branches were grown from Au-NPs prepared directly on Si-NW backbones without intervening shell layers using either solution- or gas-phase approaches (see *Materials and Methods*).

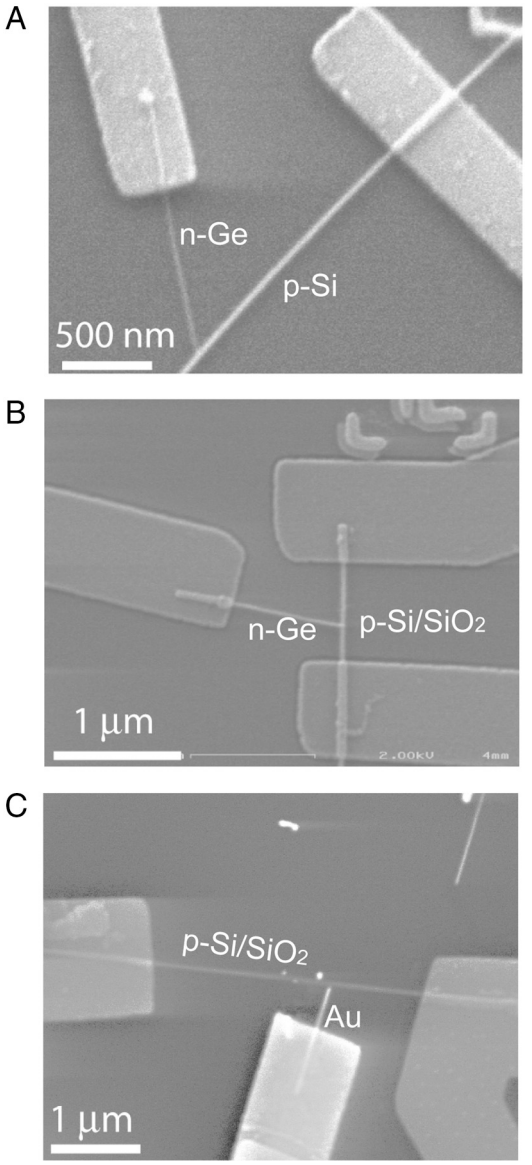


Fig. S3. SEM images of single-branch input NW devices. (*A*) Si/Ge p-n diode. The Si backbone and Ge branch were p- and n-doped, respectively. During measurement, bias was applied to the Si backbone while the Ge branch was grounded. (*B* and *C*) $Si/SiO_2/Ge$ (*B*) and $Si/SiO_2/Au$ (*C*) field effect transistors. The lightly doped Si NW backbone functions as the active semiconducting channel, the SiO_2 shell layer as the gate dielectric, and the heavily doped n-Ge or Au branch NWs as local gate electrodes. All devices were fabricated by electron-beam lithography (see *Materials and Methods*).

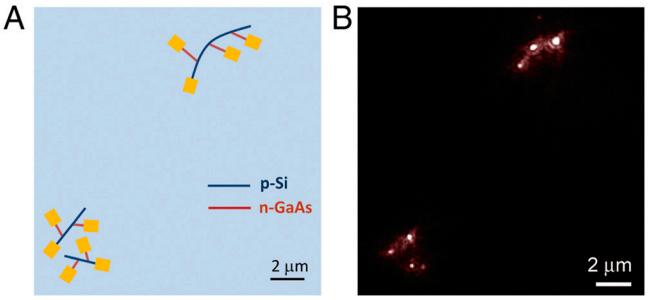
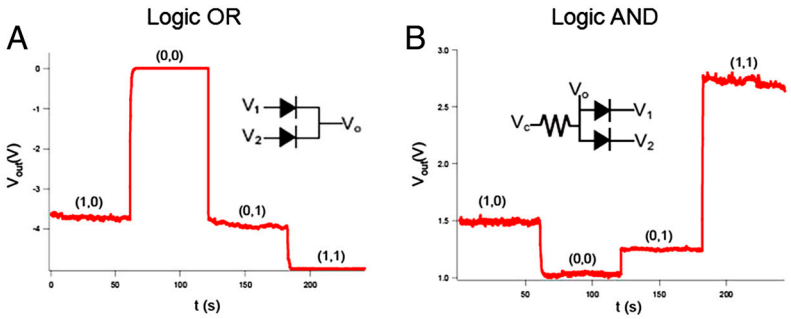


Fig. S4. Multibranch p-Si/n-GaAs backbone/branch NW nanoLEDs. (*A*) Schematic illustrating the three multibranch structures, consisting of three distinct SiNW backbones with a total of seven GaAs NW branches. The Si/GaAs branch junctions define seven nanoLEDs. (*B*) When a forward bias of 10 V was applied to turn on all of the branch nanoLEDs, electroluminescence (EL) measurements demonstrate highly localized emission from each of the junctions. Selected branch junctions could also be biased and showed addressable emission only from those junctions in forward bias (Fig. 5*B*). Localized emission from the branch junctions was robust; that is, repeated on/off cycles did not affect the emission properties. These results demonstrate the potential of this bottom-up approach for larger-scale integrated optoelectronic devices. Devices were fabricated by e-beam lithography, and EL was characterized with a homebuilt instrument (see *Materials and Methods*).



V_{i1}(V)	V_{i2}(V)	V_{out}(V)
-5.00 (1)	0.00 (0)	-3.71 (1)
0.00 (0)	0.00 (0)	0.00 (0)
0.00 (0)	-5.00 (1)	-3.95 (1)
-5.00 (1)	-5.00 (1)	-4.98 (1)

V_{i1}(V)	V_{i2}(V)	V_{out}(V)
5.00 (1)	0.00 (0)	1.47 (0)
0.00 (0)	0.00 (0)	1.02 (0)
0.00 (0)	5.00 (1)	1.24 (0)
5.00 (1)	5.00 (1)	2.74 (1)

Fig. S5. OR and AND logic gates based on two sequential p-Si/n-Ge backbone/branch p-n diodes. (*A*) OR logic gate. (*Upper*) The output voltage vs. the four possible logic address level inputs: (1,0), (0,0), (0,1), and (1,1). (*Inset*) The schematic of the OR gate. (*Bottom*) The experimental truth table for the OR gate. When either or both of the input voltages are high (−5 V), at least one of the diodes is forward-biased and the correspondent output voltages are high. The output voltage is low only when both input voltages are low (0 V). (*B*) AND logic gate. (*Upper*) The output voltage vs. the four possible logic address level inputs: (1,0), (0,0), (0,1), and (1,1). (*Inset*) The schematic of the AND gate. The p-Si backbone is biased at 5 V; the resistance of the constant resistor is 50 MΩ.(*Bottom*) The experimental truth table for the AND gate. When either or both of the inputs are low, at least one of the p-n junctions is forward-biased with low resistance, so the output voltage is low. When both inputs are high, both p-n junctions are reverse-biased with resistances much larger than that of the constant resistor so a high voltage is achieved at the output. We note that although V_{out} values at logic "0" are significantly lower than logic "1," they are not zero, which reflects leakage through the reverse-biased junctions. All devices were fabricated by electron-beam lithography (see *Materials and Methods*).