Supporting Information

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SI Text

SI Methods. ***Fabrication of Self-Aligned Graphene Transistors with Transferred Gate Stacks.*** First, a 50-nm gold thin film is deposited on a Si/SiO_2 substrate using e-beam evaporation. An Al_2O_3 top-gate dielectrics film is then deposited on gold surface by atomic layer deposition (ALD) at 250 °C. The Al_2O_3 top-gate dielectrics film is then patterned by anisotropic reactive ion etching (RIE) using e-beam patterned metal strips as the etching mask to form the metal–dielectrics stack structure. Next, the Al_2O_3 sidewall is formed by using ALD at 250 °C. The anisotropic RIE process is employed to etch away the dielectric on top of the gold, leaving the rest covered on the sidewall of the gate dielectric stacks. A thin layer of AZ4620 photoresist is then spin-coated onto the substrate to wrap around the gate stack. A thermal release tape (TRT) is attached onto the top of the substrate, and then the whole structure is immersed in deionized (DI) water at room temperature, followed by the peeling off of an edge of the TRT. The gold layer is then etched away using gold etchant. Next, the TRT and the attached top-gate structure are laminated onto patterned graphene strips. A peeling-off process is operated at the glassy transition point of the photoresist followed by repeated acetone rinsing in order to remove the photoresist. E-beam lithography and vacuum metallization (Ti/Au, 70 nm/50 nm) are used to define the source, drain, and gate electrodes. A thin layer of Pd/Au (5 nm/10 nm) metal is then deposited across the gate stack to form the self-aligned source and drain electrodes. The microstructures and morphologies of the nanostructures are characterized by a JEOL 6700 SEM. The cross-section image of the self-aligned device is obtained by a FEI Titan transmission electron microscope (TEM).

Device measurement. The dc electrical transport measurements are conducted with a Lakeshore probe station (Model TTP4) and a computer-controlled analogue-to-digital converter (model 6030E; National Instruments) under ambient conditions. The on-chip microwave measurements are carried out in the range of 50 MHz to 30 GHz using Cascade RF probes and an Agilent 8361A network analyzer under ambient conditions. The measured S parameters are de-embedded using specific "short" and "open" structures with identical layouts to remove the parasitic capacitance and resistance associated with the pads and connections. The "through" calibration is done with the exact layout in which the gate shorted to drain, and the "load" calibration is performed with a standard calibration pad.

For "open" structure, the gate stacks are transferred on to desired substrate, followed by e-beam lithography and metallization (Ti/Au, 70 nm/50 nm) processes to define the source, drain, and gate electrodes. A thin layer of Pd/Au metal with the same area as that of the actual device is then deposited across the gate stack, in which the gate stack separates the Pd/Au thin film into two isolated regions that form the self-aligned source and drain electrodes precisely close to the gate stack. For the "short" structure, the stacks are transferred onto desired substrate, followed by the formation gate and self-aligned source drain electrodes. Next, the gate stacks and the self-aligned electrodes are shorted by a narrow strip of Ti/Au film. For "through" structure, the identical ground-signal-ground (GSG) layout is fabricated with the gate electrodes directly short to drain electrodes with a 10-μm wide Ti/Au lead (1, 2).

Synthesis and transfer process of CVD-grown graphene. The graphene is grown by chemical vapor deposition on copper foil at 1,050 °C, with methane as the carbon-containing precursor. At first, Cu foils (25-μm thick, 99.8%; Alfa Aesar) are loaded into a 1-inch quartz tube inside the horizontal furnace of a home-built CVD system. The furnace is then allowed to heat up to 1,080 °C with H_2/Ar flow (25 sccm/475 sccm) to anneal the Cu foil for 90 min. After annealing, the temperature is dropped to 1,050 °C in 10 min. The graphene growth is initiated by feeding methane (500 ppm methane in Ar, 35 sccm) balanced with the H_2/Ar (25 sccm/440 sccm). After growth, the graphene is transferred onto SiO_2/Si substrate for characterization and device fabrication. Initially, the graphene is grown on both sides of the copper foils. To transfer the graphene, we first spin-coat a layer of PMMA film onto one side of the graphene/Cu foil and clean the other side with O_2 plasma. The copper is then etched away using copper etchant by floating the foil on the surface of the etchant bath. The PMMA/graphene film is washed with HCl/H2O (1:10) and DI water several times, and transferred onto desired substrate.

1. Lin YS, Chen CC, Liang HB, Huang MS (2007) Analyses and wideband modeling (DC-TO-50 GHz) of dummy open devices on silicon for accurate RF devices and ICS de-embedding application. *Microw Opt Tech Lett* 49:879–882.
2. Cho HJ, Burk DE (1991) A three-step method for the de-embedding of high frequency S-parameter measurement. *IEEE T Electron Dev* 38:1371–1375.

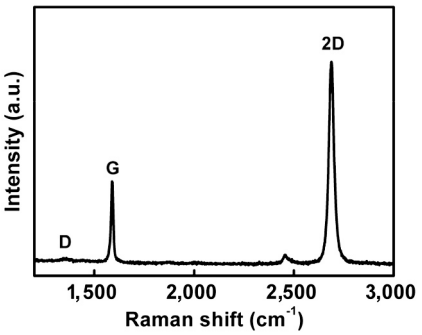

Fig. S1. The Raman spectrum of CVD-grown graphene on SiO_2/Si substrate. The ratio of G peak to 2D peak reveals the single-layer property of CVD-grown graphene.

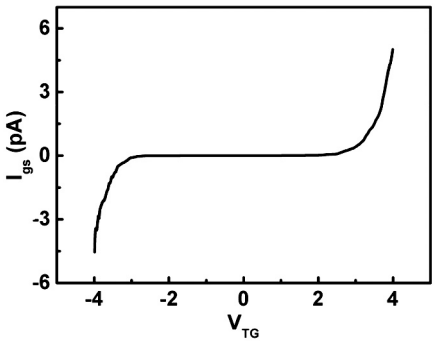

Fig. S2. Gate-leakage current versus top-gate voltage (I_{gs}–V_{TG}). With the self-aligned Pd/Au source drain electrodes, the gate-source leakage remains very small compared to the channel current in the range of $V_{TG} = -4$ to 4 V. The leakage current does not significantly affect the transistor characteristics.

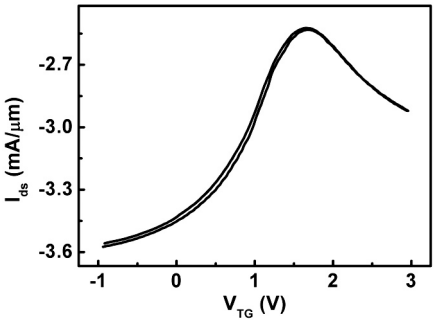

Fig. S3. The back-and-forth sweep of I_{ds}–V_{TG} curve of a peeled graphene device with transferred gate stack. The curve shows a small hysteresis <0.07 V under ambient conditions at $V_{ds} = 1$ V, highlighting the excellent dielectric quality of the gate stack.

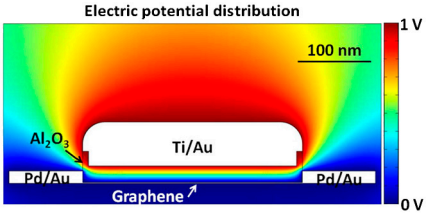

Fig. S4. Finite element simulation of the electrostatic capacitance between transferred gate stack and graphene. The simulated electrostatic capacitance normalized by graphene channel area is about 359 nF/cm^2.

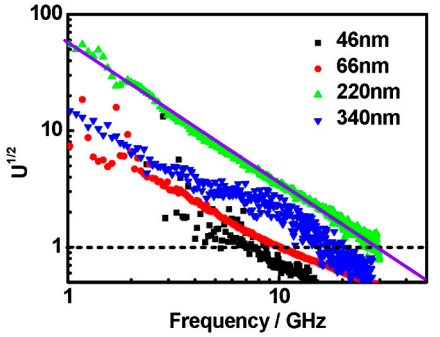

Fig. S5. Plot of power gain versus frequency. Mason's unilateral gain versus frequency for four devices with different channel lengths is plotted. A peak f_{max} of 29 GHz is obtained from the 220-nm device.

Table S1. The component parameter values for three CVD-grown graphene devices

Device	Width (μm)	Length(nm)	g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	R_s (Ω)	R_d (Ω)	Projected f_T (GHz)	f_T (GHz)
1	8	220	3.9	8.10	2.86	14	18	56	57
2	8	100	3.5	3.86	1.03	11	15	114	110
3	8	46	3.4	2.04	0.41	10	19	221	212

The projected f_T (intrinsic cutoff frequency) values can be determined based on dc device parameters. The critical device parameters (including C_{gs}, C_{gd}, gm, R_s, R_d, and f_T) derived from S-parameters are consistent with the values determined from dc measurements or electrostatic simulations, demonstrating the validity of the rf measurements and the de-embedding procedures (1).

1 Sze SM, Ng KK (2007) *Physics of Semiconductor Devices* (Wiley Interscience, New York), pp 263–275.