Supporting Information

Vlad et al. 10.1073/pnas.1208638109

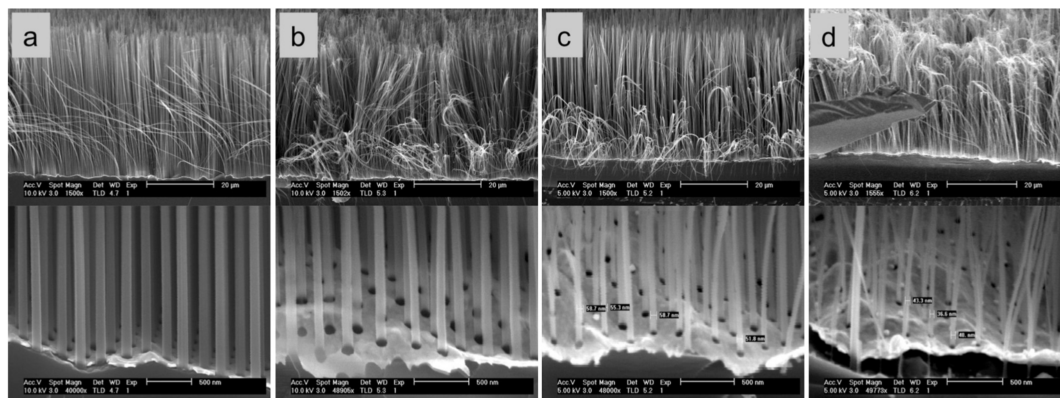

Fig. S1. *MACE processing with Au catalyst mask.* The increase in the colloidal etch time (from *A* to *D*) dictates the results in

—> decrease of the catalytic hole mask size
—> decrease in the diameter of the Si-nanowires. Three direct benefits follow:
—> (i) lower gravimetric electrode loading,
—> (ii) higher polymer/electrolyte uptake,
—> (iii) easier volume expansion/mechanical stress accommodation during the lithiation/delithiation of Si-nanowires. Nanowires as small as 20 nm in diameter have been fabricated using this method.

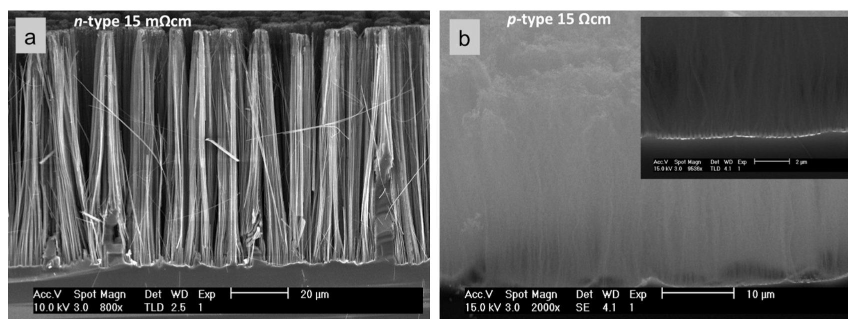

Fig. S2. *MACE processing with Pt catalyst mask.* (*A*) Ultra-high aspect ratio Si-nanowires (*n*-type Si, 15 mΩ cm) fabricated using a Pt (25 nm thick) mask and 4.8M HF + 0.2M H_2O_2 as etchant solution. The etching time was 60 min resulting in a etch rate of more than 1 μm/ min. (*B*) Applying the same recipe on *p*-type 15 Ω cm silicon produced highly porous and brittle nanowires.

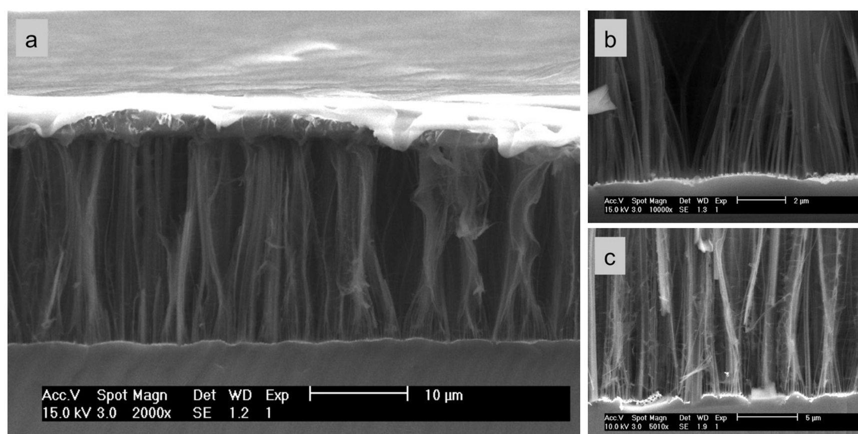

Fig. S3. *Polymer infiltration.* (*A*) The polymer infiltration was performed with a 5% polymer by wt. solution in acetone. Conformal coating of the Si nanowires failed when simply adding and drying an excess polymer solution. A continuous polymer film formed on top of the substrate without infiltrating the nanowires presumably due to a fast evaporation rate of the solvent within the high surface area Si nanowire forest. (*B*, *C*) Enlarged views evidencing the poor quality of the polymer infiltrated Si-nanowire array.

0.25h
surface nucleated *Cu* cluster
"grainy" discontinuous coating

0.5h
interconnected grains,
"porous" *Cu* shell

1h
thin continuous *Cu* shell

2h
thick continuous *Cu* shell

evolution of the
coaxial *Cu*
layer is visible

optimal configuration:
- Cu layer for charge collection;
- porosity for fast Li^+ migration;
- large free volume for polymer/electrolyte uptake

Fig. S4. *Evolution of the Cu shell layer function of reaction time at 60 °C.*