Supporting Information

Yao et al. 10.1073/pnas.1323818111

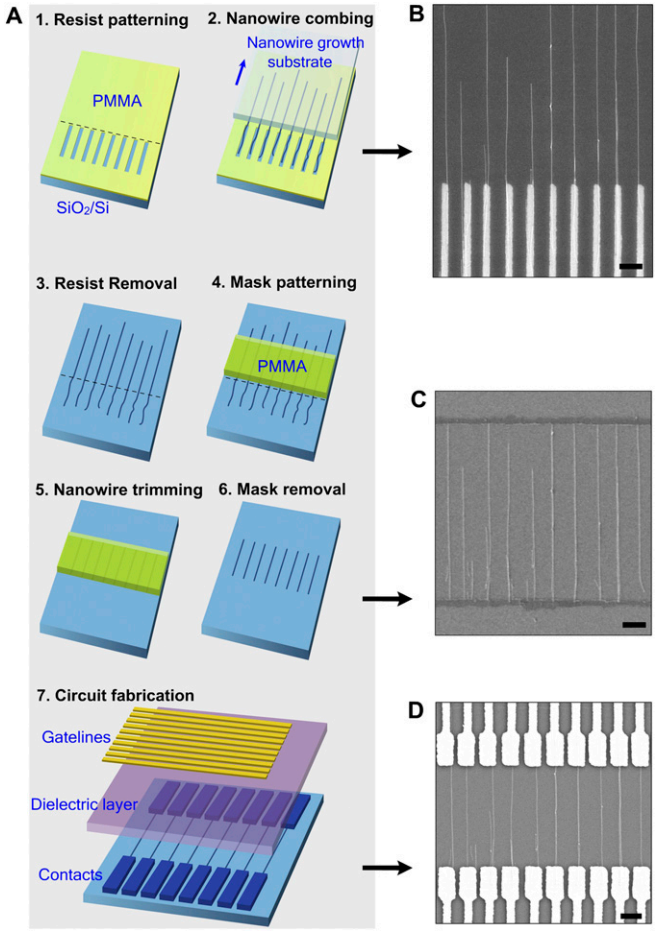


Fig. S1. Circuit fabrication. (*A*) Schematics of the deterministic fabrication flow. (Steps 1 and 2) Nanowire assembly is carried out using the deterministic nanocombing technique (1), with the details described in *Materials and Methods*. The dashed black line indicates the interface between the anchoring sites (blue stripes) and combing surface [yellow, poly(methyl methacrylate) (PMMA)]. (Step 3) The PMMA layer was subsequently removed by acetone vapor without disturbing the nanowire positions. The dashed black line indicates the position of the original interface between the anchoring sites. (Steps 4–6) Trimming process to yield deterministic nanowire array. First, a sacrificial mask (400 nm PMMA 950-C2) was defined and aligned to the anchoring–combing interface (step 4). Second, the unprotected portions of the nanowires were removed by reactive ion etching (step 5). Third, the PMMA mask was then removed in acetone (step 6). (Step 7) The subsequent fabrication of the device arrays. First, source/drain contacts (Cr/Ni 1/40 nm) were defined by mapping sets of contact patterns to the initial anchoring stripe positions without registration to nanowires. This approach contrasts the typical bottom–up electronic circuit fabrication methodology where each nanowire must be individually identified and a contact registered to its position (2). Second, Al_2O_3–ZrO_2–Al_2O_3 (2–5–5 nm) dielectric layers were deposited by atomic-layer deposition. Third, arrays of gate lines (Cr/Au, 4/65 nm) were defined by electron beam lithography. (*B*) SEM image of a typical nanocombed Ge/Si nanowire array, corresponding to the fabricated device array in Fig. 1*D*. (*C*) SEM image of the trimmed Ge/Si nanowire array. (*D*) SEM image of the Ge/Si nanowire array with defined source and drain contacts. (Scale bar, 1 μm in *B*–*D*.)

1. Yao J, Yan H, Lieber CM (2013) A nanoscale combing technique for the large-scale assembly of highly aligned nanowires. *Nat Nanotechnol* 8(5):329–335.
2. Yan H, et al. (2011) Programmable nanowire circuits for nanoprocessors. *Nature* 470(7333):240–244.

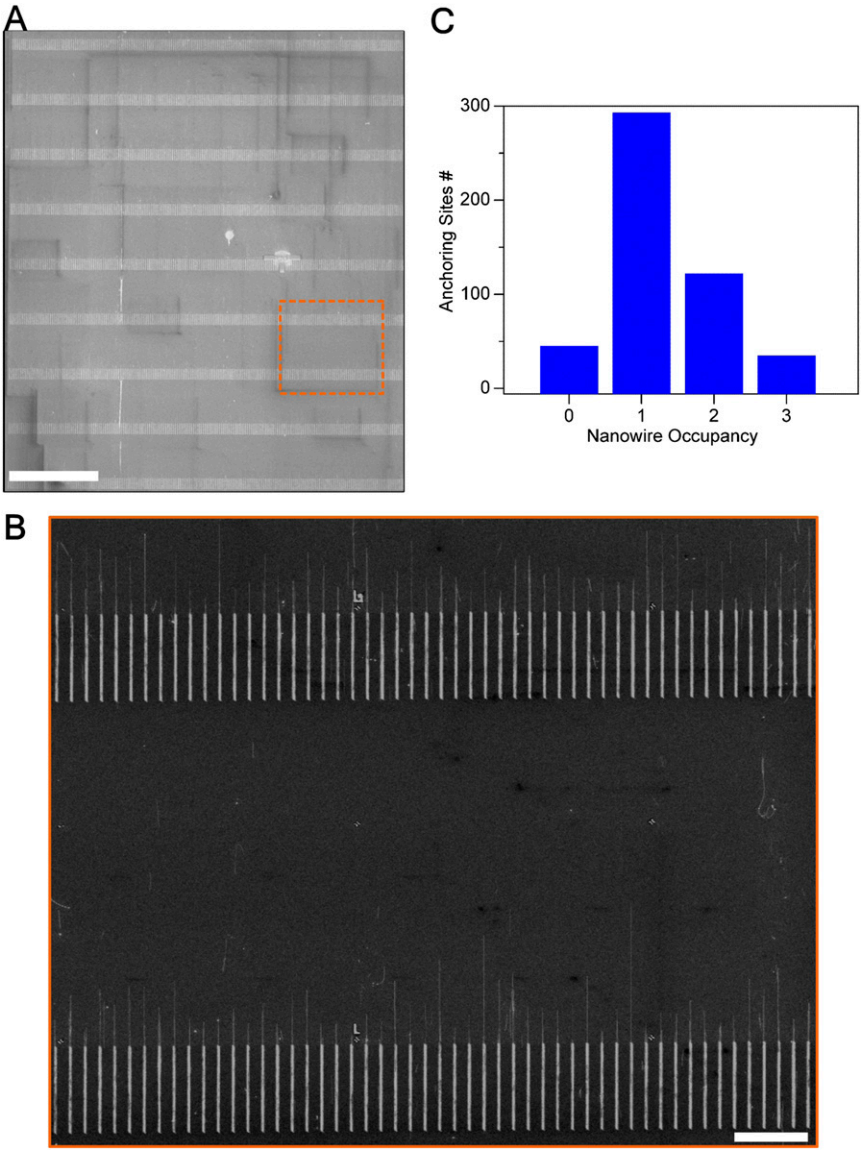


Fig. S2. Deterministic nanocombing. (*A*) SEM image of Ge/Si nanowire arrays assembled by deterministic nanocombing on a Si/SiO_2 surface covering an area of ~0.5 × 0.6 mm^2. (Scale bar, 100 μm.) (*B*) Zoomed-in SEM image of the assembled Ge/Si nanowire arrays indicated by the orange dashed region in *A*. (Scale bar, 10 μm.) (*C*) Nanowire occupancy statistics. For 496 anchoring sites equally distributed in *A*, 293 (~59%) were single-nanowire sites, 122 (~25%) were double-nanowire sites, and 45 (~9%) were vacant sites. The statistics are based on nanowires with a combing length >2 μm.

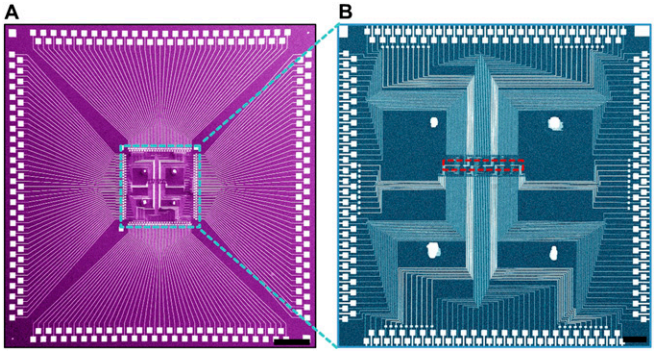


Fig. S3. Fabricated chip. (*A*) SEM image of the final chip having 204 contact pads on the outer periphery of the chip. The pads match the pins of a probe card that is connected to the test system. (Scale bar, 500 μm.) The metal pads and fan-in interconnect lines appear bright in the image. (*B*) SEM image of the inner layout of the fabricated chip as indicated in the dashed box in *A*. The red dashed box region corresponds to the three-tile circuit shown in Fig. 1*E*. (Scale bar, 100 μm.)

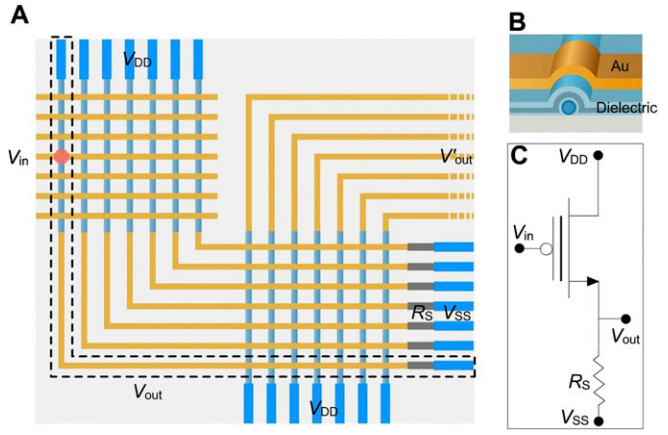


Fig. S4. Logic tile and programmable transistor node. (*A*) Schematic of the logic tile that corresponds to the tiles in Fig. 1*B*. The logic input, V_{in}, is fed to the first array (upper left) and its output, V_{out}, serves as the input to the second array (lower right) for the final output of the tile, V'_{out}. Here, V_{DD}, V_{SS}, and R_S represent the drain, source voltages, and load resistors, respectively. The dashed area delineates the testing unit for a single transistor node (red dot). (*B*) Cross-section schematic of each transistor node, which consists of a Ge/Si nanowire covered by a trilayer Al_2O_3–ZrO_2–Al_2O_3 dielectric and a top Au electrode. The trilayer dielectric layer serves similarly as a float gate (1, 2), such that electron-rich or electron-depleted configuration can be resulted to modulate the threshold voltage of the transistor to be in an inactive or active state. (*C*) The equivalent circuit (a programmable inverter) to single transistor node (red dot) in *A*. This circuit also corresponds to the V_{in}–V_{out} relationship (V_{DD} = 2 V, V_{SS} = 0 V) shown in Fig. 2*A*.

1.Yan H, et al. (2011) Programmable nanowire circuits for nanoprocessors. *Nature* 470(7333):240–244.
2. Liu J, Wang Q, Long S, Zhang M, Liu M (2010) A metal/Al2O3/ZrO2/SiO2/Si (MAZOS) structure for high-performance non-volatile memory application. *Semicond Sci Technol* 25(5): 055013.

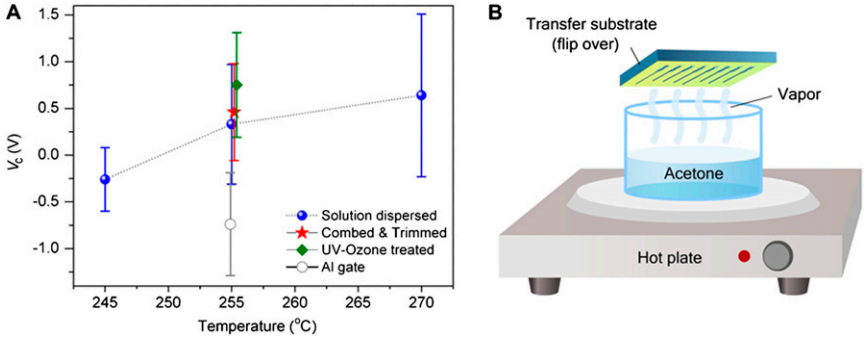


Fig. S5. Control of threshold voltage. (*A*) The circuit threshold voltage V_c (at V_d = 1 V) for the active Ge/Si transistor nodes from different control tests. The charge-trapping transistor devices all adopt the same structure as described in the main text, with the gate line (Cr/Au, 4/65 nm) width of 200 nm. First, a trend of reduction in the V_c was observed with the decrease of growth temperature for the Ge core (blue dots). Second, for nanowires with the Ge core grown at a fixed temperature of 255 °C [the ones used for the construction of nanoelectronic finite-state machine (nanoFSM)], the nanocombing and trimming processes involved in device-array fabrication (*Materials and Methods*) had little effect on V_c (0.46 ± 0.52 V, red star), compared with the value (0.33 ± 0.64 V) obtained from analysis of single-nanowire devices prepared by solution dispersion on a substrate (without nanocombing and trimming steps). However, resist removal (Fig. S1 *A*, *3*) by UV ozone (120 °C, 15 s) does result in an increase in the V_c (0.75 ± 0.56 V, green diamond), which is unfavorable to input/output (I/O) matching. Therefore, the resist, which serves as the combing layer, was removed in acetone vapor; this method did not perturb the combed nanowires and did not adversely affect V_c. In addition, V_c can be reduced further by using Al gate lines (–0.74 ± 0.55 V, gray circle). (*B*) Schematic of the resist removal by acetone vapor (Fig. S1 *A*, *3*).

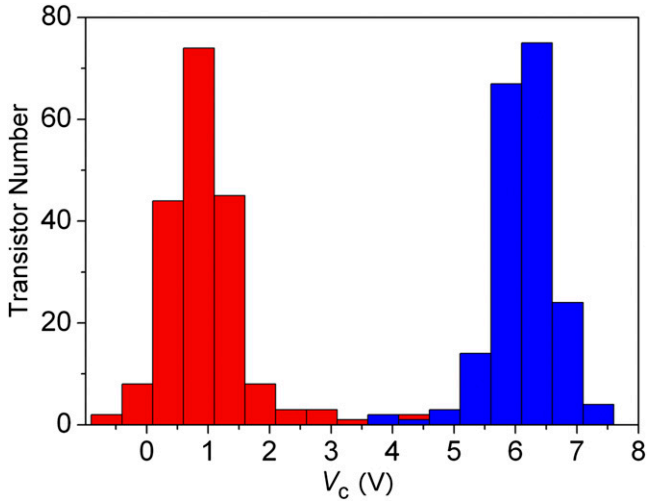


Fig. S6. Statistics of V_c. It features the V_c from both active (red) and inactive (blue) states (at V_d = 2 V) from the 190 transistor nodes shown in Fig. 2*B*.

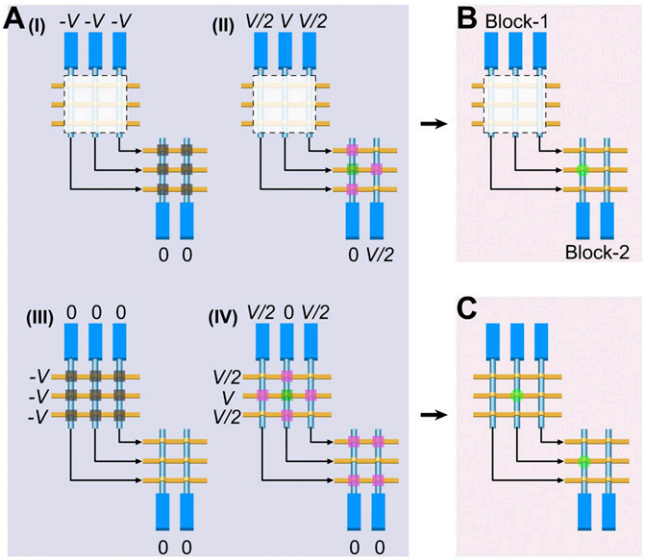
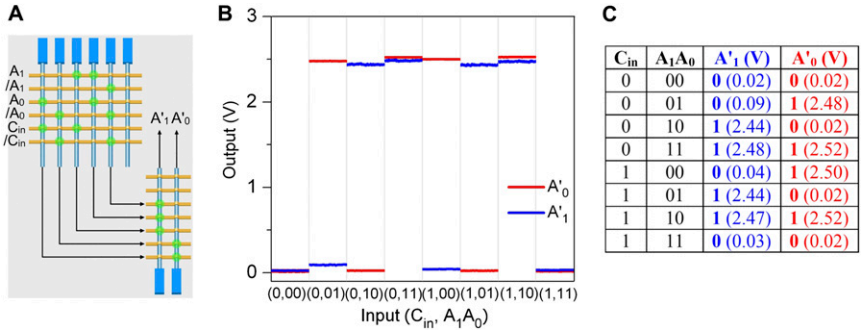


Fig. S7. Programming scheme for the logic tiles. The programming scheme is illustrated in a simplified tile structure, with 3 × 3 transistor nodes in block 1 and 2 × 3 in block 2. This scheme is expandable to tiles with arbitrary size and number of transistor nodes as in our work. (*A*) Consecutive steps for programming the selected transistor nodes to be active in both blocks in the tile. The square box at each transistor node indicates voltage difference between the gate line and nanowire during the programming, with dark, green, and magenta indicating the difference of –*V*, *V*, and *V*/2, respectively. For the actual programming voltage used (*V* = –9 V for 5 s), a –*V* and *V* difference can program the node to be inactive and active, respectively, whereas a *V*/2 difference does not alter the state. The dashed white box indicates that the programmed state in the block 1 is presently not relevant to the final state. (*B*) The intermediate programmed state of block 2, with the circled green dot indicating the programmed active state in the node. (*C*) The final programmed state of the tile (target programming state). The programming process starts from block 2. First, all of the nanowires (source and drain) in block 1 are applied –*V* with all of the nanowires in block 2 grounded, which maps the entire block 2 to be inactive (*A*, *I*). Then for the selected node, the nanowire in block 1 connecting to the gate line of this node is applied *V* with the corresponding nanowire in block 2 grounded; the rest of the nanowires in block 1 and block 2 are all applied *V*/2 (*A*, *II*). In this manner, a voltage difference *V* is produced at the selected node in block 2, with the rest of the nodes having voltage difference of either *V*/2 or 0. Therefore, only the selected node is programmed to be active (as shown in *B*). Similarly, for the subsequent programming of block 1, all of the gate lines in block 1 are applied –*V* with all of the nanowires in the tile grounded to map the entire block 1 inactive (*A*, *III*). Then for the selected node, the corresponding gate line and nanowire are applied *V* and 0, respectively; the rest of the gate lines and nanowires in block 1 are applied *V*/2 with the nanowires in block 2 grounded (*A*, *IV*). In this way, the selected node is applied a voltage difference of *V*, with the rest of the nodes in the entire tile having a voltage difference no larger than *V*/2. Therefore, the selected node in block 1 is programmed to be active, without altering the previously programmed states in block 2 (as shown in *C*). Note that for multiple nodes to be programmed, the programming can be done sequentially for each gate line, and the multiple nodes sharing the same gate line in the same block can be programmed simultaneously.



C_{in}	A_1A_0	A'_1 (V)	A'_0 (V)
0	00	**0** (0.02)	**0** (0.02)
0	01	**0** (0.09)	**1** (2.48)
0	10	**1** (2.44)	**0** (0.02)
0	11	**1** (2.48)	**1** (2.52)
1	00	**0** (0.04)	**1** (2.50)
1	01	**1** (2.44)	**0** (0.02)
1	10	**1** (2.47)	**1** (2.52)
1	11	**0** (0.03)	**0** (0.02)

Fig. S8. Logic outputs of the half adder. The half adder constitutes the first tile in the FSM circuit in Fig. 1*B*. (*A*) Schematic of the programmed circuit, with A_1A_0, C_{in}, and $A'_1A'_0$ representing the 2-bit input, 1-bit input, and 2-bit output, respectively. The green dots at cross-points highlight nodes programmed to the active state. (*B*) The complete logic outputs with respect to different inputs (C_{in}, A_1A_0). The logic inputs 0 and 1 had values of 0 and 2.4 V, respectively, and V_{dd} = 2.6 V. (*C*) The corresponding truth table of the half adder. The logic outputs of 0 and 1 show an experimental range of 0–0.1 V and 2.4–2.5 V, respectively, thus demonstrating strict I/O matching.

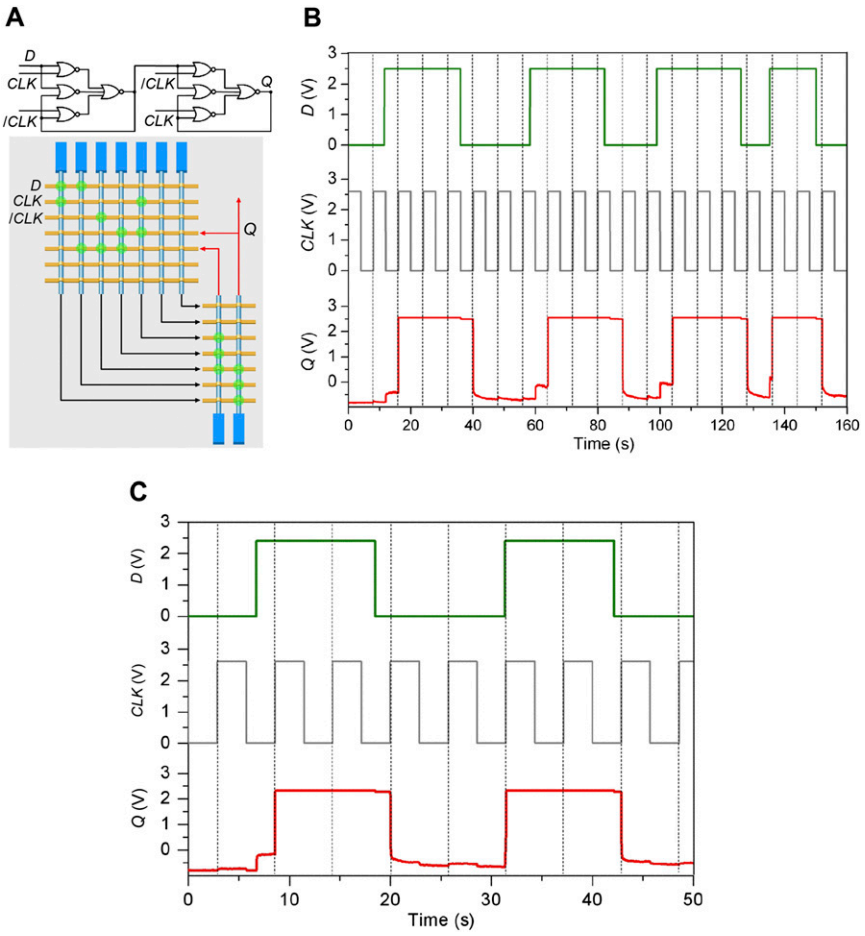


Fig. S9. D flip-flop (DFF) circuit and logic output. (*A*) Schematic of the logic (*Upper*) and physical tile circuit design (*Lower*) of the DFF that serves as the register elements in the FSM circuit. The green dots indicate the active transistor nodes. (*B*) Measurement of Q (V) with respect to D and clock (CLK) signals demonstrates that Q is consistently changed to new values of D with the rising edge of CLK, whereas the circuit holds or locks its state at other times, and that the output Q (2.55 V) matches closely the input D (2.50 V) and CLK (2.60 V). (*C*) Stability of the programmed DFF circuit. Logic output from the same circuit after 10 h in ambient environment without reprogramming. The output exhibits no obvious degradation during this time period. Degradation of the output was observed beyond 15 h, which is largely due to changes in individual transistor nodes (e.g., by moisture). We expect that hermetic sealing/passivation of the circuit, which is standard for conventional top–down fabricated circuits, will resolve this issue and substantially improve the long-term stability of our programmable nanowire circuits.