Supplementary Information

Enabling an Integrated Rate-temporal Learning Scheme on Memristor

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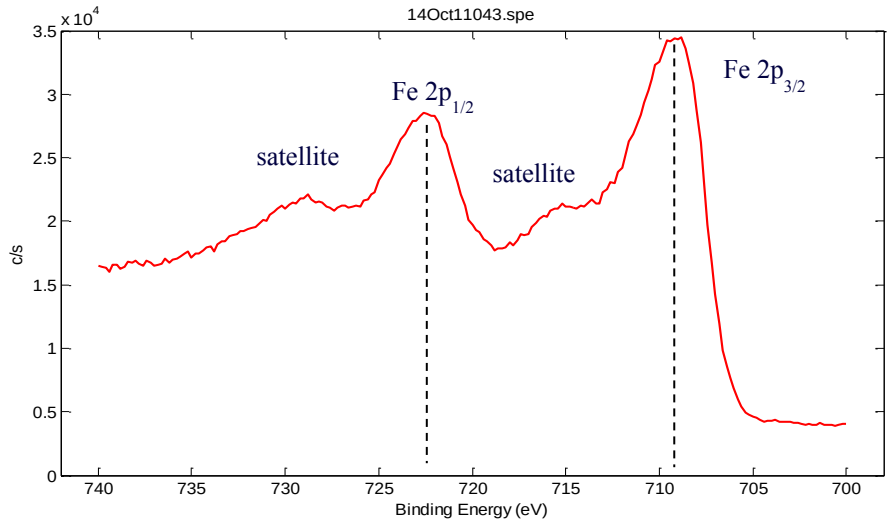
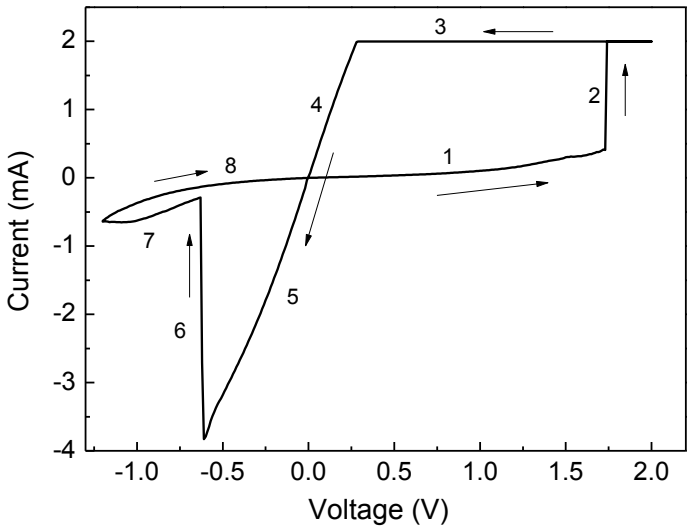
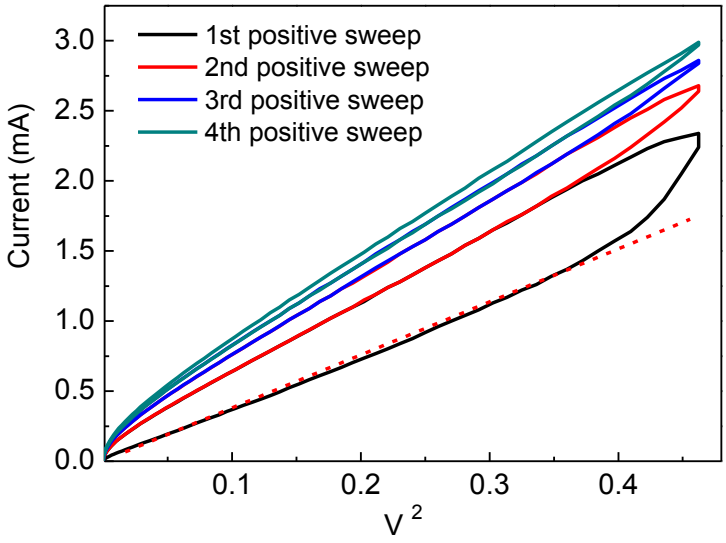


Supplementary Figure S1: XPS spectra of iron element from switching film. The core level of Fe 2P 3/2 locates at 708.5 eV, corresponding to Fe^{2+} species[1]. This indicates that the majority compound inside the iron oxide switching film is FeO. This result is consistent with the atomic ratio of Fe over O (1: 1.14). The number of oxygen atoms is slightly higher than that of iron atoms.

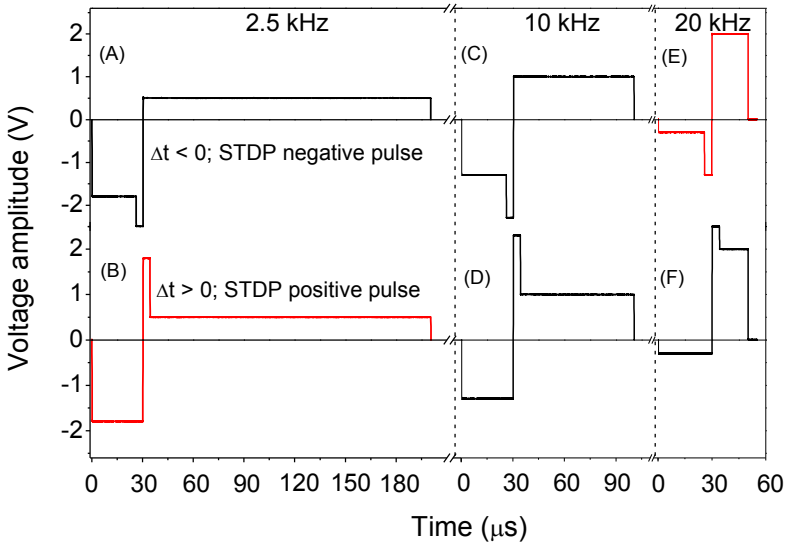


Supplementary Figure S2: An illustration of the electroforming process required by the iron oxide memristor. The electroforming process is conducted by sweeping the positive voltage from low to high slowly. During the sweeping, the current flowing through the memristor was clamped to 2 mA. The suddenly jump in the current (segment 2) indicates a generation of conduction filament path inside the switching material. The reset process is conducted by applying the opposite voltage bias without the current clamp. At -0.75V, the current sharply reduces (segment 6). It is believed that this backward jumping is caused by the block of the filament path. After the reset process, the analog memristor is formed. The memristor is working at the filament rupture states, which is different from other reports where the electroforming process is not involved[2-5].



Supplementary Figure S3. The current-voltage (I-V) curves during the continuously positive DC sweeping. At the low electric field, there is a linear relationship between the current and square

of voltage. This relationship implies a space-charge-limited-current (SCLC) conduction mechanism[6].



Supplementary Figure S4: An illustration of the overlapping effect between incoming neural spikes and STDP pulses at different frequencies.

Figure 4(d) indicates that, when incoming neural spikes fire at 2.5 kHz, the memristor conductance always decreases (LTD); when incoming neural spikes fire at 20 kHz, the memristor conductance always increases (LTP). These conclusions are in agreement with the trend of SRDP drawn from Fig. 3(d) regardless of the STDP input. If the polarity of the integrated STDP pulse has the same effect as SRDP, it will definitely follow the trend of SRDP. On the other hand, if the polarity of STDP pulse is contrary to the effect of SRDP, the situation becomes complicated and requires careful analysis.

Before the analysis, there is some testing information that needs to be addressed. The voltage drop in the memristor was clamped to 2.5V to avoid any device breakdown. The amplitudes of

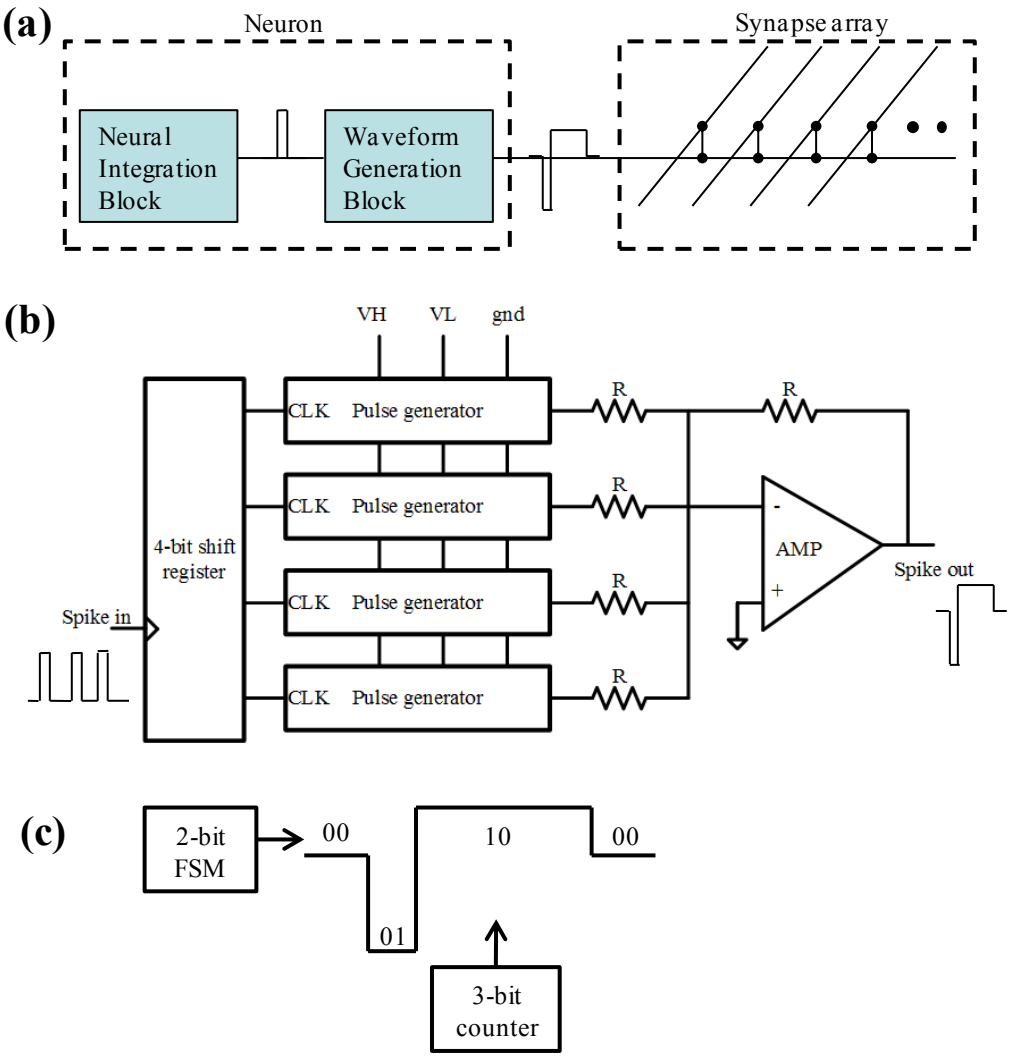
STDP pulses, as shown in Fig. 4(a), was configured to 0.7, 0.8, 0.9, 1.0, -1.3, -0.9, -0.7, -0.6 V from left to right, respectively. According to the STDP operation scheme addressed in Fig. 4(a) and Fig. 4(b), only one pulse will be selected during the integration with incoming neural spikes. For the sake of simplicity, only the conditions of the highest amplitude STDP pulse will be discussed in this document (1V & -1.3V), as shown in supplementary Fig. S4.

In plot (B) of supplementary Fig. S4, the negative amplitude of incoming neural spikes (-1.8V) is much higher than the positive amplitude (0.5V). The overall effect of low frequency incoming neural spikes decreases the conductance (LTD). When positive STDP pulse overlaps with incoming neural spikes, the integrated amplitude of positive voltage is increased to 1.8V, which holds the same value of amplitude as the negative pulse. However, the pulse width of integrated positive pulse caused by STDP is much shorter than that of the negative pulse. Therefore, the final effect of SRDP + STDP decreases the conductance (LTD, the same trend of SRDP at low frequency).

The other contradictive condition is shown in plot (E) of supplementary Fig. S4. The high frequency incoming neural spikes increase the conductance (LTP) because of the higher amplitude of positive pulses (2.0V). The amplitude of integrated negative pulse is increased from -0.3V to -1.3V when it overlaps with the negative STDP pulse. Because both the amplitude and pulse width of integrated negative pulse are smaller than that of the positive pulse, the final effect of SRDP + STDP increases the conductance (LTP, the same trend of SRDP at high frequency).

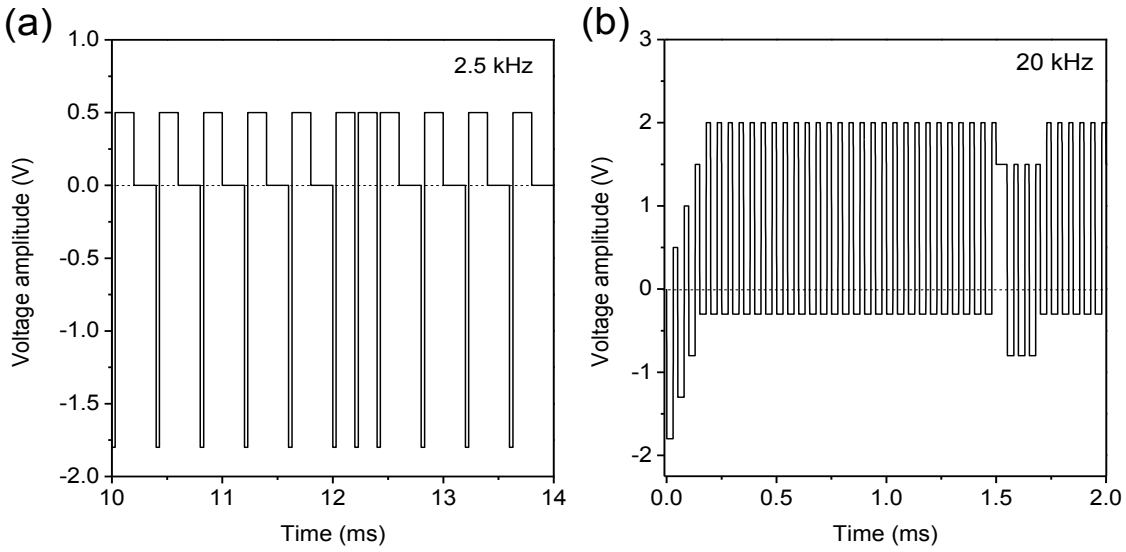
When incoming neural spikes fire at a moderate frequency, the amplitudes of positive and negative spikes are comparable. Therefore, the pulse integrated with STDP becomes extrusive. The final effect of SRDP + STDP will be dominated by STDP.

In summary, when STDP pulses are integrated with incoming neural spikes at low frequency or high frequency region, the effect of STDP pulses is covered by the incoming spikes. Therefore, SRDP effect dominates the two regions regardless of the STDP input, which is consistent with the *in-vivo* experiments[7-10].



Supplementary Figure S5: (a) An illustration of waveform generation block in neural network. (b) A schematic architecture diagram of the waveform generation block for the SRDP implementation. The circuit consists of one 4-bit shift registers, four pulse generators, five resistors and one operational amplifier. The input spikes come directly from the standard neuron output. (c) A fully digital realization of the pulse generator. It consists of one 2-bit finite-state machine (FSM) to achieve 3 levels of voltage output (VH, VL & GND) and one 3-bit counter to achieve flexible pulse width.

The waveform generation block can be regarded as one part of neuron and it will not affect the architecture of synapse array, as shown in Supplementary Fig. S5. The realization circuit of SRDP inputting waveform is proposed, as shown in Supplementary Fig. S5 (b). The block can be realized by 24 flip-flops, 1 amplifier, 5 resistors, and a few combinational logics. The transistors may use the minimum feature size design that consumes small areas. This circuit block is calculated to occupy comparable area size as the STDP learning block proposed by Seo, Brezzo *et al*[11]. Furthermore, the pulse generator shown in Supplementary Figure S5 (b) can be further optimized by using capacitors to reduce the area consumption. In addition, because the number of synapses in human brain is 1000 times greater than the number of neurons, the area size of synaptic array is expected to dominate the neuromorphic die size[11]. Therefore, the extra circuit used to implement the SRDP learning rule will not alter the neuromorphic chip size too much.



Supplementary Figure S6: An example of extra spike (a) and missing spike (b) in incoming neural spike-train. The waveforms have been treated by Waveform Generation Block.

Our proposal of dual coding learning scheme is robust to the variation of the presynaptic input. When the presynaptic firing frequency is slightly varied, or even one spike is missed or is inserted owing to system instability, the learning scheme will tolerate these fluctuations and produce similar results. It is necessary to analyze the case of extra spike at low frequency condition. The effect of having an extra spike in incoming spike-train transformed by Waveform Generation Block is illustrated in Supplementary Fig. S6(a). It is obvious that the negative pulse still dominates the conductance changing direction, which follows the same trend of SRDP at low frequency region (LTD). The other case of missing spike at high frequency condition is also analyzed in Supplementary Fig. S6(b). It is clear that the positive amplitudes are still greater than the negative amplitudes, resulting in an increase of conductance which follows the same trend of SRDP at high frequency region (LTP). In addition, if there is a slight frequency variation, based on the graph of Fig. 3(c), the variation will not change the output result at the low frequency or

high frequency region. Therefore, the customized pulsing scheme we proposed is robust to the spike variations and systematic noise.

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