Supporting Information

Adaptive optoelectronic camouflage systems with designs inspired by cephalopod skins

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1. Preparing the thermochromic composite and measuring its optical characteristics

Preparation of the photodefinable thermochromic composite involved mixing microencapsulated leuco dye (black 47C, LCR Hallcrest) with SU-8 50 (Microchem, USA) at a weight ratio of 1:5 to form a liquid slurry. Microcapsules contain mixtures of leuco dye with a color developer and a low melting point solvent. At low temperatures, the developer and leuco dye form a complex that favors a colored ring-open state. Upon heating, the solvent melts, and the developer and dye dissociate. In this state, the leuco dye favors a colorless, ring-closed configuration. Such transformation occurs at 47 °C in a reversible manner. Figure S1A shows an optical image of the slurry at 22 °C. Heating to a temperature above 47 °C causes the slurry to become transparent. As shown in Fig. S1B, a background picture underneath the slurry is clearly visible at temperatures above 47 °C. Standard procedures for pattering SU-8 yield pixelated arrays of this slurry with thickness defined by the spin-speed. Figures S1C and D provide SEM images of examples. Detailed fabrication steps appear below.

The optical reflectance of the color changeable pixels (Ag/composite dye) was measured using a spectrometer (Cary 5G UV-VIS-NIR) as a function of temperature. A portable thermoelectric heater/cooler (InbS1-031.021, WATRONIX, Inc.) served to control the sample temperature. A thermocouple (Fluke 233, Fluke Corporation) was used to measure the temperature.

Fabrication steps:

1. Mix leuco dye and SU-8 50 at weight ratio of 1:5.
2. Spin-coat the mixture slurry (3000rpm, 30 sec).
3. Pre-bake at 65 °C for 5 min and 95 °C for 20 min.
4. Expose to UV light under a mask aligner (Karl Suss MJB3) at a dose of 1440 mJ/cm^2.
5. Post-bake at 65 °C for 2 min and 95 °C for 5 min.

6. Develop in SU-8 developer (MicroChem, USA) for 6 minutes.
7. Rinse in isopropyl alcohol (IPA) and deionized (DI) water.

2. Fabricating the diode array and measuring its electrical characteristics

Figure S2A shows an exploded schematic illustration of the layout of the Si, metal and polyimide (PI) layers associated with a single pixel in the heater array. The major steps in the fabrication include retrieving a thin (1.25 μm) crystalline film of Si with pre-defined patterns of doping from a silicon-on-insulator (SOI) wafer followed by transfer printing onto a thin polyimide (PI) substrate, and then applying layers for metallization and passivation, as outlined in Figs. S3 and 4. A thin layer of gold eliminates the potential for crosstalk induced by light. Figure S2B shows the planar structure and design of the Si heater; the small dots correspond to holes introduced into the Si to facilitate chemical etching for release. The measured I-V curves at different temperatures appear in Fig. 2B. Figure S2C shows an optical image of a 16×16 array of unit cells. Individual addressing is achieved without affecting the neighborhood pixels, as evidenced by the IR image (QFI InfraScope II) of Fig. S2D. Here, the background temperature was set to 30 °C, to facilitate IR imaging. Detailed fabrication steps are as follows.

Fabrication steps:

Defining alignment markers

1. Clean 1.25 μm SOI wafer (acetone, isopropyl alcohol (IPA), deionized (DI) water).
2. Pattern photoresist (PR; Clariant AZ5214, 3000 rpm, 30 sec) with 365 nm optical lithography (Mask #1: Alignment marker).
3. Etch Si by RIE (50 mTorr, 40 sccm SF_6, 100 Watt, 1 min).
4. Remove PR by acetone and clean by piranha for 10 min.

Performing p+ doping

5. Deposit 900 nm SiO_2 by plasma enhanced chemical vapor deposition (PECVD; PlasmaTherm SLR).
6. Treat with hexamethyldisilazane (HMDS) for 2 min.
7. Pattern PR (Mask #2: P doping).
8. Bake at 110°C for 5 min.
9. Etch SiO_2 in buffered oxide etchant (BOE, 6:1) for 1.5 min.
10. Remove PR by acetone and clean by piranha for 10 min.
11. Expose to a boron doping source at 1000°C for 30 min.
12. Clean the processed wafer (concentrated (49%) HF 2 min, piranha 10 min, BOE 1 min).

Performing n+ doping

13. Deposit 900 nm SiO_2 by PECVD.
14. Treat with HMDS for 2 min.
15. Pattern PR (Mask #3: N doping).
16. Bake at 110°C for 5 min.
17. Etch SiO_2 in buffered oxide etchant (BOE, 6:1) for 1.5 min.
18. Remove PR by acetone and clean by piranha for 10 min.
19. Expose to a phosphorus doping source at 1000°C for 10 min.
20. Clean the processed wafer (HF 2 min, piranha 10 min, BOE 1 min).

Releasing the top Si from SOI

21. Pattern PR (AZ 5214) (Mask #4: Releasing hole 1).
22. Etch Si by RIE (50 mTorr, 40 sccm SF_6, 100 Watt, 3.5 min).
23. Remove PR by acetone and clean by piranha for 10 min.
24. Etch buried oxide layer in concentrated HF for 45 min.

25. Rinse and clean the processed wafer in DI wafer.

Retrieving the Si film

26. Bring a 6 mm thick PDMS (weight ratio of base: curing agent=10:1) stamp into contact with the Si.

27. Peel the stamp back to lift the Si film from SOI onto the stamp.

Preparing the carrier wafer

28. Spin cast polyimide (PI, poly(pyromellitic dianhydride-co-4,4'-oxydianiline) (4000 rpm, 30 sec) onto a 3"×2" glass slide.

29. Anneal at 150 °C for 10 min.

30. Anneal at 250 °C for 60 min in an N_2 atmosphere.

31. Deposit Cr/Au (5/300 nm) by electron beam evaporation (AJA International).

Transfer printing the Si film

32. Spin coat the carrier wafer with PI (4000 rpm, 30 sec).

33. Bake at 110 °C for 30 sec.

34. Bring the stamp with Si film on its surface into contact with the carrier wafer.

35. Bake at 110 °C for 30 sec.

36. Remove the PDMS stamp, leaving the Si on carrier wafer

37. Anneal at 150 °C for 10 min.

38. Anneal at 250 °C for 60 min in N_2 atmosphere.

Isolating the PIN heaters

39. Pattern PR (Mask #5: Diode isolation).

40. Etch Si by RIE (50 mTorr, 40 sccm SF_6, 100 Watt, 3.5 min).

41. Remove PR by acetone.

Patterning metal to block light

42. Pattern PR (AZ 4620, 3000 rpm, 30 sec) (Mask #6: Back light blocking metal).

43. Etch PI by RIE (MARCH, 300 mTorr, 150 Watt, 10 min).

44. Wet etch exposed Au/Cr for 54/7 sec.

45. Remove PR by acetone.

Defining the via hole to the p contact

46. Spin coat PI (4000 rpm, 30 sec).

47. Anneal at 150°C for 10 min.

48. Anneal at 250°C for 60 min in N_2 atmosphere.

49. Pattern PR (AZ 4620) (Mask #7: P via hole).

50. Etch PI by RIE (MARCH, 300 mTorr, 150 Watt, 10 min).

51. Remove PR by acetone.

Defining the metal for the p contact

52. Deposit Cr/Au (5/300 nm) by DC sputtering (AJA International).

53. Pattern PR (AZ 5214) (Mask #8: P metal).

54. Wet etch exposed Au/Cr for 54/7 sec.

55. Remove PR by acetone.

Defining the via hole to the n contact

56. Spin coat PI (4000 rpm, 30 sec).

57. Anneal at 150°C for 10 min.

58. Anneal at 250°C for 60 min in N_2 atmosphere.

59. Pattern PR (AZ 4620) (Mask #9: N via hole).

60. Etch PI by RIE (MARCH, 300 mTorr, 150 Watt, 20 min).

61. Remove PR by acetone.

Defining the metal for the n contact

62. Deposit Cr/Au (5/300 nm) by DC sputtering (AJA International).

63. Pattern PR (AZ 5214) (Mask #10: N metal).

64. Wet etch exposed Au/Cr for 54/7 sec.

65. Remove PR by acetone.

Depositing PI encapsulation

66. Spin coat PI (4000 rpm, 30 sec).

67. Anneal at 150°C for 10 min.

68. Anneal at 250°C for 60 min in N_2 atmosphere.

Releasing the device

69. Deposit 150 nm SiO_2 by PECVD.

70. Treat with HMDS for 2 min.

71. Pattern PR (Mask #11: Releasing hole 2).

72. Etch SiO_2 by RIE (50 mTorr, 40:1.2 sccm CF4:O2, 150 Watt, 8.5 min).

73. Remove PR by acetone.

74. Release device in BOE (6:1).

3. Fabricating the photodetector array and measuring its characteristics

Figure S7A shows an exploded schematic illustration of the layout of the Si, metal and PI layers associated with a single unit cell in the photodetector array. The major steps in the fabrication are similar to those for the heater array. Every unit cell in the photodetector array includes a photodiode and blocking diode constructed in a back-to-back configuration to eliminate crosstalk in passive matrix readout. In addition, the light sensitive intrinsic region of

the blocking diode is covered by a layer of Cr/Au to eliminate any response to light. Figure S7B shows the planar structure design of the photodetector. An optical image of the thin photodetector array appears in Fig. S7C. Detailed fabrication steps are as follows.

Fabrication steps:

Defining alignment markers

1. Clean 1.25 μm SOI wafer with acetone, IPA and DI water.
2. Pattern PR (AZ5214) (Mask #1: Alignment marker).
3. Etch Si by RIE (50 mTorr, 40 sccm SF6, 100 Watt, 1 min).
4. Remove PR by acetone and clean by piranha for 10 min.

Performing p+ doping

5. Deposit 900 nm SiO_2 by PECVD.
6. Treat with HMDS for 2 min.
7. Pattern PR (Mask #2: P doping).
8. Bake at 110°C for 5 min.
9. Etch SiO_2 in BOE (6:1) for 1.5 min.
10. Remove PR by acetone and clean by piranha for 10 min.
11. Expose to a boron doping source at 1000°C for 30 min.
12. Clean the processed wafer (HF 2 min, piranha 10 min, BOE 1 min).

Performing n+ doping

13. Deposit 900 nm SiO_2 by PECVD,
14. Treat with HMDS for 2 min.
15. Pattern PR (Mask #3: N doping).
16. Bake at 110°C for 5 min.

17. Etch SiO_2 in buffered oxide etchant (BOE, 6:1) for 1.5 min.

18. Remove PR by acetone and clean by piranha for 10 min.

19. Expose to a phosphorus doping source at 1000°C for 10 min.

20. Clean the processed wafer (HF 2 min, piranha 10 min, BOE 1 min).

Releasing top Si from SOI

21. Pattern PR (AZ 5214) (Mask #4: Releasing hole 1).

22. Etch Si by RIE (50 mTorr, 40 sccm SF_6, 100 Watt, 3.5 min).

23. Remove PR by acetone and clean by piranha for 10 min.

24. Etch buried oxide layer in concentrated HF for 45 min.

25. Rinse and clean the processed wafer in DI wafer.

Retrieving the Si film

26. Bring a 6 mm thick PDMS (weight ratio of base: curing agent=10:1) stamp into contact with the Si.

27. Peel the stamp back to lift the Si film from SOI onto the stamp.

Preparing the carrier wafer

28. Spin cast PI (4000 rpm, 30 sec) onto a 3”×2” glass slide

29. Anneal at 150°C for 10 min.

30. Anneal at 250°C for 60 min in N_2 atmosphere.

31. Deposit Cr/Au (5/300 nm) by electron beam evaporation.

Transfer printing the Si film

32. Spin coat the carrier wafer with PI (4000 rpm, 30 sec).

33. Bake at 110°C for 30 sec.

34. Bring the stamp with Si film on onto contact with the carrier wafer.

35. Bake 110°C for 30 sec.

36. Retrieve the PDMS stamp, leaving the Si on carrier wafer.

37. Anneal at 150°C for 10 min.

38. Anneal at 250°C for 60 min in N_2 atmosphere.

Isolating the photodetectors

39. Pattern PR (Mask #5: Photodetector isolation).

40. Etch Si by RIE (50 mTorr, 40 sccm SF_6, 100 Watt, 3.5 min).

41. Remove PR by acetone.

Patterning metal to block light

42. Pattern PR (AZ 4620, 3000 rpm, 30 sec) (Mask #6: Back light blocking metal).

43. Etch PI by RIE (MARCH, 300 mTorr, 150 Watt, 10 min).

44. Wet etch exposed Au/Cr for 54/7 sec.

45. Remove PR by acetone.

Defining via 1

46. Spin coat PI (4000 rpm, 30 sec).

47. Anneal at 150°C for 10 min.

48. Anneal at 250°C for 60 min in a N_2 atmosphere.

49. Pattern PR (AZ 4620) (Mask #7: Via hole 1).

50. Etch PI by RIE (MARCH, 300 mTorr, 150 Watt, 10 min).

51. Remove PR by acetone.

Depositing and patterning metal 1

52. Deposit Cr/Au (5/300 nm) by DC sputtering (AJA International).

53. Pattern PR (AZ 5214) (Mask #8: Metal 1).

54. Wet etch exposed Au/Cr for 54/7 sec.

55. Remove PR by acetone.

Patterning via 2

56. Spin coat PI (4000 rpm, 30 sec).

57. Bake at 150 °C for 10 min.

58. Anneal at 250 °C for 60 min in N_2 atmosphere.

59. Pattern PR (AZ 4620) (Mask #9: Via hole 2).

60. Etch PI by RIE (MARCH, 300 mTorr, 150 Watt, 20 min).

61. Remove PR by acetone.

Depositing and patterning metal 2

62. Deposit Cr/Au (5/300 nm) by DC sputtering (AJA International).

63. Pattern PR (AZ 5214) (Mask #10: Metal 2).

64. Wet etch exposed Au/Cr for 54/7 sec.

65. Remove PR by acetone.

Depositing PI encapsulation

66. Spin coat PI (4000 rpm, 30 sec).

67. Anneal at 150 °C for 10 min.

68. Anneal at 250 °C for 60 min in N_2 atmosphere.

Opening the bonding pad

69. Cover the device with a 2 mm thick piece of PDMS and expose the bonding pad.

70. Etch the unprotected PI (MARCH, 300 mTorr, 150 Watt, 10 min) to expose the bonding pad.

Releasing the device

71. Deposit 150 nm SiO_2 by PECVD.

72. Treat with HMDS for 2 min.

73. Pattern PR (Mask #11: Releasing hole 2).

74. Etch SiO_2 by RIE (50 mTorr, 40:1.2 sccm CF_4:O_2, 150W, 8.5 min).

75. Remove PR by acetone.

76. Release device in BOE (6:1).

4. Fabricating and assembling the complete system

Assembling the complete system involves multiple steps of functional component fabrication and integration. Detailed fabrication steps are outlined in the following.

Fabrication steps:

Bonding the heater array with thin PDMS

1. Retrieve the thin heater array with a PDMS stamp.
2. Deposit 40 nm SiO_2 by PECVD.
3. Spin coat PDMS (10:1, 500rpm, 1 min) on a glass slide (2”×3”).
4. Bake at 80°C for 10 min.
5. Treat the front surface of the PDMS under a UVO lamp (BHK Inc.) for 5 min.
6. Bond the heater array with the treated PDMS.

Constructing the artificial leucophor and chromatophore pixels

7. Deposit Ag (300 nm) for the white background and heat spreading layer by electron beam evaporation.
8. Pattern PR (AZ 5214) (Mask #1: Ag).
9. Etch exposed Ag by wet etchants for 20 sec.
10. Remove PR by acetone.

11. Pattern the thermochromic composite by spin coating, pre-baking, exposing, post-baking and developing.
12. Clean with isopropyl alcohol (IPA) and deionized (DI) water.

Opening the bonding pad for the heater

13. Cover the device by a rectangular, ring-shaped piece of PDMS (2 mm thick) with a glass slide on top and expose the bonding pad.
14. Etch the unprotected PI (MARCH, 300 mTorr, 150 Watt, 10 min) to expose the bonding pad.
15. Peel off the PDMS with the heater and color changeable pixel array from the glass slide.

Bonding the photodetector array

16. Treat the back surface of the PDMS under a UVO lamp for 5 min.
17. Retrieve the photodetector array with a PDMS stamp.
18. Deposit 40 nm SiO_2 by PECVD.
19. Align and bond the photodetector array to the activated rear surface of the PDMS with all other components on the front side.

5. Optical system and data acquisition

Connecting the pins on a custom printed circuit board (PCB) that is interfaced to the devices, with control electronics and software enables background image acquisition, signal processing, and pulse power signal generation. Electronic diagrams for image acquisition are shown in Fig. S7D. The inputs and outputs, i.e. the columns and rows respectively, are interfaced with the control electronics of NI PXIe-6363(National Instruments). The current responses at an applied bias of 3 V were measured for all the pixels in the 16 x 16 array, used to generate the image results of Fig. S8. Three different light intensities ranging from bright, working to complete darkness served to test the detector arrays. A good range of sensitivity is possible for the

photodetecting pixels, from current responses of 1100~1200 nA at the highest brightness to 0.5~3 nA in the dark state, as shown in Fig. 2C. The greyscale image of Fig. S8A represents the normalized photocurrent intensity map during image acquisition, while the binarized image by choosing the cut-off value of 0.25 was achieved as shown in Fig. S8B. The binarized data were used to control the pulse voltages to supply the heaters, thus to induce color change and pattern matching.

The circuit diagram of the heater array is shown in Fig. S5. Instead of directly interfacing the devices with the PXI control electronics, the heaters were powered using the output of a transistor (MCT2EM-ND, Fairchild Semiconductor Corp.) capable of meeting the power requirements. Figure S6 shows the controlling pulse (3 V) from the PXIe-6723 and the power supply pulse (12 V). The voltage directly applied to the heater pixel is 10.5 V, since there is some voltage drop on the two forward biased junctions from the circuit.

6. Moving background setup and device testing

The changeable background, which was used to verify the camouflaging capabilities, consisted of a backlight and a transparency mask. Specifically, diffusive light from an array of light emitting diodes (MB-BL4X4, Metaphase Technologies, Inc., USA) provided a uniform, white light illumination. The plastic transparency masks consist of various black patterns that block the light. Motion of this mask relative to the device system allowed demonstrations of dynamic change of the patterns. The schematic cartoons with various patterns are shown in Fig. 4. The whole setup was built on a stage to allow temperature control, with a set point of T_0.

7. Thermal analysis

FEM, specifically the continuum element DC3D8 in the ABAQUS software(1), was used to study the temperature distribution in the device. The substrate, made of PI (thickness 9.95 μm) and PDMS (thickness 100 μm), was supported by a glass slide (thickness 1100 μm). As shown in Fig. S16A, the device consists of 16 × 16 pixels on the substrate, where each pixel consists of a layer of composite dye (thickness 65 μm) and Ag (thickness 0.3 μm) (Fig. S16B). The pixels have spacing of 100 μm, and in-plane dimensions of 820 × 820 μm^2 with four corners (each 110 × 110 μm^2) removed (Fig. S16C). For each pixel, the PI layer underneath contains the (Si) heater and the gold layer with dimensions of 640 × 640 × 1.25 μm^3 and 720 × 720 × 0.3 μm^3, respectively (Fig. S2B). Figures S16 A and C also show Au interconnects between the heaters. The bottom of the glass slide has a constant temperature 40.5 °C, as in experiments. The entire top surface, and the lateral surfaces of pixels, have natural convection with the coefficient of heat convection of 5 W/(m^2·K) and air temperature of 20 °C. Figure S16D illustrates the pulsed voltage of U_0 = 10.5 V and duration of t_0 = 17.5 ms in the period of T = 280 ms.

The thermal conductivity, heat capacity, and mass density are 0.2 W/(m·K), 1800 J/(kg·K), and 1200 kg/m^3 for thermochromic dye(2, 3); 371 W/(m·K), 235 J/(kg·K), and 10492 kg/m^3 for silver(4); 0.52 W/(m·K), 1090 J/(kg·K), and 1420 kg/m^3 for PI(5, 6); 160 W/(m·K), 700 J/(kg·K), and 2329 kg/m^3 for silicon(7); 317 W/(m·K), 129 J/(kg·K), and 19280 kg/m^3 for gold(8, 9); 0.18 W/(m·K), 970 J/(kg·K), and 1460 kg/m^3 for PDMS(7); 1.2 W/(m·K), 790 J/(kg·K), and 2700 kg/m^3 for glass(10), respectively.

Figure S17A shows the temperature distribution, obtained by FEM, along the plane of the Si heaters (x direction) as illustrated in Fig. S17B, when all heaters are off except the center one, which receives pulsed power, and the temperature fluctuation is stabilized. The maximum

temperature increase in all heaters without power is only 3% of that in the center heater, which clearly demonstrates that the heat is well confined. Figure S18 shows that, during thermal fluctuation due to pulsed power, the maximum temperature on the surface of the heated pixel ranges from 57 to 65 °C. The temperature along *z* direction (normal to the surface) given in Fig. S19 suggests relatively uniform temperature across the thickness of the dye. Figure S20 compares the temperature distributions at the bottom surface of the dye, with and without the Ag layer. With Ag, the temperature is more uniform than that of the case of without Ag layer.

8. Mechanical analysis

This analysis of strains and stresses in the device during bending by FEM upon application of a load along the *x* and *y* directions is performed. The thermochromic composite dye and PDMS are modeled as three-dimensional solids. The multilayer structures consist of metal, silicon and PI, are modeled as shells. The Young's modulus and Poisson's ratio are 130 GPa and 0.27 for silicon, 78 GPa and 0.44 for Au, 2 MPa and 0.49 for PDMS and 2.5 GPa and 0.34 for PI, respectively. Figure S12B captures the maximum strain in the silicon for bending to different bending radii.

References

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Supplementary Movie Legends

Movie S1. Experimental thermal movie of camouflaging of a digital pattern "O".

Movie S2. FEM thermal movie of camouflaging of a digital pattern "O".

Movie S3. Movie of dynamic, adaptive pattern recognition and color camouflaging against a moving square background. The video is sped up by 3 times.

Movie S4. Movie of dynamic, adaptive pattern recognition and color camouflaging on a changing background. The video is sped up by 3 times.

Supplementary Figure Legends

Figure S1. (A) Optical image of the black thermochromic slurry at room temperature, ~22°C. (B) Optical image of the slurry at 47°C. At this temperature, the slurry is transparent, thereby a background picture underneath is visible. (C) SEM image of an array of photopatterned thermochromic pixels. (D) SEM image of the top surface of a patterned pixel. (E) Optical image of the pixel arrays (16×16) at room temperature of 22°C. (F) Optical image of the arrays (16×16) at 47°C.

Figure S2. (A) Exploded schematic illustration of the layout of the Si, metal, and PI layers of a single pixel in the heater array. (B) Optical image of the Si diode. The dark dots represent the releasing holes etched through the Si. (C) Optical image of the heater array. (D) Thermal image of the array with one pixel activated. The heat is mostly confined within the area of the activated heater, with minimal changes in neighboring pixels. The background temperature was set to 30°C.

Figure S3. Schematic illustration of the major steps for fabricating flexible devices based on Si nanomembranes. (A) Preparing the device elements by selective doping. (B) Opening holes and undercut etching in concentrated HF. (C) Retrieving the Si from the SOI wafer using a PDMS stamp. (D) Printing the Si onto a glass substrate with a thin layer of PI. (E) Peeling away the stamp to leave the Si on the glass. (F) Patterning the Si and completing the metallization and passivation steps. (G) Releasing the flexible device from the glass.

Figure S4. (A) Optical images of a diode heater with P^+ and N^+ doping regions on an SOI wafer. (B) Optical image of a 1.25 μm thick Si membrane on a PDMS stamp. (C) Optical image of the Si membrane transfer printed onto a glass substrate which was coated with PI. (D) Optical image of a flexible array of diode heater held by a tweezer.

Figure S5. Schematic circuit diagram of a heater array and its external circuits.

Figure S6. Images of representative pulse signals. (A) The green curve is the control signal generated with a program created in Labview. The yellow curve is the output pulse applied to the heater. (B) Magnified image of both curves.

Figure S7. (A) Exploded schematic illustration of the layout of the Si, metal, and PI layers of a single pixel in the photodetector array. (B) Schematic illustration of the photodiode and blocking diode. (C) Optical image of the thin flexible photodetector array folded on a glass slide. (D) Schematic circuit diagram of the photodetector array.

Figure S8. (A) Normalized photocurrent intensity map associated with a digital pattern in the geometry of the text “UIUC MRL”. (B) Corresponding binarized intensity map.

Figure S9. Schematic steps for assembling the entire system. (A) Schematic illustration of a unit cell of the heater array and a thin PDMS substrate, prior to bonding. (B) Illustration of the bonded device. (C) Illustration of the Ag pixel fabricated on the device. (D) Illustration of a unit cell of the thermochromic pixel on top of the Ag pixel and the photodetector to be bonded together. (E) Illustration of the integrated system.

Figure S10. (A) Optical image of the heater array on a PDMS substrate. (B) Optical image of the Ag pixels fabricated on the heater array. (C) Optical image of the heater array and Ag pixels viewed from the backside.

Figure S11. Optical image of the device with ACF cable and custom made PCB with pin connectors.

Figure S12. (A) FEM model of the system, showing a 5×5 array. (B) FEM results of the maximum strain in the Si within the device at different bending radii. The red dots are the results for bending along *x* axis. The blue dots are the results for bending along *y* axis.

Figure S13. (A-H) IR images of the device when one pixel is actuated, as the actuation voltage increases from 5.5 V to 12.5 V, with an increment of 1 V.

Figure S14. (A-D) IR images of the device when 8 pixels (digital pattern of "o") are actuated, as the actuation voltage increases from 8.5V to 11.5V, with the increment of 1V.

Figure S15. (A) IR image of the heater array with one pixel activated at 10.5V. The arrow points to the geometrical center of the pixel. (B) Temperature fluctuation at the center of the pixel. The power was turned on and off at 11 s and 41 s, respectively. (C) Temperature information during the period of 20~30 s, as highlighted by the red dotted rectangular in (B).

Figure S16. (A) FEM model for the thermal analysis. (B) Cross-sectional (front) view of the pixel with the key dimensions. (C) Top view of the pixels. (D) Schematic pulse input for the FEM simulation.

Figure S17. (A) FEM results of the temperature within the layer of the Si heater arrays. The red curve shows the maximum temperature, and the black curve represents the minimum temperature. The results clearly show good heat confinement within the region of the activated pixel. (B) Schematic cross-sectional view of the heater layer.

Figure S18. (A) FEM results of the temperature along the *x* axis of the pixel. The black curve shows the maximum temperature, and the red curve represents the minimum temperature. (B) Schematic cross-section view of the heater.

Figure S19. (A) FEM results of the temperature across the thickness of the device. The black curve shows the maximum temperature, and the red curve represents the minimum temperature.

(B) Schematic cross-sectional view of the heater pixel.

Figure S20. (A) FEM results of the temperature along the *x* axis of the pixel for the cases with and without Ag heat spreading layer. The black curve shows the maximum temperature with the Ag, and the red curve shows the maximum temperature without Ag. The temperature is more uniform across the whole pixel with Ag. (B) Schematic cross-sectional view of the heater pixel.

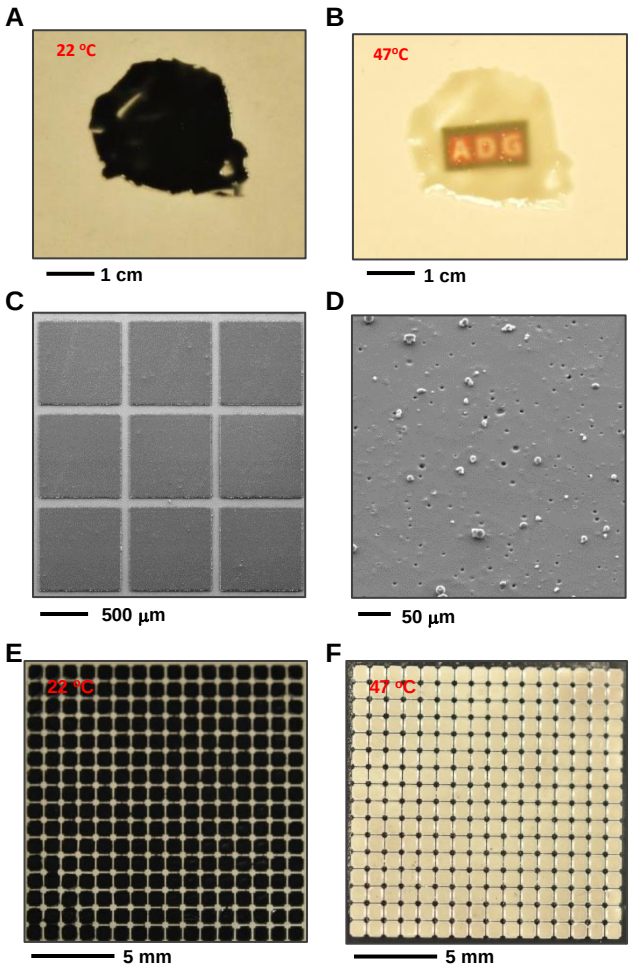


Figure S1

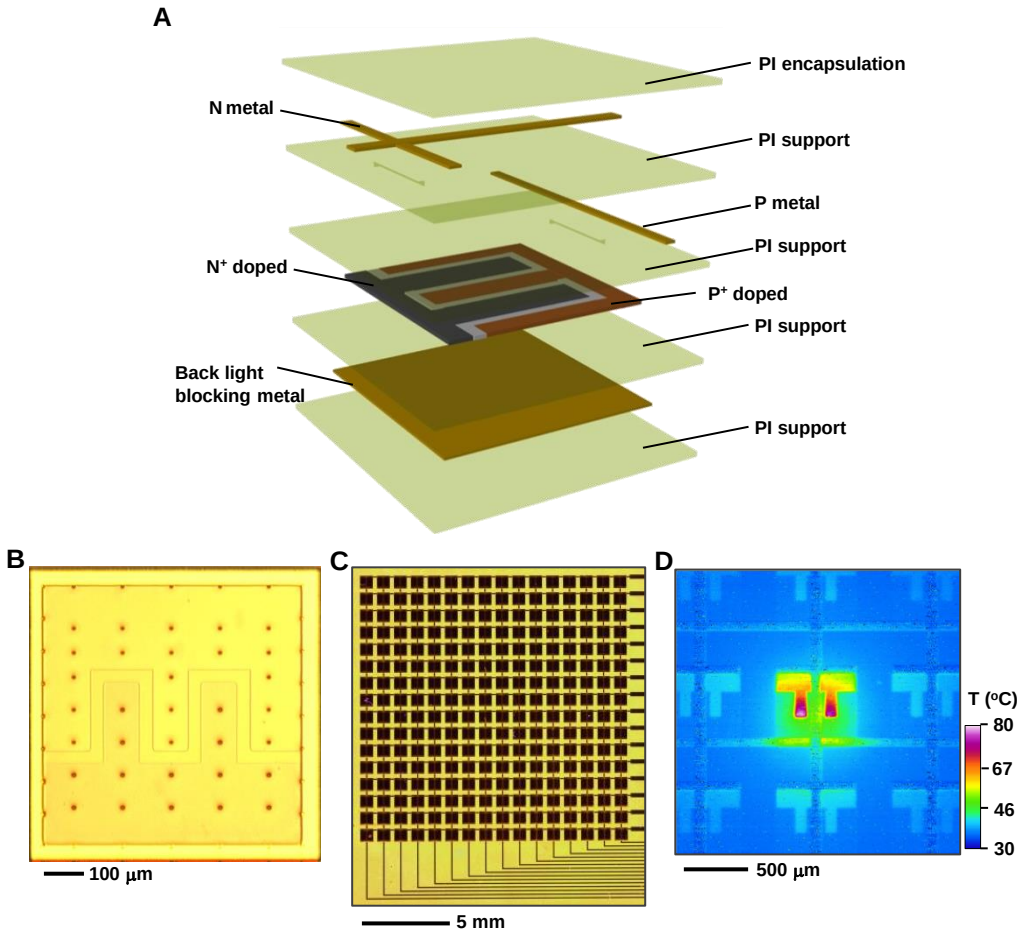

A
PI encapsulation
N metal
PI support
P metal
PI support
N+ doped
P+ doped
PI support
Back light
blocking metal
PI support
B
100 μm
C
5 mm
D
T (°C)
80
67
46
30
500 μm

Figure S2

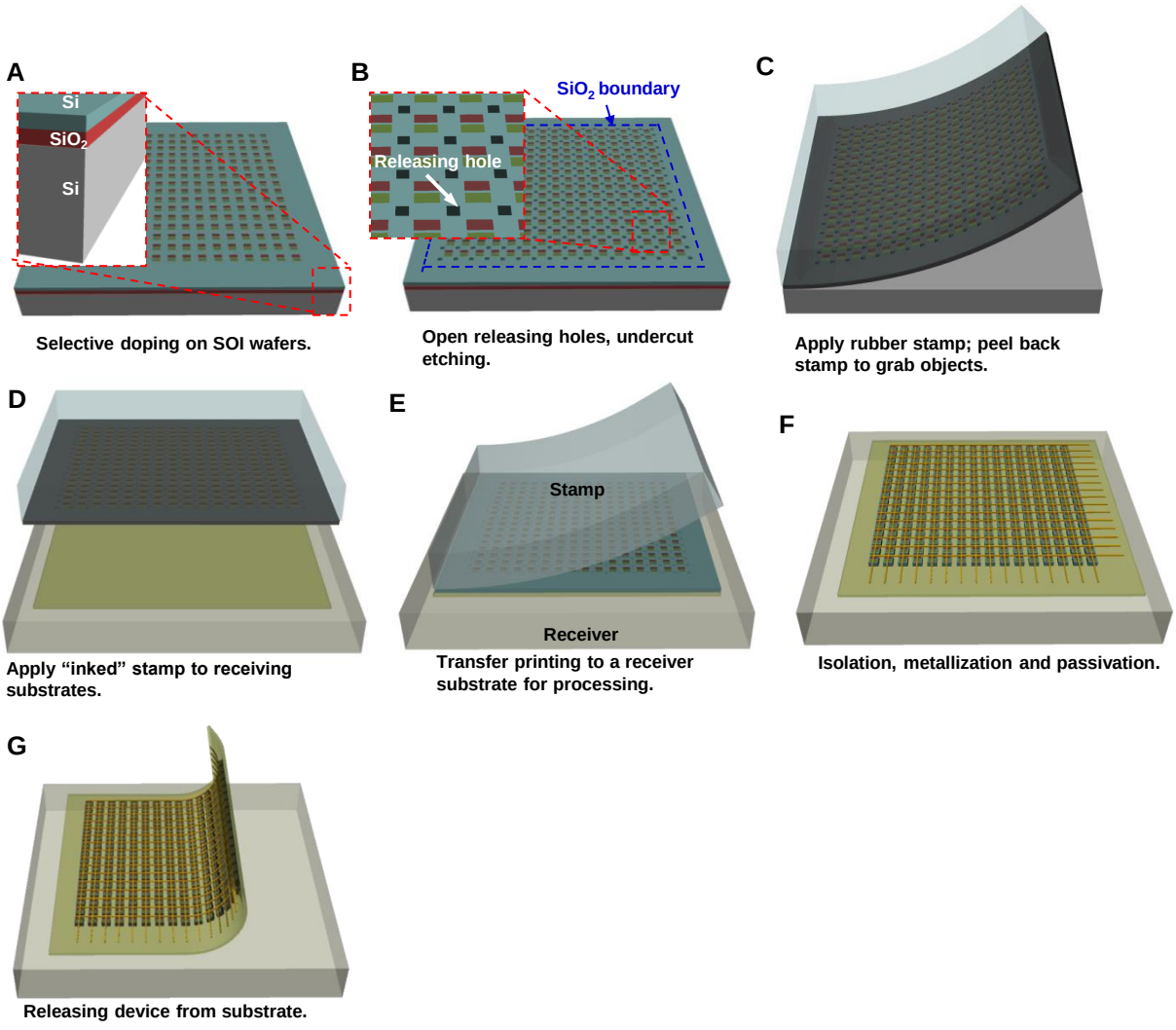

A
Si
SiO2
Si
Selective doping on SOI wafers.
B
SiO2 boundary
Releasing hole
Open releasing holes, undercut etching.
C
Apply rubber stamp; peel back stamp to grab objects.
D
Apply “inked” stamp to receiving substrates.
E
Stamp
Receiver
Transfer printing to a receiver substrate for processing.
F
Isolation, metallization and passivation.
G
Releasing device from substrate.

Figure S3

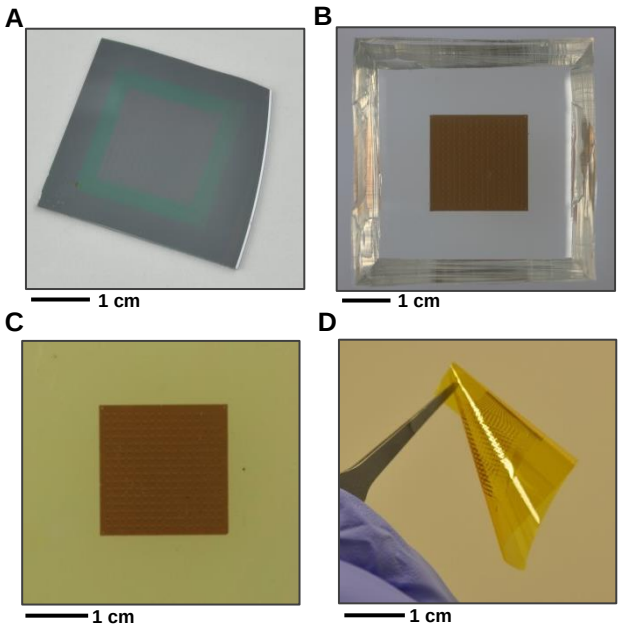


Figure S4

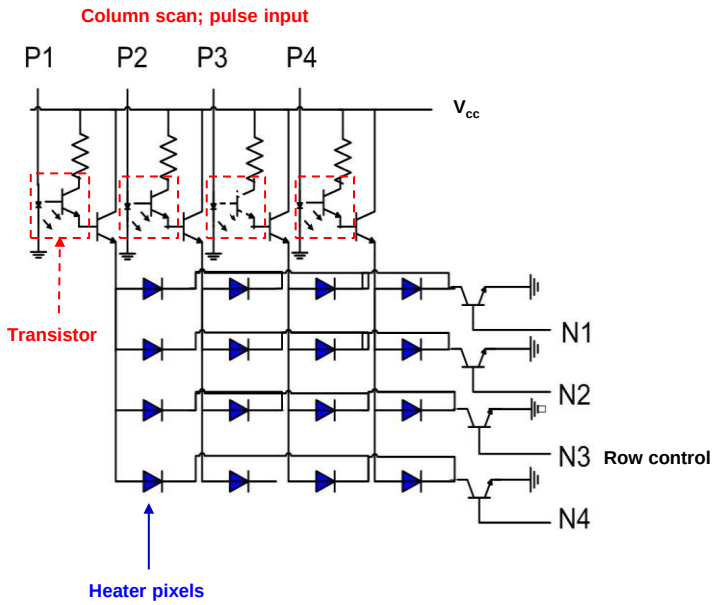
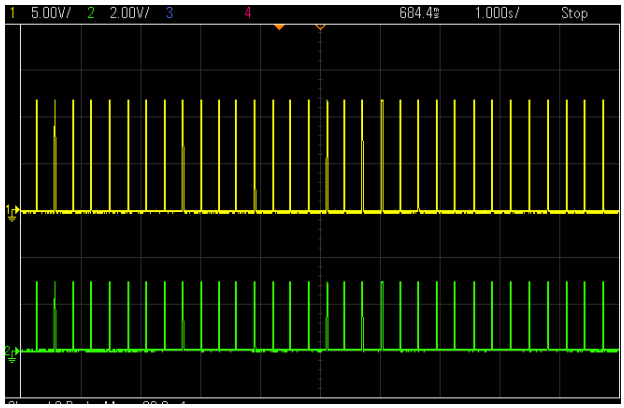

Column scan; pulse input
P1
P2
P3
P4
V_{cc}
Transistor
N1
N2
N3
N4
Row control
Heater pixels

Figure S5

A


1 5.00V/ 2 2.00V/ 3 4 684.4µs 1.000s/ Stop

B

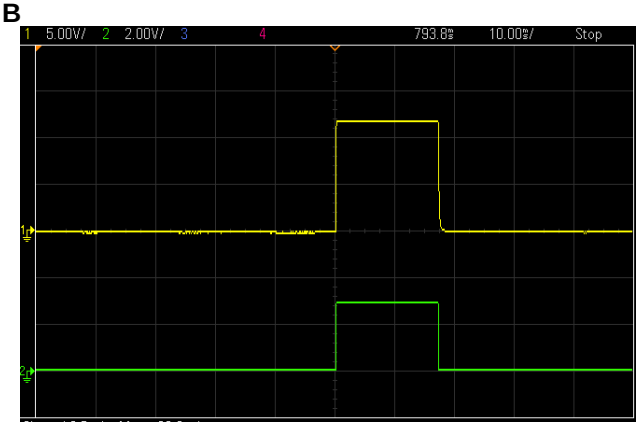

1 5.00V/ 2 2.00V/ 3 4 793.8µs 10.00µ/ Stop

Figure S6

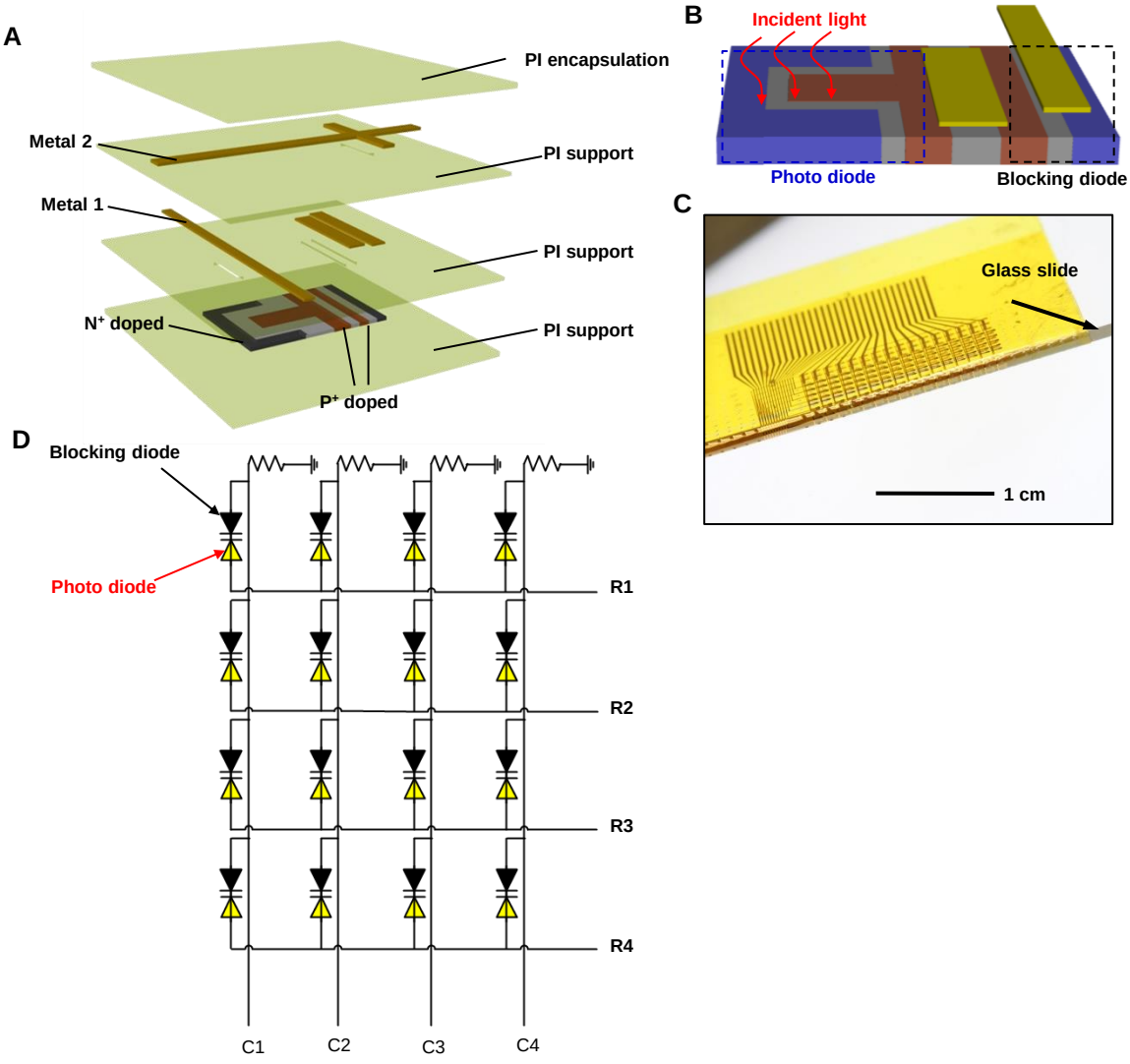

A
PI encapsulation
Metal 2
PI support
Metal 1
PI support
N+ doped
PI support
P+ doped
B
Incident light
Photo diode
Blocking diode
C
Glass slide
1 cm
D
Blocking diode
Photo diode
R1
R2
R3
R4
C1
C2
C3
C4

Figure S7

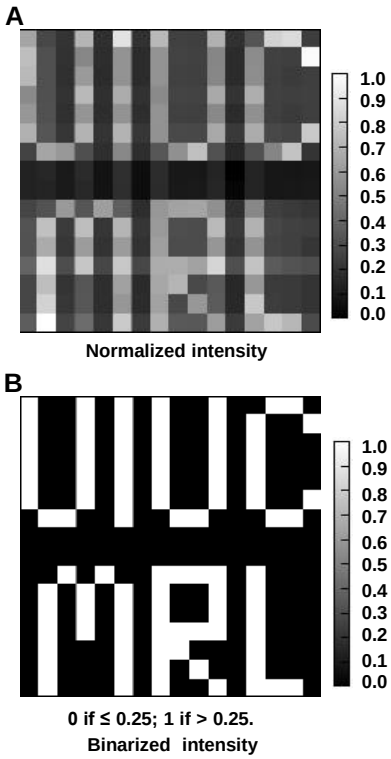

A
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
Normalized intensity
B
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0 if ≤ 0.25; 1 if > 0.25.
Binarized intensity

Figure S8

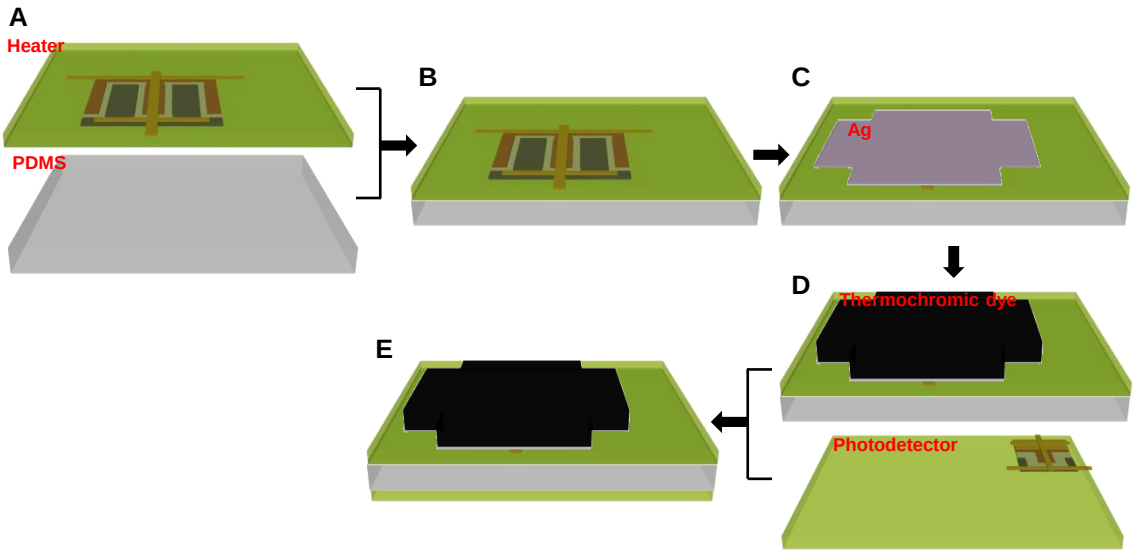


Figure S9

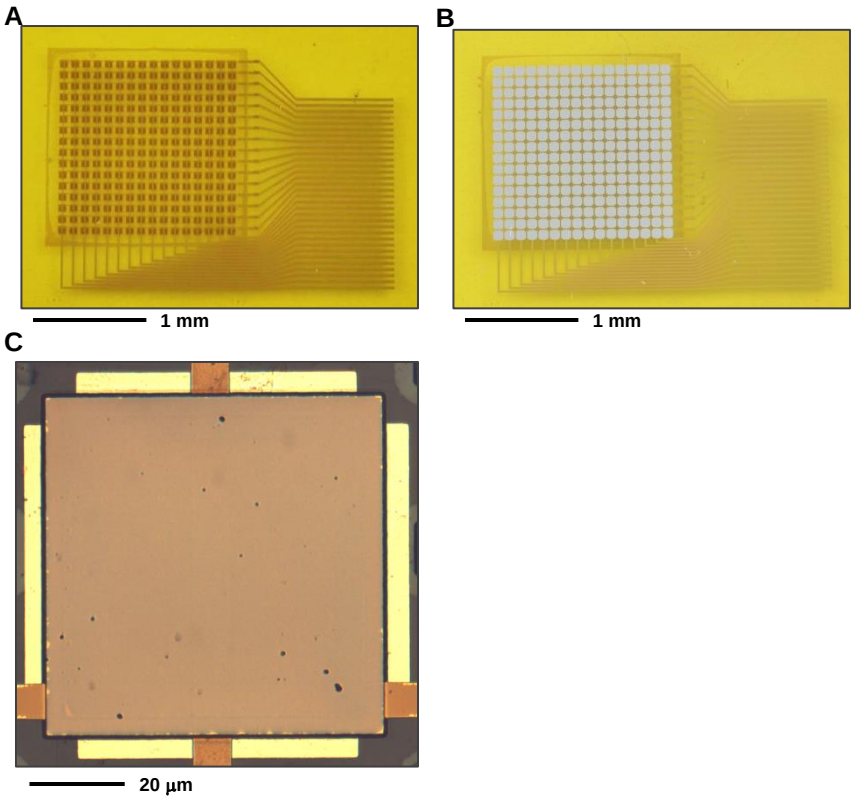


Figure S10

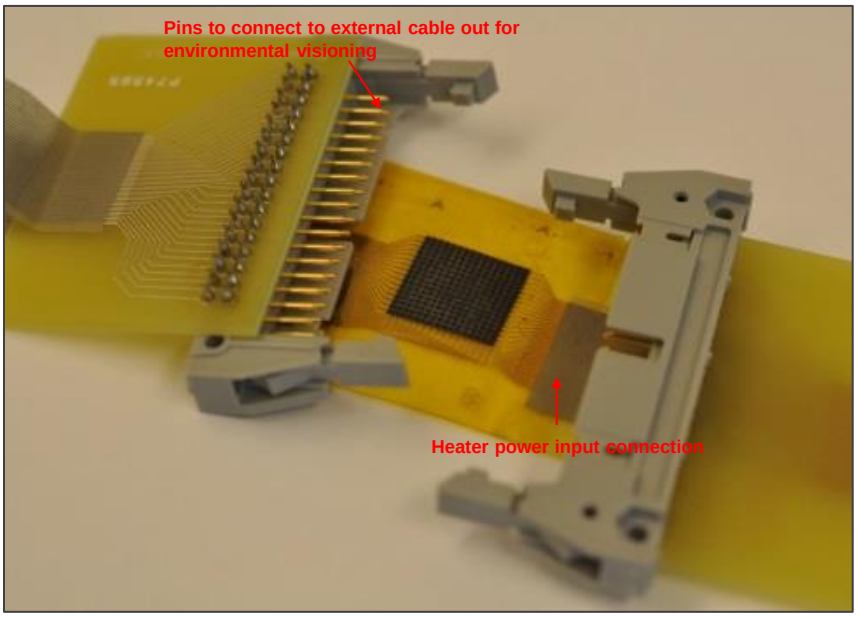

Pins to connect to external cable out for environmental visioning
Heater power input connection
1 cm

Figure S11

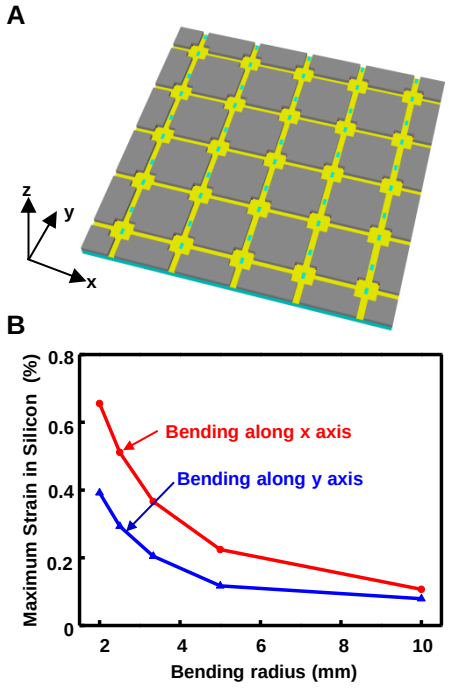

A
z
y
x
B
Maximum Strain in Silicon (%)
0.8
0.6
0.4
0.2
0
Bending along x axis
Bending along y axis
2
4
6
8
10
Bending radius (mm)

Figure S12

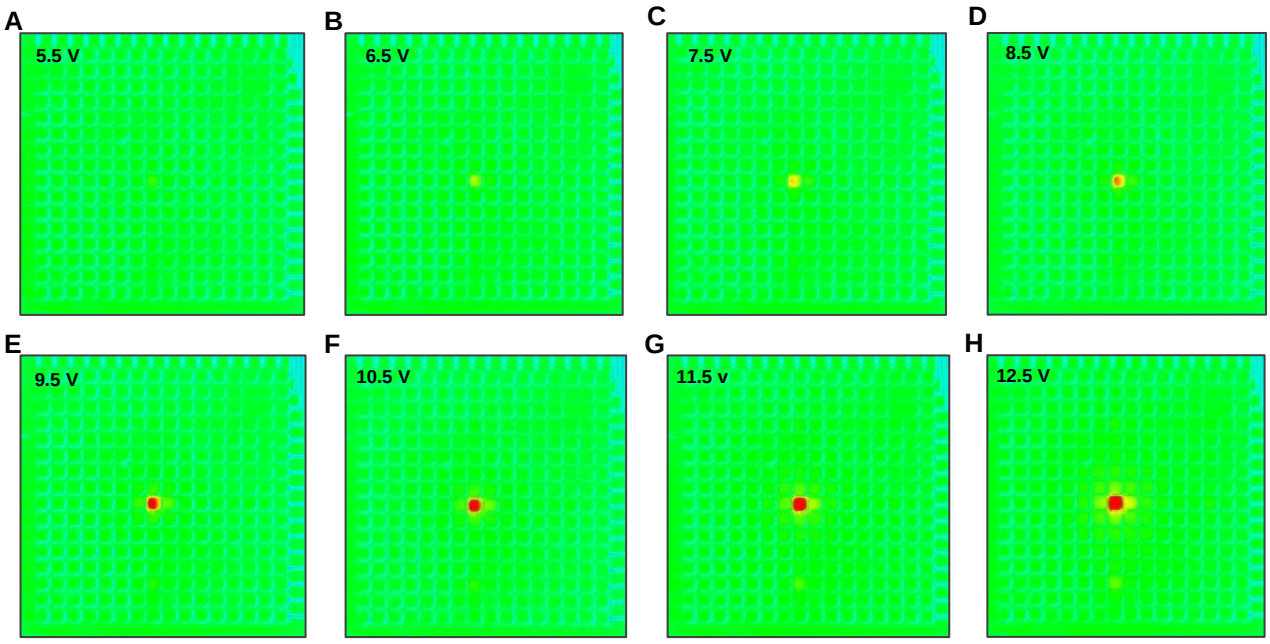


Figure S13

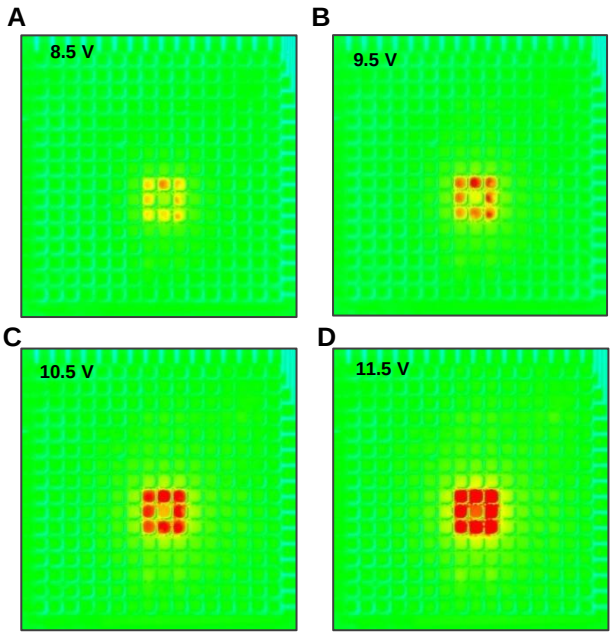


Figure S14

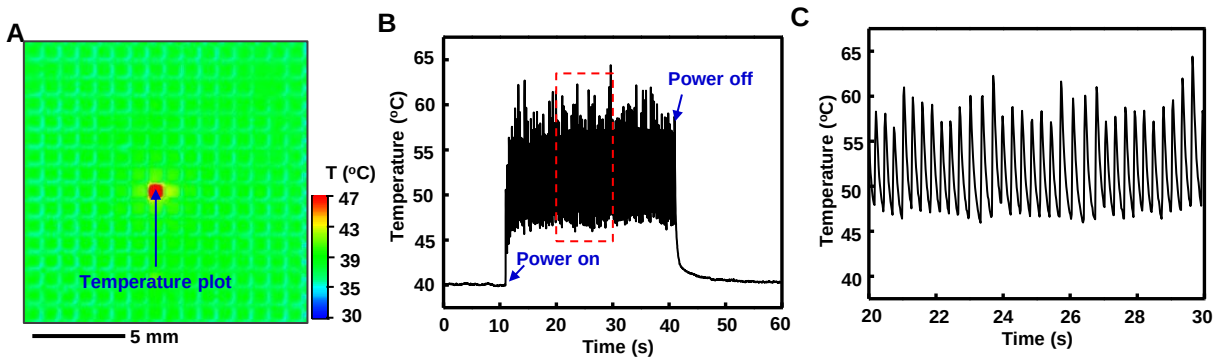

A
T (°C)
47
43
39
35
30
Temperature plot
5 mm
B
Temperature (°C)
65
60
55
50
45
40
Power off
Power on
0
10
20
30
40
50
60
Time (s)
C
Temperature (°C)
65
60
55
50
45
40
20
22
24
26
28
30
Time (s)

Figure S15

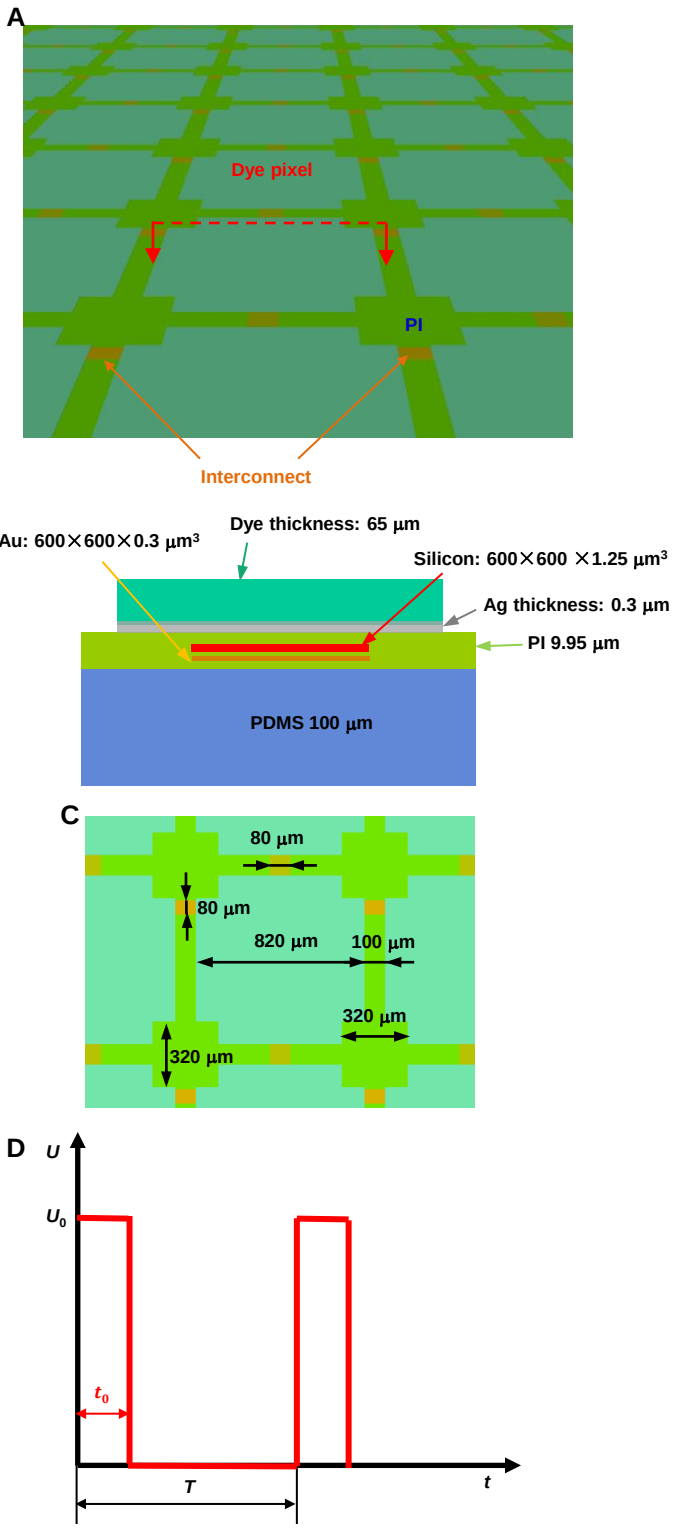

A
Dye pixel
PI
Interconnect
B
Au: 600×600×0.3 μm³
Dye thickness: 65 μm
Silicon: 600×600 ×1.25 μm³
Ag thickness: 0.3 μm
PI 9.95 μm
PDMS 100 μm
C
80 μm
80 μm
820 μm
100 μm
320 μm
320 μm
D
U
U0
t0
T
t

Figure S16

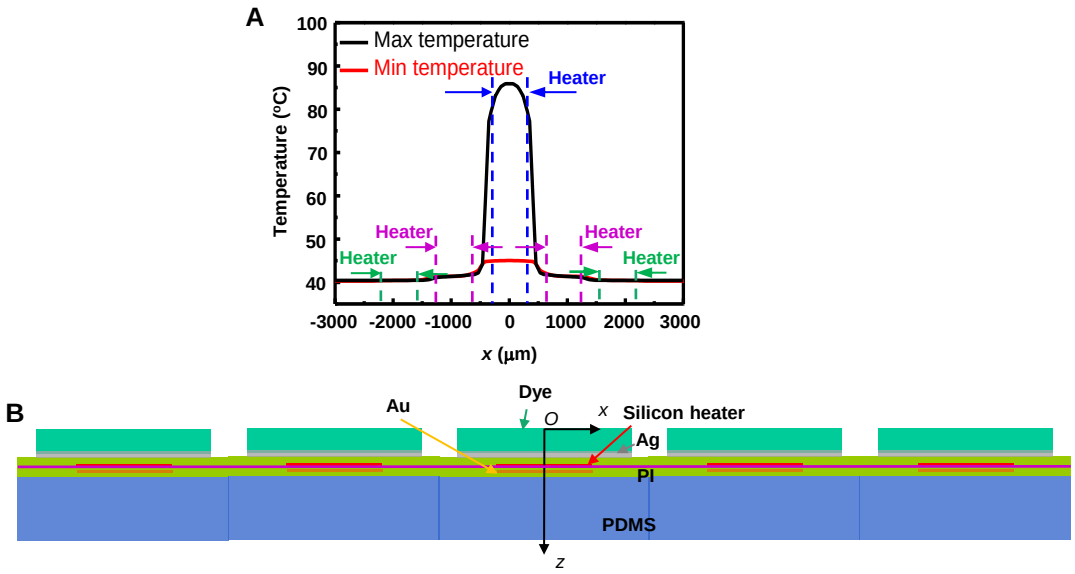

A
Max temperature
Min temperature
Heater
Heater
Heater
Heater
Heater
Temperature (°C)
100
90
80
70
60
50
40
-3000
-2000
-1000
0
1000
2000
3000
x (μm)
B
Au
Dye
O
x
Silicon heater
Ag
PI
PDMS
z

Figure S17

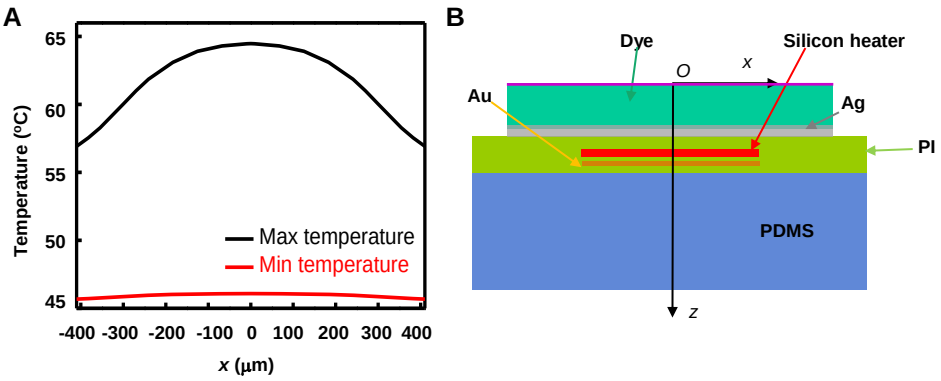

A
65
60
55
50
45
Temperature (°C)
Max temperature
Min temperature
-400 -300 -200 -100 0 100 200 300 400
x (μm)
B
Dye
Silicon heater
O
x
Au
Ag
PI
PDMS
z

Figure S18

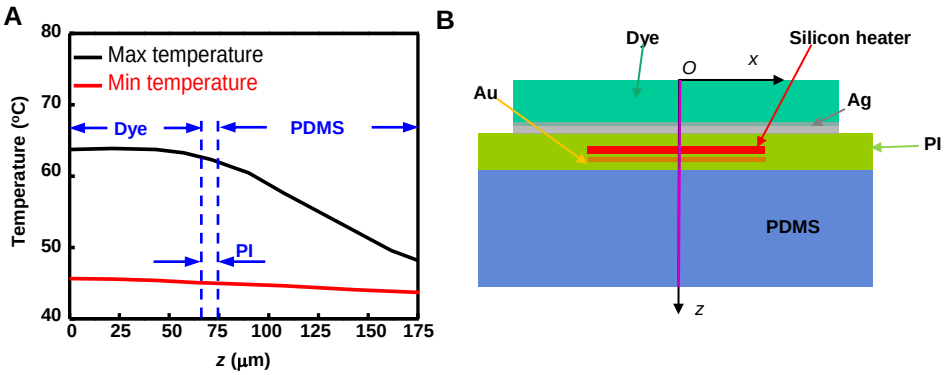

A
B
Max temperature
Min temperature
Dye
PDMS
PI
Temperature (°C)
z (μm)
80
70
60
50
40
0
25
50
75
100
125
150
175
Dye
Silicon heater
O
x
Au
Ag
PI
PDMS
z

Figure S19

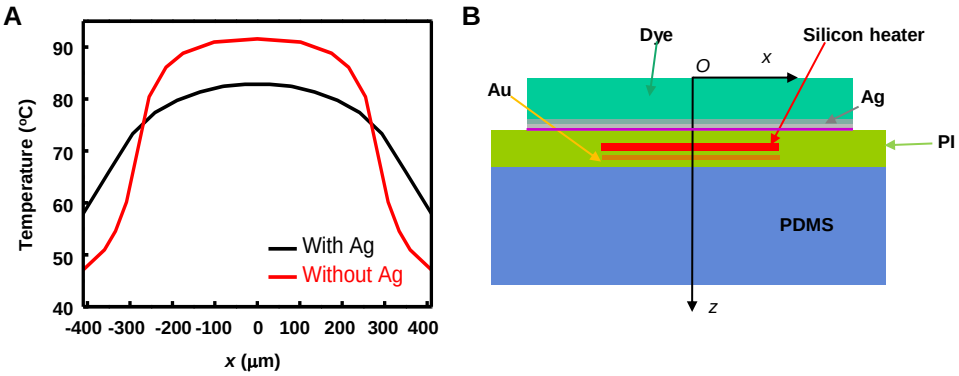

A
Temperature (°C)
90
80
70
60
50
40
-400 -300 -200 -100 0 100 200 300 400
x (μm)
With Ag
Without Ag
B
Dye
Silicon heater
O
x
Au
Ag
PI
PDMS
z

Figure S20