Supporting Information

Large Area Growth and Electrical Properties of p-Type WSe_2 Atomic Layers

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Experimental Section

WSe_2 growth: To synthesize the layered WS_2 flakes, the 0.2 g WSe_2 powder (Alfa Aesar, 13084) was added into an alumina boat as precursor. The blank SiO_2/Si substrates (1 cm by 5 cm) loaded into a home-built vapour deposition system in a horizontal tube furnace (Lindberg/Blue M) with 1-inch quartz tube (Figure S1 in the Supporting information). The system was pumped down to a vacuum of 10 mTorr in 10 min, and re-filled with 150 sccm of ultra-high purity argon gas (Airgas, ~ 99.9999%) then heated to desired growth temperature within 30 min. After that, the growth kept at the designed temperature for 30 min, and then terminated by shutoff the power of the furnace. The sample was naturally cooled down to ambient temperature.

WSe_2 Transfer: The transfer of the WSe_2 films onto arbitrary substrates was performed by the wet-etching of the SiO_2 layer. The top side of the WSe_2/SiO_2/Si surface was spin-coated with PMMA (495 PMMA C2, MicroChem) and baked at 120 ℃ for 1 min. After that, the SiO_2 were etched away using buffered oxide etchant (5:1:8 of NH_4F: HF:

deionized H_2O), resulting in a free-standing PMMA/WSe_2 membrane floating on the surface of the etchant bath. The PMMA/WSe_2 film was washed with deionized (DI) H_2O for several times, and then transferred onto a prepared substrate. After dried in the air, the PMMA was dissolved by acetone and the substrate was rinsed with isopropyl alcohol to yield a WSe_2 film on the substrate.

WSe_2 device fabrication: Single back-gated FETs were fabricated on the monolayer, bilayer, and few-layer WSe_2 on a silicon substrate with 300 nm SiO_2 substrates. E-beam lithography was employed to pattern the contact electrodes. The source/drain electrodes (Au: 100 nm) were deposited using e-beam evaporation. The back gate voltage was applied by using a Si back gate with SiO_2 as the dielectric.

Characterizations: The morphology and structure of the graphene were characterized with optical microscope (Olympus BX51), field emission scanning electron microscope (FESEM, JSM-6701F), high-resolution transmission electron microscopy (HRTEM, FEI Titan S/TEM at 300 kV), and Raman spectroscopy (Horiba, 514 nm laser wavelength, 50 $\times$objective). Electrical transport properties of the samples were measured at room temperature in a Lakeshore probe station (Model PTT4) with a computer-controlled precision source/measure unit (Agilent B2902A.

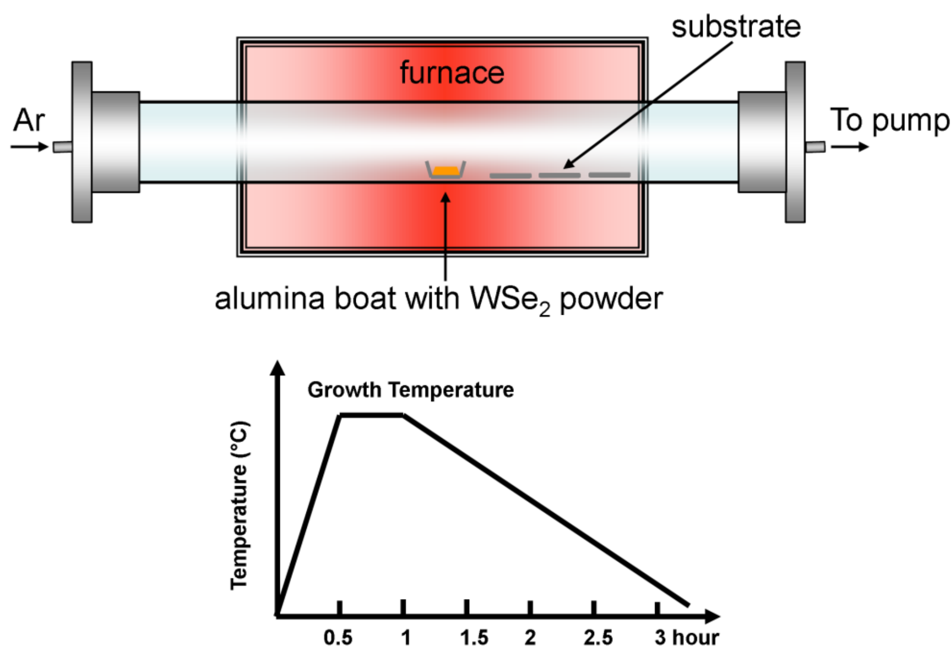

Figure S1. Schematic illustration of the growth equipment and recipe. Up: The WSe_2 powders are placed in an alumina boat at the center of the quartz tube, and the clean SiO_2/Si substrates designated for growth of WSe_2 atomic layers are leaved on the down-stream side. Argon is continuously supplied through the reactor with designed flow rate. Down: temperature control curve of substrate during growth.

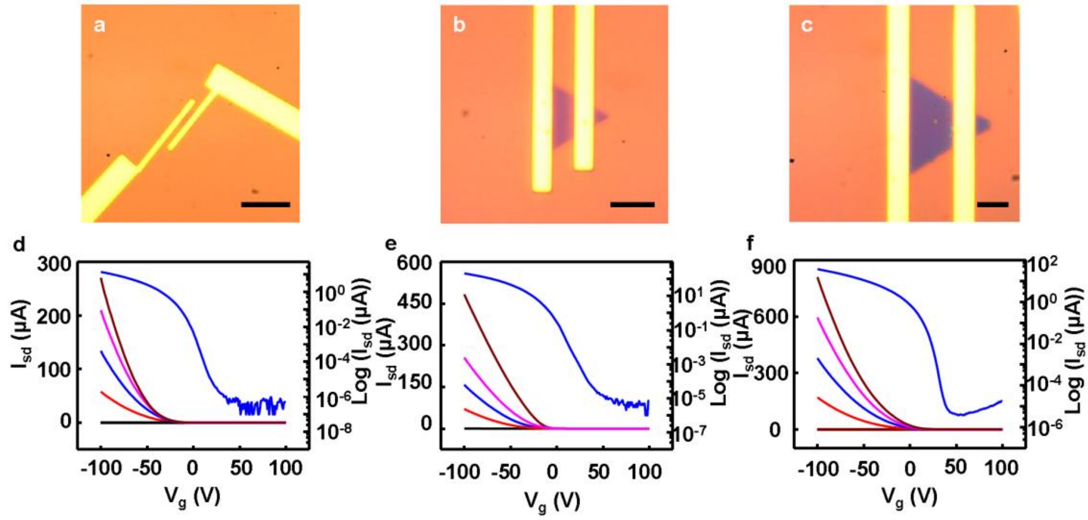

Figure S2. Electrical characteristics of the WSe_2 monodomains. Optical microscope image of (a) a monolayer WSe_2 transistor, (b) bilayer WSe_2 transistor, and (c) few-layer WSe_2 transistor, respectively. I_{sd}-V_g transfer characteristics plotted in (d), (e), and (f) of the device shown in panels (a), (b), and (c) at V_{sd} = 0, 1, 2, 3 and 4 V, respectively. All scale bars are 5 μm.