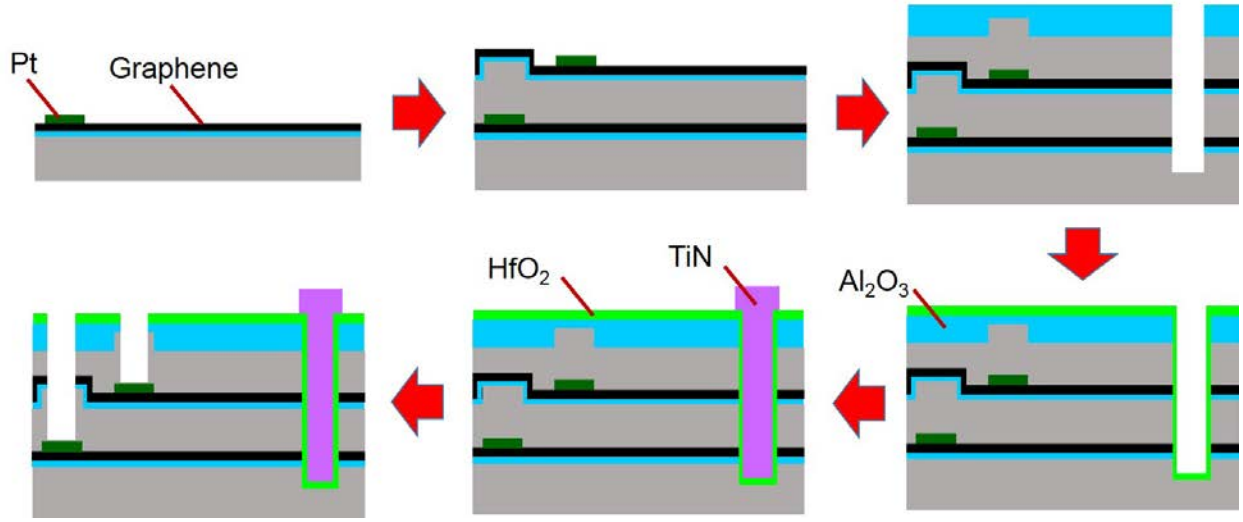
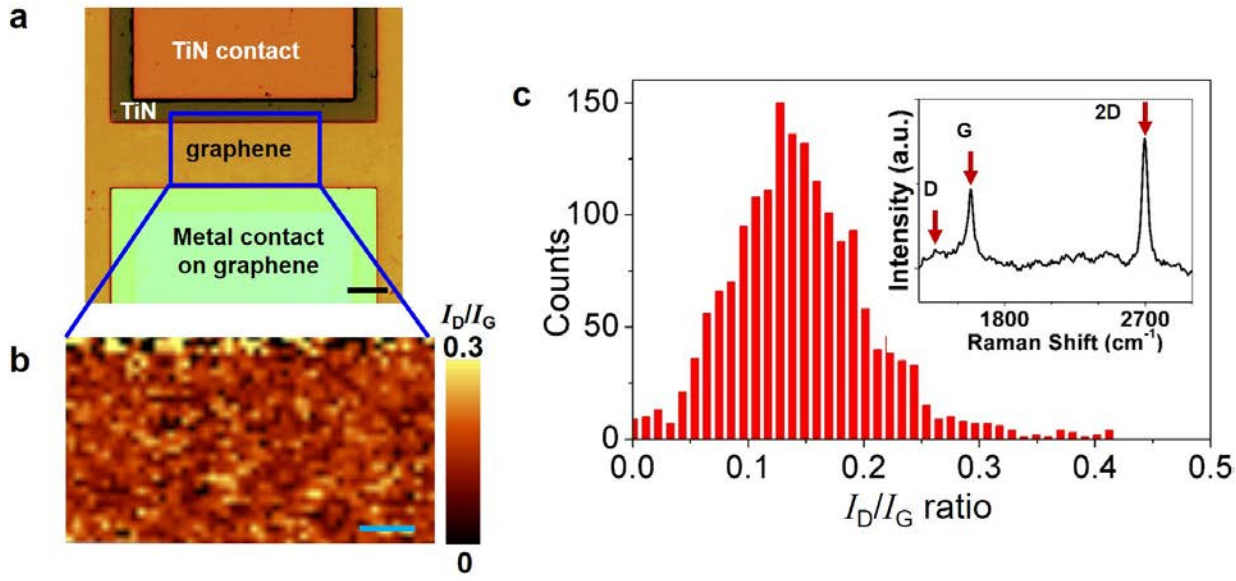
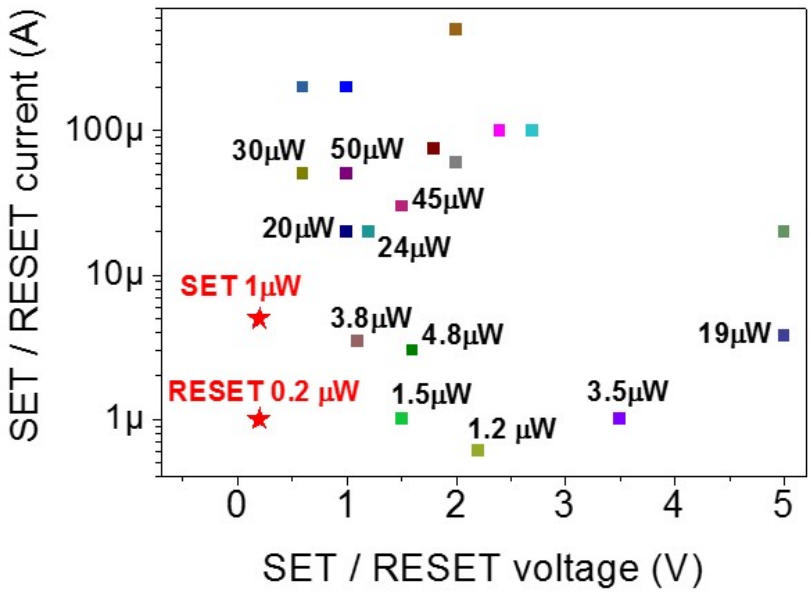
Supplementary Figures



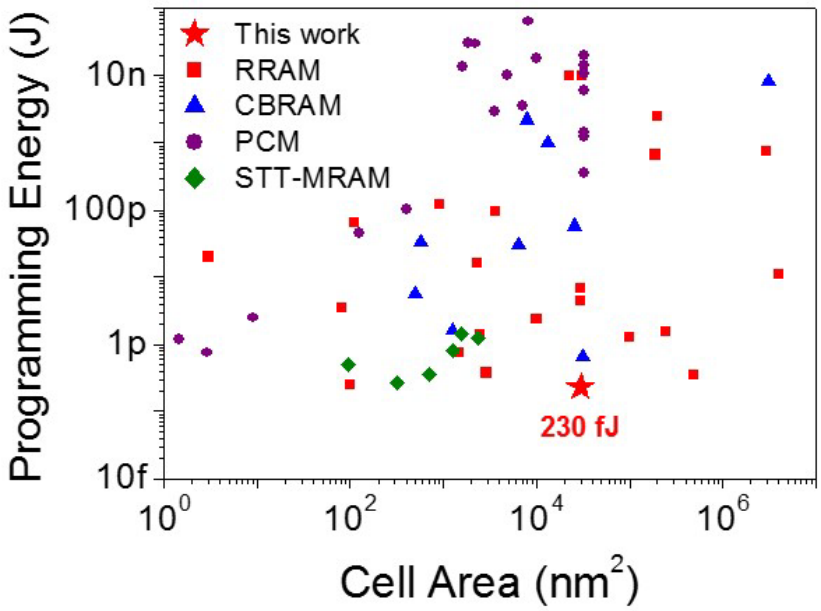
Supplementary Figure 1 Fabrication process. The devices were fabricated via sequential transfer of graphene, metal contact deposition, deep trench etching, HfO_2 deposition (atomic layer deposition) followed by TiN pillar formation (sputtering and lift-off) A thin layer (5nm) of Al_2O_3 was deposited before the graphene transfer process to promote graphene adhesion to the surface. First, single layer graphene is transferred on to a dielectric surface with 5 nm Al_2O_3 and 100 nm of SiO_2. The transfer method is identical to the previous works[1-3]. Monolayer graphene grown on copper foil with chemical vapour deposition method was purchased (Single Layer Graphene on Copper foil: 2 inch × 2inch, Graphene supermarket) and the monolayer quality was confirmed with Raman spectroscopy (Supplementary Figure 2c). Ti/Pt (3 nm/30 nm) layers are deposited by evaporation and patterned by lift-off process. 60 nm of SiO_2 (LPCVD) is deposited. Then these processes are repeated twice for two layers of single layer graphene; 50 nm ALD Al_2O_3 is deposited on the top layer for etch hard mask. A trench is etched down to the bottom SiO_2 layer followed by 5nm of HfO_x (ALD) which is conformally deposited as the active resistive switching layer and 200 nm of TiN electrode is deposited by sputtering and patterned via lift-off. The contacts are opened via dry etching.



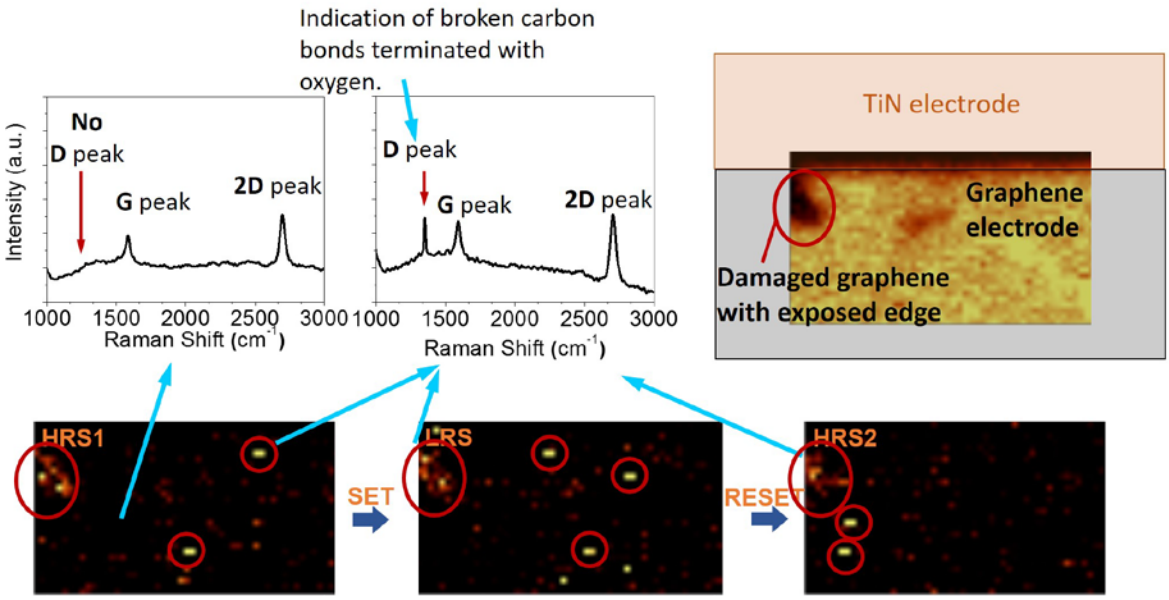
Supplementary Figure 2 Verification of graphene thickness and quality. a, Actual device image. The Raman laser scanned area is highlighted in blue. The scale bar is 15 µm. **b,** A 2D Raman spectra map of D peak to G peak ratio (I_D/I_G) after the complete fabrication process. This ratio is a known indicator of the disorders in graphene films. The I_D/I_G value is limited to approximately 0.1, indicating a low defect density in the film[4]. The inset shows a typical Raman spectrum of monolayer graphene with weak D-peak intensity after the complete fabrication process. Minimized physical disturbance and the low fabrication temperature (<300 °C) were essential to maintaining the high quality graphene. The scale bar is 10µm. **c,** A histogram of I_D/I_G ratio of Supplementary Figure 2b. The median value is 0.12. A typical Raman spectrum of the scanned area is shown as the inset.



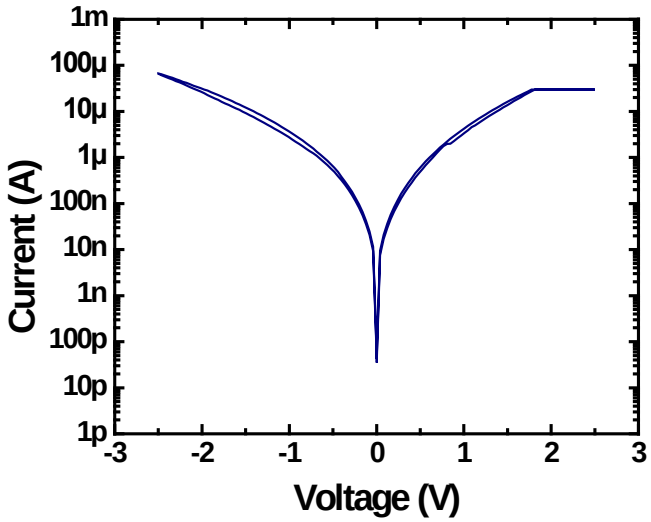
Supplementary Figure 3 Comparison of power consumption. Programming voltages, currents, and power consumptions from the recent reports[5-23] on low power RRAMs were plotted. With one of the lowest SET/RESET voltages ever recorded, the SET and the RESET power consumption of the demonstrated GS-RRAM (shown as red stars above) exhibit extremely low values. From a practical application point of view, the process that consumes the most power (SET or RESET) is plotted for other works, since the larger value determines the power delivery requirements for the chip.



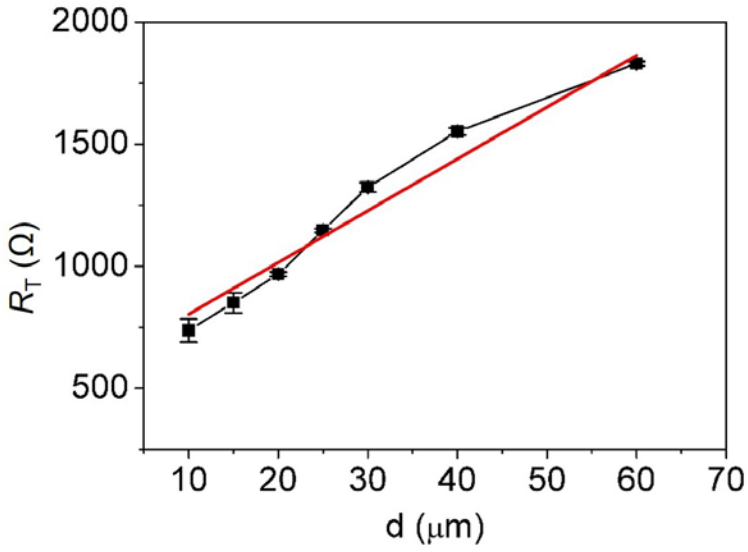
Supplementary Figure 4 Comparison of energy consumption. Comparison of programming energy for GS-RRAM and other emerging non-volatile memories with respect to cell area. The switching energy for GS-RRAM is one of the lowest. RRAM references are [5,11,24-47], CBRAM references are [48-56], PCM references are [57-76], and STT-MRAM references are[77,78], repectively.



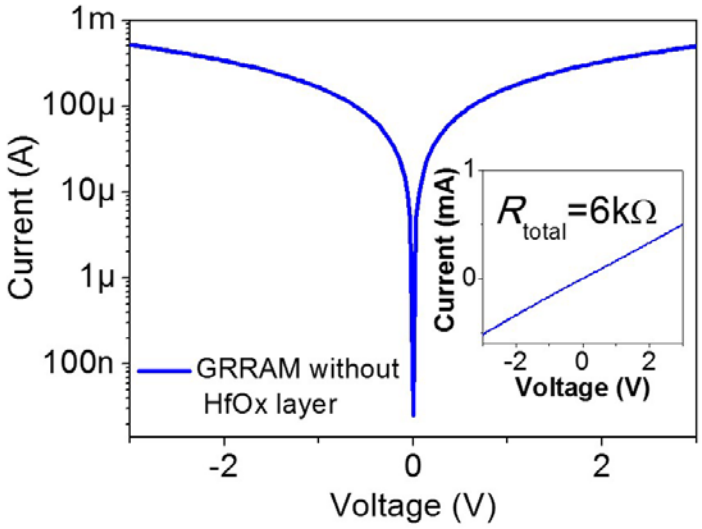
Supplementary Figure 5 Oxygen bonding in the graphene electrode. Although graphene is widely known to be inert, the edge and the broken bonds at the defect sites are more active compared to the basal plane of the graphene sheet. Typical graphene oxide Raman signature is the pronounced D peak[79]. (The intensity of G peak, on the other hand, is associated with the number of graphene layers and this may or may not be related to the graphene oxide.) D peak is also a strong indication of broken carbon bonds (i.e. dislocations, defects) and is pronounced in graphene ribbons with the edges exposed. These broken carbon bonds are more likely to be terminated with oxygen atoms. We specifically found an area in one of devices where the graphene was damaged and the edge was exposed. This edge is composed of broken carbon bonds similar to defects/dislocations at the basal plane and can be detected with the D peak intensity map as shown below in Supplementary Figure 3. An interesting aspect is that the defect region (bright area) highlighted with red circles seems to be created/annihilated (or even shifted) after consecutive SET and RESET process. Several past research results confirm that graphene broken bonds (dislocations) can be created/annihilated and shifted depending on which state is more thermodynamically favorable[80,81]. More importantly, this indicate that these oxygen binding phenomenon is reversible as previous work[82] suggested. As indicated in the reference[82], the oxygen may form a covalent bond at the defect sites of graphene after the SET process and the process is reversed during the RESET process. Another important observation is that the point defects seems to be created and annihilated randomly but at the edge, the bright colored region is pervasive regardless of whether it is after the SET or the RESET process. This may indicate that the edge is always oxidized when it is in contact with the HfO_x. The oxidized edge seems to have little effect on switching endurance of the device. We have switched the device more than 1600 times to observe that the memory function did not degrade (Fig. 4c).



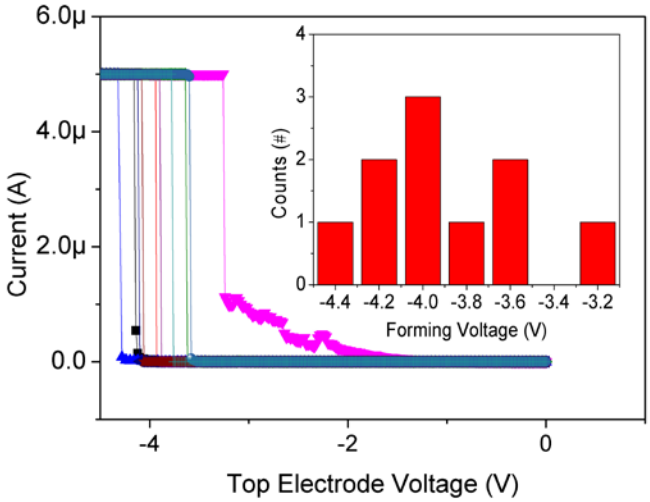
Supplementary Figure 6 Degradation of memory window for Pt-RRAM with 30 µA SET compliance. Pt-RRAM devices with lower SET compliance than 80 µA suffers from memory window degradation as shown in the plot. This is expected since PtRRAM's HRS is significantly more conductive compared to GRRAM due to the larger area of the Pt bottom (passive) electrode.



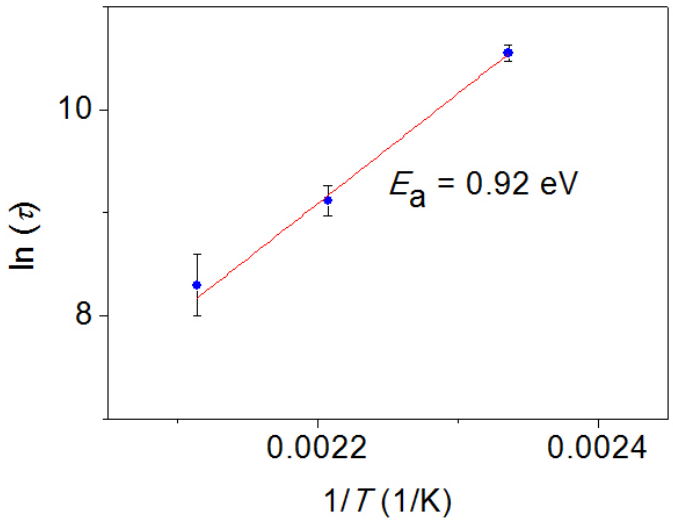
Supplementary Figure 7 Total resistance value from the as-fabricated wafer with circular transmission line test structure[83] as a function of gap distance. From the Y-intercept = $2R_C$ = 591Ω. The corresponding contact resistance R_C between the graphene and the metal (Ti/Pt) contact was found to be 295Ω with specific contact resistance of 9.3Ω·cm. With the slope of 21.2 Ω μm^{-1}, the sheet resistance of graphene ($R_{sh,G}$) is extracted to be 6.7kΩ per square. Pristine, exfoliated graphene without environmental doping is reported to have sheet resistance value of ~6 kΩ per square.[84]. From our I_D/I_G Raman map (Supplementary Figure 2), the defect level was not significant after dielectric deposition (LTO, 300°C). Considering the low D-peak level in our graphene, the resulting $R_{sh,G}$ is in close agreement with that of a pristine graphene that is void of any dopants or defects [85-87]. Since the measurements are done on the as-fabricated wafers, small discrepancies may arise from the process conditions. For Ti/Pt layer (Ti 1 nm/Pt 5 nm), the sheet resistance $R_{sh,Pt}$ was extracted to be 558Ω from 20 TLM measurements. The Pt sheet resistance is also in agreement with the literature [88]. Graphene is approximately ×20 thinner than the Ti/Pt layer and ×12 more resistive, showing slightly superior conductance with similar thicknesses. However, it should be noted that atomically thin metal such as Pt layer tends to form discontinuous island, and a sharp nonlinear increase in sheet resistance is observed as the thickness decreases [88].



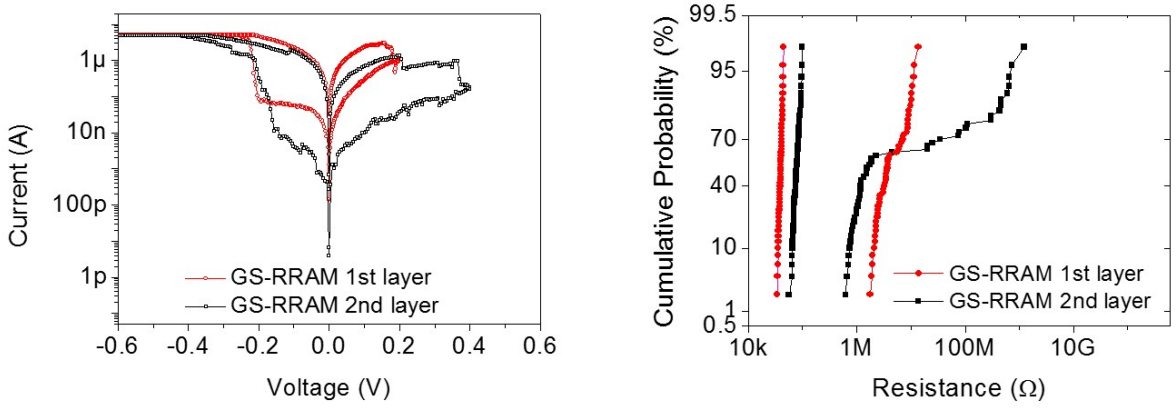
Supplementary Figure 8 The I-V curve of GS-RRAM without the HfOx layer (inset: linear scale). The I-V curve of GS-RRAM without the HfOx layer (inset: linear scale). The total resistance of the GS-RRAM device *without* the HfO_2 is close to 6 kΩ, which is only a fraction of HRS resistance. This strongly indicates that the series resistance R_{series} (i.e. $R_{sh,G}$ + R_c) of GS-RRAM is not the major factor that contributes to the increases of the HRS resistance in GS-RRAM. On the contrary, this outcome suggests that the difference between the R_{switch} of GS-RRAM ($R_{int,G}$ + $R_{filament,G}$) and Pt-RRAM ($R_{int,Pt}$ + $R_{filament,Pt}$) determines the HRS of GS-RRAM and Pt-RRAM, respectively.



Supplementary Figure 9 Forming of GS-RRAM. The top electrode is the TiN electrode during the forming process. Forming curves are collected from 10 cells with 5µA compliance current. Inset: forming voltage distribution.



Supplementary Figure 10 Arrhenius type plot of the wait time versus 1/*T* extracted from Fig. 4b. The sudden transitions to the OFF state in Fig. 4b corresponds to the rupture of the oxygen vacancy based filament by the diffusion of oxygen ion towards HfO_x layer. The activation energy of the barriers can be extracted from temperature dependence of the characteristic dwell time for RESET transition (Arrhenius equation in Methods). From the linear fitting of retention time in logarithm scale versus reciprocal temperature, we estimate of the activation energy E_a for ion migration in graphene to be 0.92 eV.



Supplementary Figure 11 Typical DC I-V switching and HRS/LRS characteristics of bottom layer and top layer of GS-RRAM. The GS-RRAM in the bottom layer exhibited even lower RESET current with similar SET voltages. However, there were some discrepancies in the RESET voltages for bottom and top layer. Importantly, the overall RESET power is still similar due to lower RESET current. Qualitatively similar memory windows were observed for top and bottom devices. The lowest memory window in the second layer is still above 10×.

Supplementary Table

	Thickness in nm (Electrode+SiO_2)	F = 20 nm	F = 22 nm	F = 26 nm
Etch ratio 30 Etch Angle 88°	11nm (Pt=5nm)	54	60	70
	16nm (Pt=10nm)	37	41	48
	21nm (Pt=15nm)	28	31	37
Etch Angle 89°	6.3nm (graphene=0.3nm)	181	200	236

Supplementary Table 1 Analysis of the number of achievable stacks with a dielectric thickness of 6nm. The achievable number of stacks can be calculated using the equation for reliability projection from reference [88]. Total stack height = $R \times F/T$ (R is the etching aspect ratio, F is the lithographic half pitch, and T is the combined thickness of the plane electrode and the dielectric in between). Assuming SiO_2 thickness of 6 nm, half-pitch of 22nm, and etch angle increase of just 1°, the maximum graphene RRAM stacks possible will be 200 stacks compared to the 60 stacks possible with Pt-RRAM. With an operating voltage of 0.2V in our GS-RRAM and a higher etching angle, we expect the number of possible graphene RRAM stacks to increase even more since a thinner dielectric can be used.

Supplementary Notes

Supplementary Note 1 3D vertical cross-point architectures

A pressing imperative for RRAM technology is to adopt a bit-cost-effective 3D architecture satisfying the requirements of performance metrics (density, latency, and energy consumption), which surpass those of 3D stackable multi-bit NAND Flash technology. Many industry/research groups [89-93] are actively working on variations of 3D vertical cross-point architectures as shown in Supplementary Fig. S1. The graphene RRAM in this work (with pillar electrode and planar graphene electrode) is compatible with all the 3D vertical cross-point architectures recently introduced [89-93].

The integration density of such 3D architectures depends on the number of stacks which is limited by the plane electrode thickness, the sheet resistance of the plane electrode, the dielectric thickness (related to the programming voltages and cross-talk), the pillar etch angle, the lithographic pitch, and the resistance of the pillar/plane electrode [88,94].

Since the total pillar height is limited, a thin device structure will be important for ultra-high density storage[88,94]. However, there is a fundamental limitation on how thin the metal plane electrode can be.

There has been a recent report of an RRAM structure with a sub-5nm thick vertical TiN electrode [95]. Although it is possible to form such sub-5nm metal electrodes, the main challenge lies not in the thickness of the metal, but in the high sheet resistance. All metal films are known to exhibit a steep exponential increase in sheet resistance as the thickness decreases under 10 nm[88,96]. This is because extremely thin metal films tend to form discontinuous islands, and thin dielectric layers are formed on the grain boundaries[96]. Such high sheet resistance of the plane electrode will result in a significant voltage drop on the electrode and severely degrade the write/read margin of the 3D RRAM structure[88,94], which limits the integration density. Hence, producing a sub-5nm conducting film with a low enough sheet resistance for 3D RRAM is a difficult task without using special methods or materials.

Graphene's sheet resistance per thickness is significantly lower than that of any metal. Graphene has been experimentally proven through the use of doping technique[97] to have sheet resistance as low as 125 - 200 Ω per square[1,86,97] with a monolayer thickness. These levels of resistance are something impossible to achieve (at such thickness) with conventional metal. From the measurements, graphene exhibited superior sheet resistance value per thickness (i.e. graphene is 20× thinner and 12× more resistive) compared to Pt after fabrication (Supplementary Section 7). Considering the nonlinear increase of Pt sheet resistance in such a scale, the actual sheet resistance of Pt when it is as thin as graphene will be drastically higher.

It is also important to note that metal contact to graphene is an ohmic contact, and the contact resistance is relatively low due to the graphene's semi-metallic nature[97]. An optimized

metal/graphene specific contact resistivity is 7.5×10^{-8} Ω cm^2 [98]. This value is smaller than that of both Al and Pt contact to degenerately N-doped silicon ($2\times10^{20}cm^{-3}$) as shown in [99].

From the analysis in the previous work[88], the required dielectric thickness is approximately 6 nm of SiO_2 in between each layer if the devices are to work with operating voltages of 3V (much higher than the 0.2V required for our GS-RRAM). The 6 nm SiO_2 is required since it can maintain a lifetime > 10 years at the operating voltage of 3V based on the breakdown voltage and the time dependent dielectric breakdown (TDDB) lifetime extrapolation for PECVD SiO_2 sandwiched between metal electrodes[100]. Finally, graphene (3Å) is significantly easier to etch vertically than Pt (6nm) during pillar formation. (Graphene is simply etched with weak O_2 plasma treatment.) This property is highly beneficial since the etch angle is a very important factor that determines the number of achievable stacks [88,94].

Supplementary Note 2 Comparison of using graphene as an oxygen detector (previous work, ref[82]) and for oxygen storage (this work)

In RRAM devices, the resistive switching is attributed to the formation (SET) and the subsequent rupture (RESET) of nanoscale conductive filaments involving oxygen ion migration[14,101-106]. A generally accepted theory claims that the filament formation is based on the oxygen ion movement from the switching material.

It is fairly well known that the oxygen function as dopants in graphene, and the doping level of graphene can be observed with Raman spectroscopy[82,107,108]. We have previously monitored the oxygen ion in a RRAM structure by inserting graphene film between the TiN layer and HfO_x[82].

The memory structures in our previous work and the current work are very different. In the previous work, the SET electrode is the TiN and the RESET electrode is the Pt. In our work, the SET electrode is the graphene edge and the RESET electrode is the TiN. Also the previous work is a planar structure and the current work is a vertical structure.

Although both previous and current work report low power consumption, the mechanisms for achieving low power consumption are fundamentally different. In the previous work, the low power was due to reduced RESET current from the high built-in series resistance of inter-layer graphene. The overall SET/RESET voltages (~2V) have few differences between structures "with" and "without" graphene interlayer.

In the current work, we see a drastic difference in SET/RESET voltages between GS-RRAM (~0.2V) and the Pt-based device (~1.5 to 2V). This is because the graphene, instead of the TiN layer, is used as the SET electrode. Here we are using graphene as a stand-alone oxygen reservoir, unlike in the previous work. The lowering of SET/RESET voltage is related to the lack of a TiO_xN_{1-x} barrier layer in the HfOx/graphene interface, and the ease of oxygen diffusion across the graphene electrode as explained in the main text.

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