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Supplementary Materials for

A wearable multiplexed silicon nonvolatile memory array using nanocrystal charge confinement

Jaemin Kim, Donghee Son, Mincheol Lee, Changyeong Song, Jun-Kyul Song, Ja Hoon Koo, Dong Jun Lee, Hyung Joon Shim, Ji Hoon Kim, Minbaek Lee, Taeghwan Hyeon, Dae-Hyeong Kim

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Supplementary text

Synthesis of AuNPs for LB assembly

0.4 g of $HAuCl_4 \cdot 3H_2O$ (99.9%, Strem, USA) and 25 mL of 1-octadecene (90%, Sigma Aldrich, USA) are mixed in a 50-mL glass vial. The vial is heated up to 90°C in an oil bath. 10 mL of oleylamine (Acros, 90%, USA) is added to the vial and reacted for 3 h. AuNPs are washed with ethanol three times and precipitated. The AuNPs are redispersed in 10 mL of toluene.

Fabrication of memory capacitor

The fabrication of the memory capacitor shown in Fig. 3C starts with the deposition of an Al_2O_3 T_{ox} layer on a bare Si wafer using the PEALD process (250°C, 50 cycles). For a film-type FG, a Au film is deposited on the T_{ox} layer by thermal evaporation (10 nm). For the chemically absorbed AuNP FG, the T_{ox} layer is treated with (3-aminopropyl)triethoxysilane:ethanol solution (1% v/v), and AuNPs are coated by a dipping process. For the AuNP FG assembled by the LB method, the typical LB process is used. As a B_{ox} layer, Al_2O_3 is deposited using the PEALD process (150°C, 350 cycles). A Au/Cr (70 nm/7 nm) layer is subsequently deposited on B_{ox} by thermal evaporation for forming contact pads.

Characterization of CTFM

The electrical characteristics of a CTFM are measured using a parameter analyser (B1500A, Agilent, USA). A high-voltage semiconductor pulse generator unit (HV-SPGU, Agilent, USA) is used to apply PGM/ERS pulses (-40 to 40 V) to the CTFM for a certain period of time (1 μs to 1 s). Source monitor units (SMUs; Agilent, USA) are used to apply the drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}) to the CTFM and to measure the drain current (I_d). All measured transfer characteristics of the CTFM are obtained using V_{DS} = 0.1 V. The threshold voltage is defined as the corresponding V_{GS} that induces I_d = 100 nA.

FEA of CTFM array and pseudo-CMOS inverter

FEA is used to analyse the strain distribution of a CTFM array and pseudo-CMOS inverter during stretching (Fig. 3M and N, and fig. S18C and D). The CTFM array and pseudo-CMOS inverter are modelled using four-node composite shell elements. The devices are placed on 1-mm-thick PDMS substrates that are modelled with eight-node solid elements. We assume perfect bonding (no slip condition) between devices and PDMS substrates. To simulate stretching, the stretching boundary conditions are applied on the bottom surface of the substrate. The linear elasticity represents the behaviour of the materials of the CTFM array and pseudo-CMOS inverters. Young's moduli of gold, Al_2O_3, epoxy (SU-8), SiO_2, and PI are 77.2, 463, 3.48, 73.1, and 2.5 GPa, respectively. Poisson's ratios of gold, Al_2O_3, epoxy (SU-8), SiO_2, and PI are 0.42, 0.22, 0.22, 0.17, and 0.34, respectively. The following anisotropic elasticity parameters are used for single-crystal Si: $E_{xx} = E_{yy} = 169$ GPa, $\nu_{xy} = 0.064$, $G_{xy} = 50.9$ GPa, and $G_{xz} = G_{yz} = 79.6$ GPa, where E and ν denote Young's modulus and Poisson's ratio, respectively, and the *x*- and *y*-axes are the <110> directions and are aligned in the horizontal and vertical in-plane directions, respectively. The incompressible neo-Hookean model is used to represent the PDMS substrate: $W = C_1(I_1 - 3)$, where W is the strain energy potential; I_1, the first invariant of the left Cauchy-Green tensor; and C_1 (=3 kPa for PDMS), a material parameter.

Fabrication of pseudo-CMOS inverter

As previously described in CTFM fabrication methods, the active regions of the doped SiNM transferred onto the PI layer (thickness: 1 μm) are isolated using RIE (SF_6 plasma) with photolithography. A 60-nm-thick SiO_2 gate dielectric layer is deposited by using plasma-enhanced chemical vapour deposition (PECVD) at 300°C. The subsequent deposition and patterning of a metal layer is conducted using thermal evaporation (Au/Cr, 100 nm/7 nm), photolithography, and wet etching to form the gate, source, and drain interconnections. The top PI layer (thickness: 1 μm) is coated and annealed. The entire trilayer (PI/device/PI) is patterned and etched by RIE (O_2 plasma). The fabricated pseudo-CMOS inverter is

then transferred onto a PDMS substrate, as described previously.

Data storage of heart rate recovery in wearable CTFM array

The wearable electrode array shown in Fig. 1E is laminated on the skin of the lower inner arm to acquire ECG signals, and it is interconnected to the wearable amplifier. A power supply is used to increase the body potential to 3.17 V (V_M) to maximize the effective gain of the amplifier. The amplified ECG signals are filtered using a digital band-pass filter to remove 60 Hz noise and analysed to measure the heart rate. Using SMUs (NI PXIe-4143, National Instruments, USA) and a matrix switching module (NI PXI-2530B, National Instruments, USA) controlled by custom-made LabVIEW (National Instruments, USA) software, each CTFM pixel in the array can be readily accessed, and the data stored in it can be read and modulated. To read the state of a CTFM pixel, the values of the drain current measured while the drain and gate voltage are set as 0.1 and 5 V, respectively, are obtained. If the drain current is below 50 nA, the stored data is considered the binary number “1.” If the drain current is above 50 nA, the stored data is considered the binary number “0.”

Supplementary figures

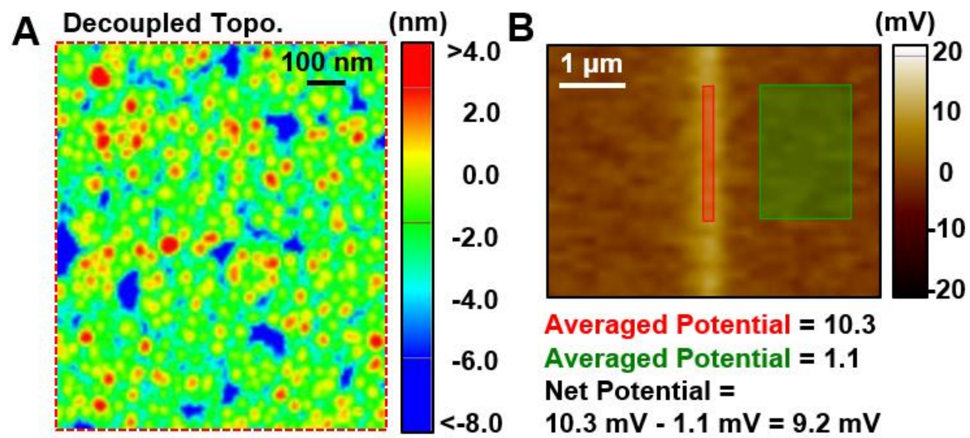

Figure S1: Original data corresponding to Fig. 1B. (A) Topographical AFM image decoupled with EFM signals. (**B**) EFM image of a FG cell after charge injection with an AFM tip biased with 7 V. The amount of charge stored in the FG is evaluated by subtracting the averaged potential of green region from that of red region.

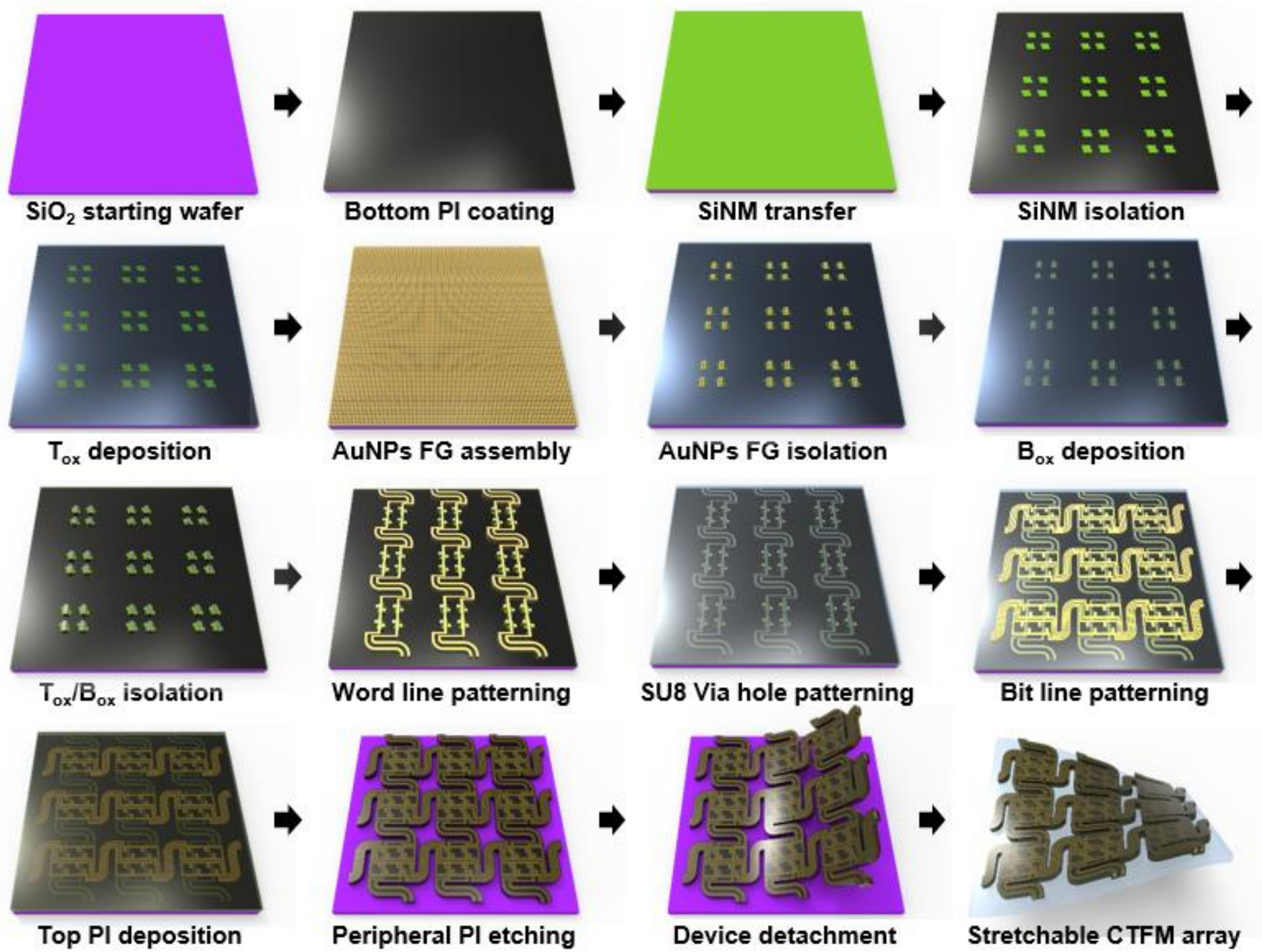

Figure S2: Fabrication process of the CTFM array. Schematic images showing the fabrication process of the stretchable CTFM array.

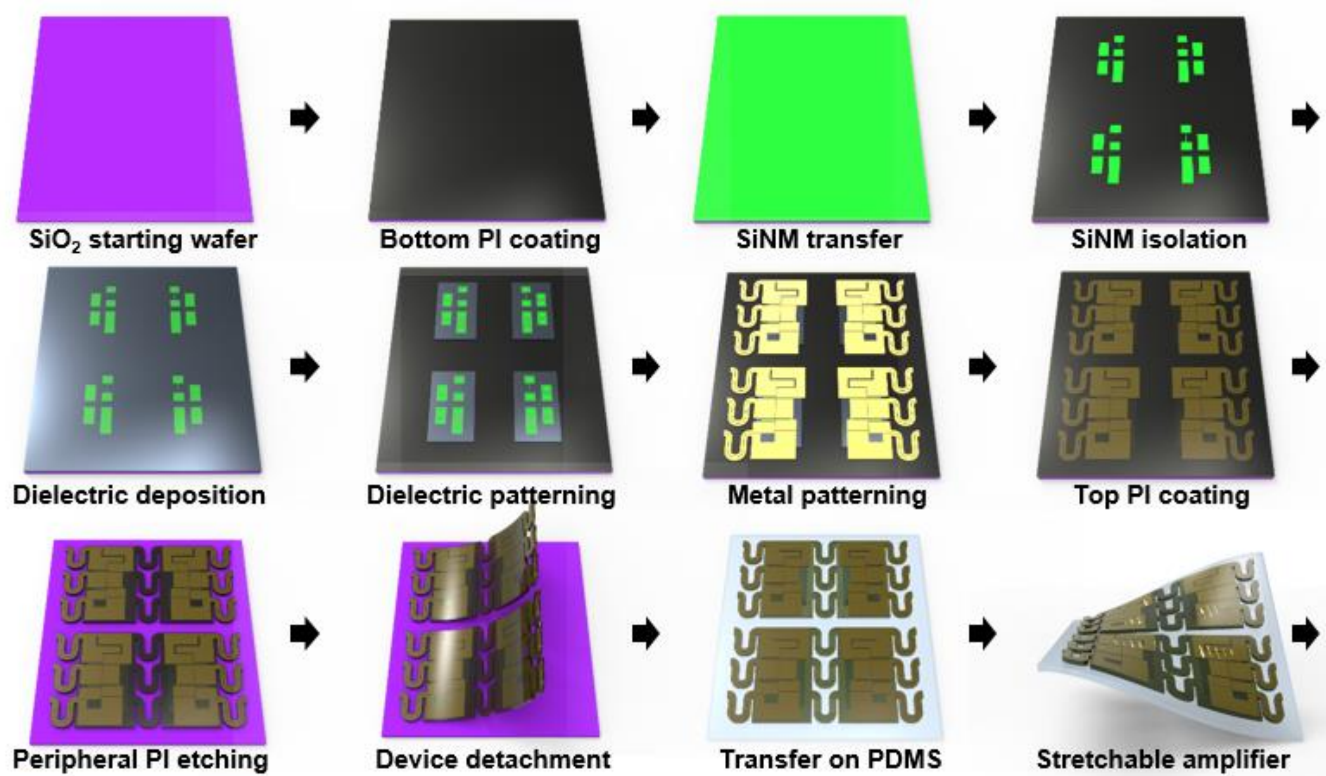

Figure S3: Fabrication process of the pseudo-CMOS inverter array. Schematic images showing the fabrication process of the stretchable pseudo-CMOS inverter.

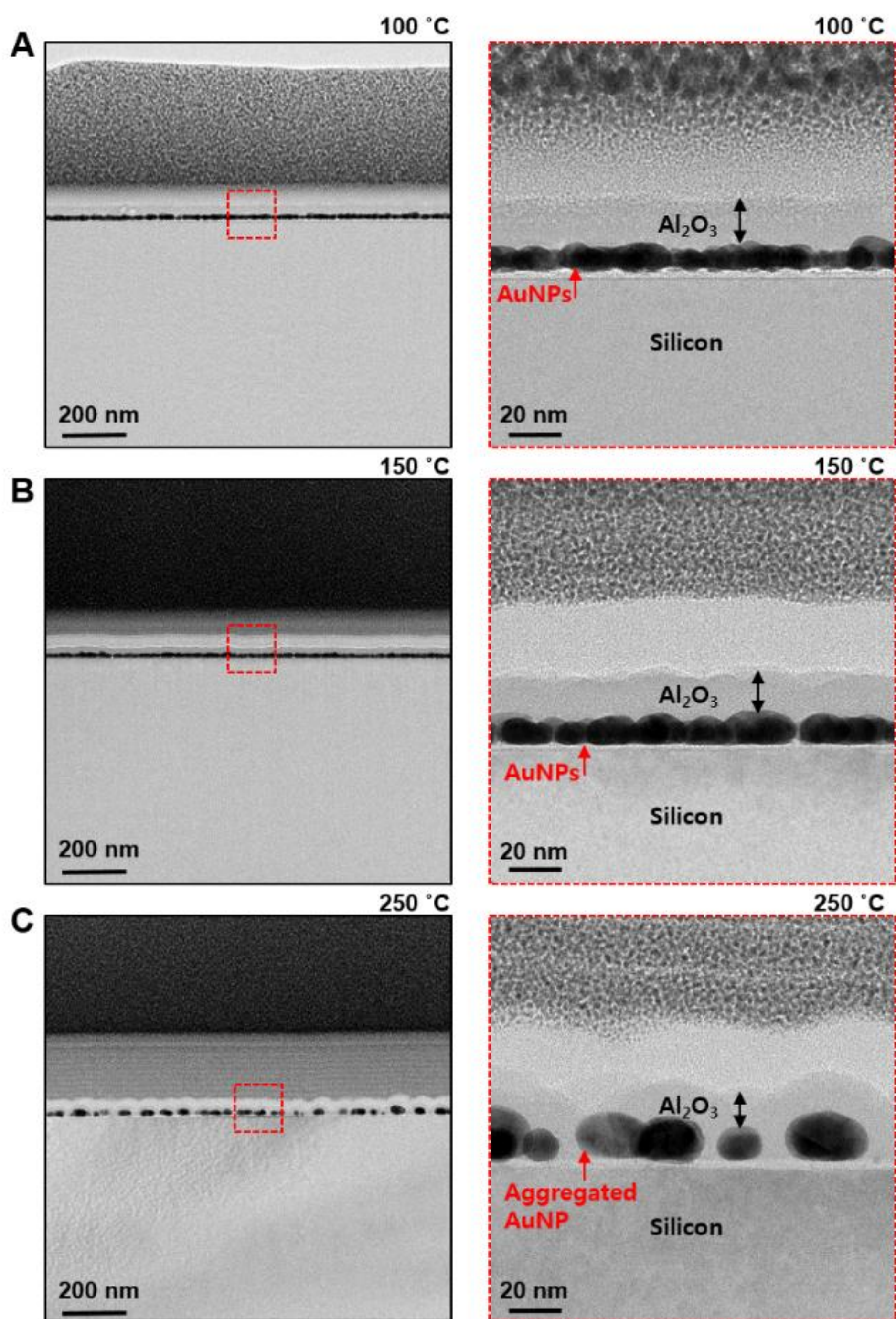

Figure S4: TEM images of AuNP FG assembled using the LB method after the B_{ox} deposition using the PEALD process. (**A-C**) TEM images of AuNP FG assembled by LB method after the B_{ox} deposition using PEALD process under (**A**) 100 °C, (**B**) 150 °C, and (**C**) 250 °C. As shown in the magnified TEM images (red-dashed boxes), morphological transformation of AuNPs is strongly dependent on the process temperature. Specifically, the aggregation of AuNPs are evidently observed when the process temperature approaches to 250 °C.

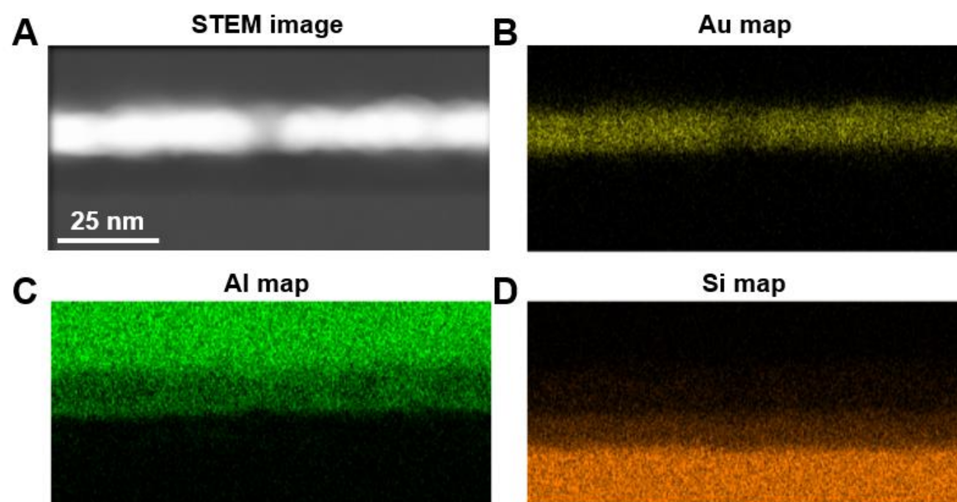

Figure S5: TEM-EDS analysis of AuNPs embedded in an FG cell. (**A**) Cross-sectional scanning TEM (STEM) image of a FG cell containing a AuNP FG. (**B-D**) EDS analysis images obtained by two-dimensional scanning. Yellow, green, and orange colors represent different materials of (**B**) Au, (**C**) Al, and (**D**) Si, respectively.

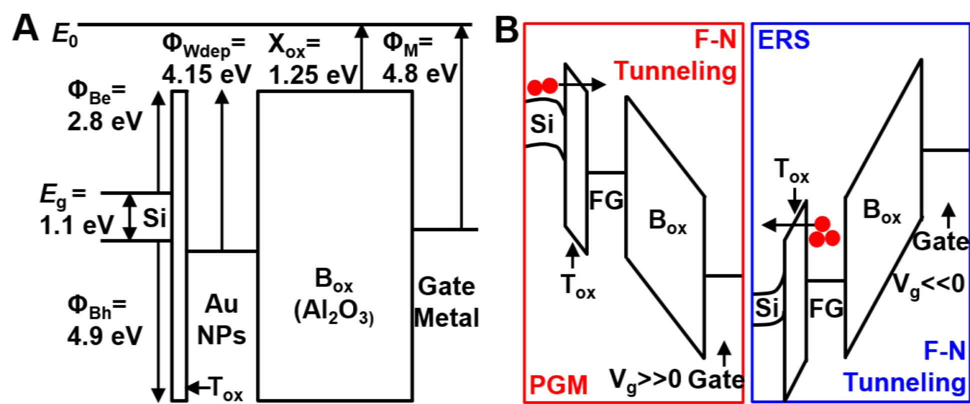

Figure S6: Energy band diagrams of CTFM under three representative bias conditions. (**A**) flat-band condition. (**B**) PGM/ERS operation.

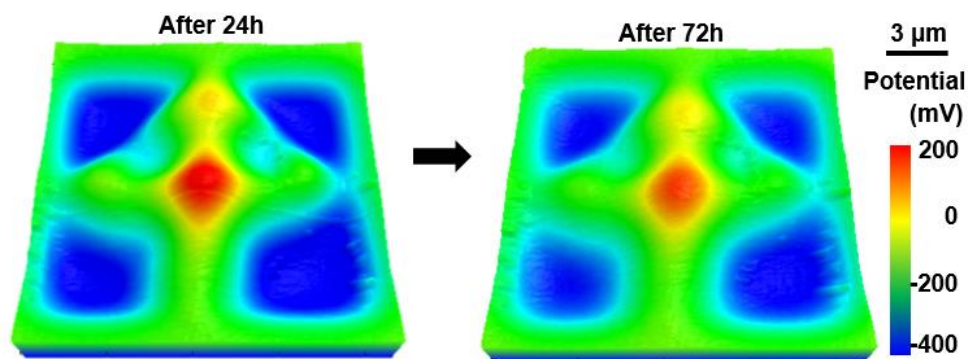

Figure S7: EFM images of the FG cell containing different amounts of charges at different locations according to the elapsed time after charge injection.

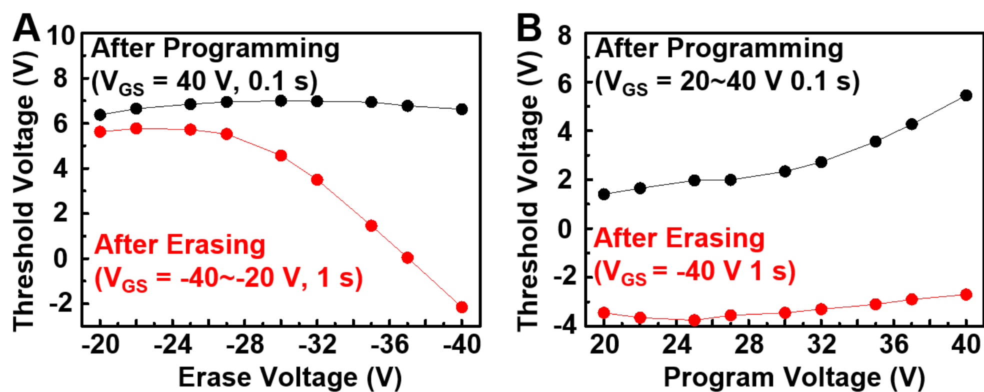

Figure S8: PGM/ERS characteristics with operation voltages. (**A**) Threshold voltage of a CTFM pixel as a function of ERS operation voltage with fixed PGM conditions (V_{GS}, 40 V/pulse width, 0.1 s). (**B**) Threshold voltage of the CTFM cell versus PGM operation voltage with fixed erasing conditions (V_{GS}, -40 V/pulse width, 1 s).

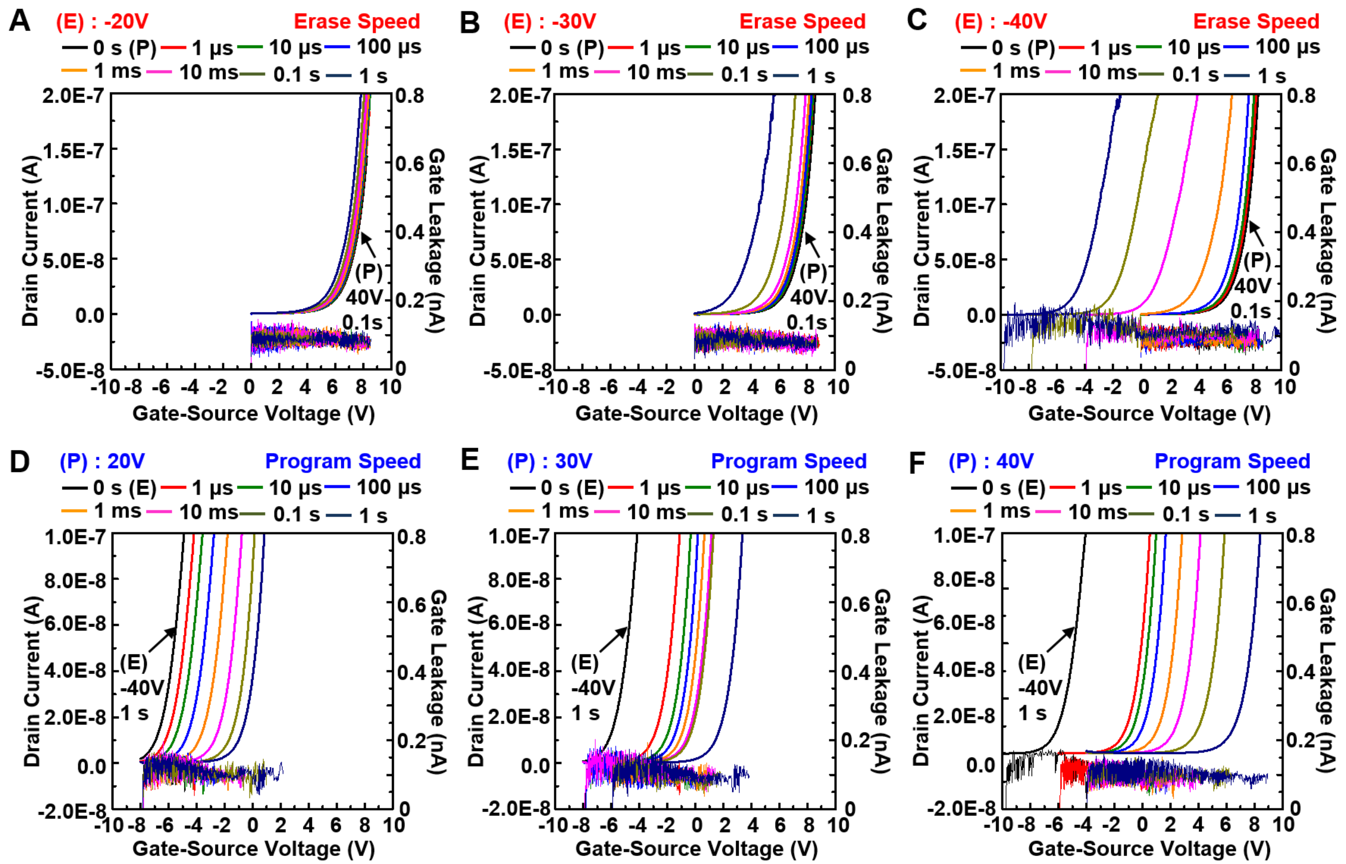

Figure S9: PGM/ERS speed analysis of the CTFM array. (**A-C**) Drain current of a CTFM pixel as a function of gate-source voltage with different pulse widths and fixed ERS voltages ((**A**) -20 V; (**B**) -30 V; (**C**) -40 V) after a PGM operation (40 V, 0.1 s). (**D-F**) Drain current of the CTFM pixel as a function of gate-source voltage with different pulse widths and fixed PGM voltages ((**D**) 20 V; (**E**) 30 V; (**F**) 40 V) after an ERS operation (-40 V, 1 s).

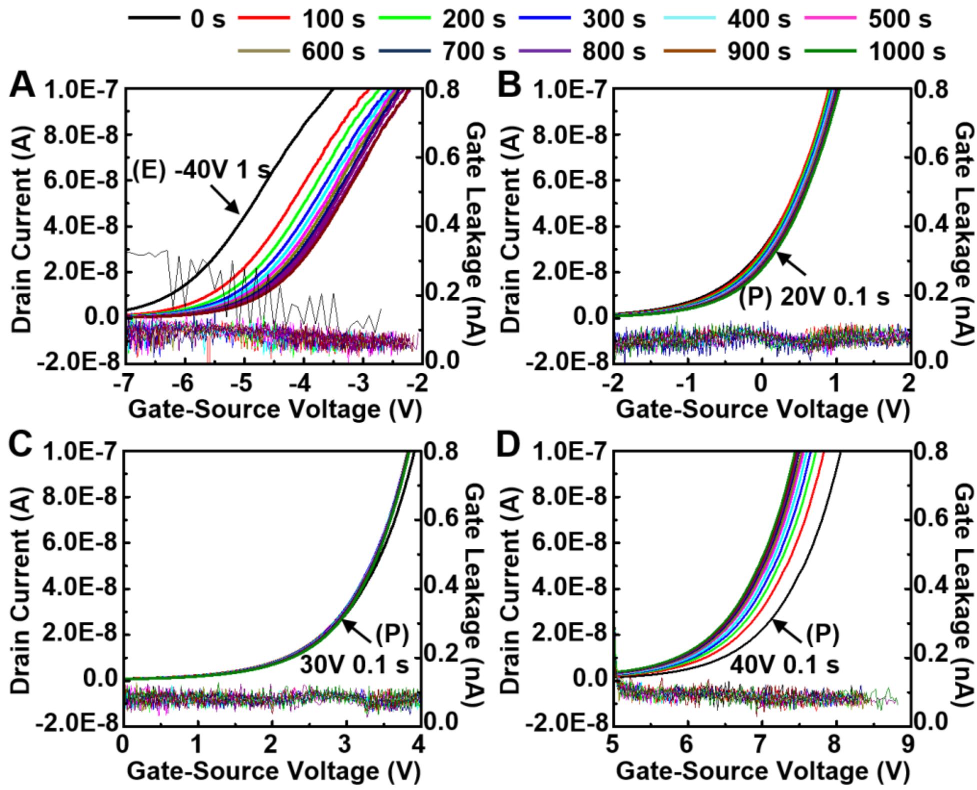

Figure S10: Retention characteristics of a CTFM pixel for different memory states. (**A**) Changes in the transfer curve of the erased CTFM pixel (-40 V, 1 s) during the next 1000 s after an ERS operation. (**B-D**) Changes in the transfer curve of the programmed CTFM pixel ((**B**) 20 V; (**C**) 30 V; (**D**) 40 V) during the next 1000 s after a PGM operation.

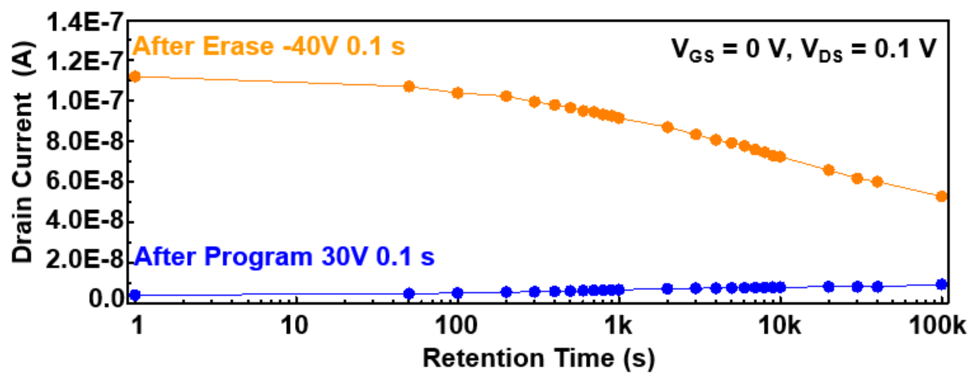

Figure S11: Retention characteristics of the programmed state (30 V, 0.1 s) and the erased state (-40 V, 0.1 s). Drain current levels of each state are read with biases (V_{GS} = 0 V, V_{DS} = 0.1 V).

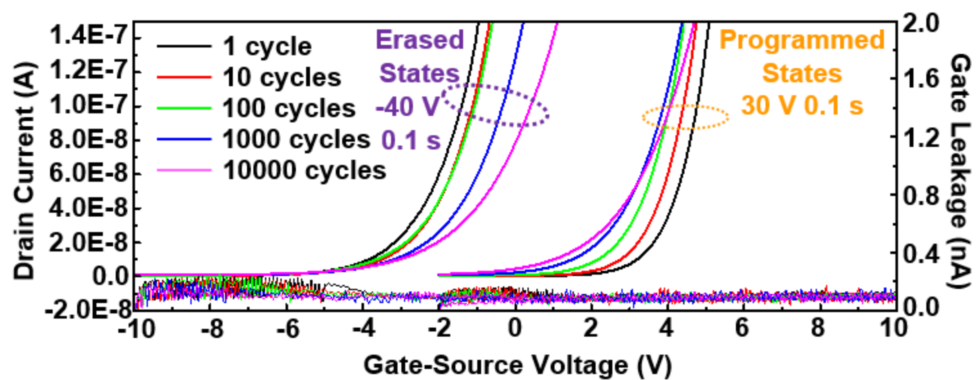

Figure S12: Changes in transfer curves of a CTFM pixel after repetitive PGM and ERS cycles. PGM, 30 V; ERS, -40 V; pulse duration of 0.1 s.

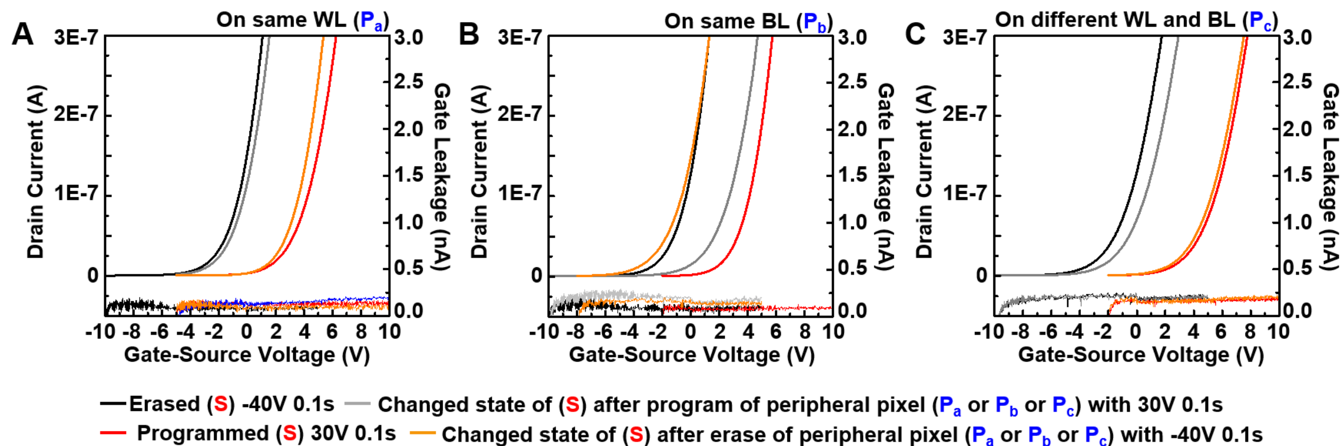

Figure S13: Changes in transfer curves of a CTFM pixel (selected one) after programming or erasing peripheral ones. (**A**) Peripheral pixel on the same WL; (**B**) Peripheral pixel on the same BL; (**C**) Peripheral pixel on the different WL and BL.

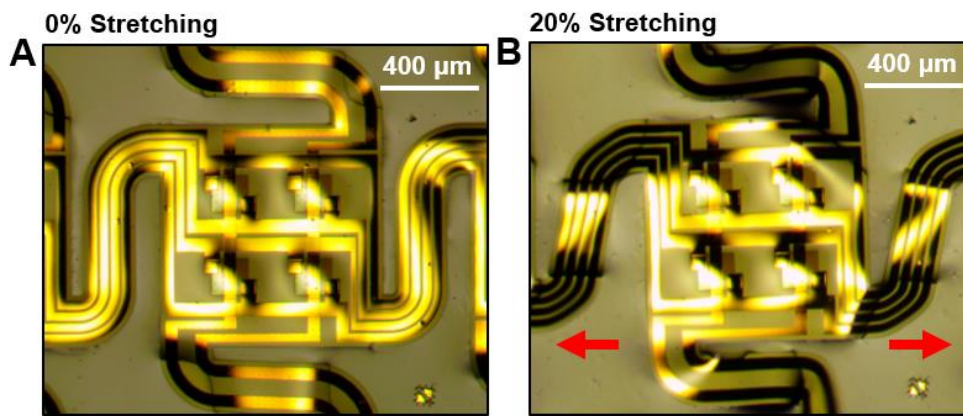

Figure S14: Stretching test of the CTFM pixels. Photographs of (**A**) not stretched (0%) and (**B**) stretched (20%) CTFM array.

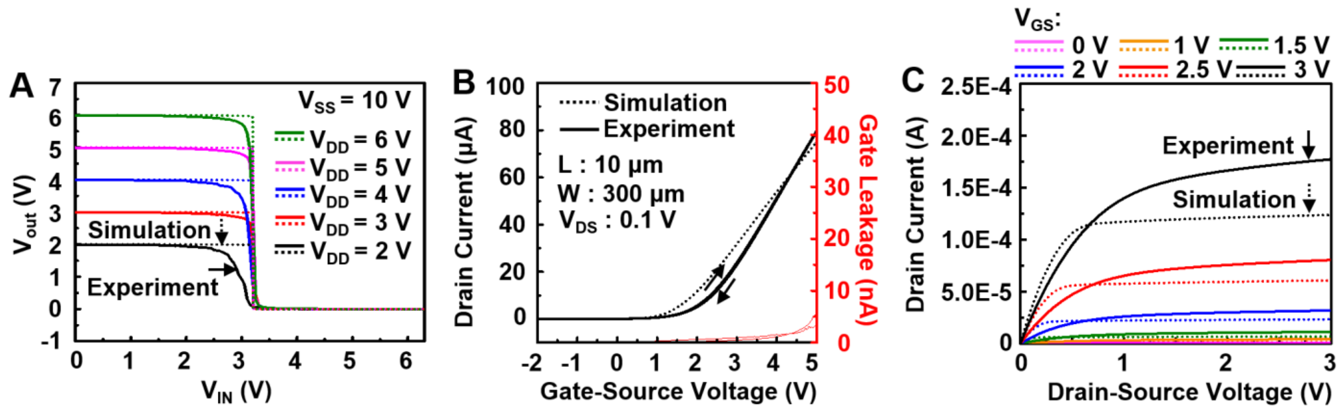

Figure S15: Characteristic curves/simulation results of the pseudo-CMOS inverter and a transistor. (**A**) Voltage transfer characteristic curves of the pseudo-CMOS inverter (dashed line: simulation results; solid line: experimental results) depending on various values of V_{DD} when V_{SS} is fixed to 10 V. (**B**) Transfer curve of a transistor which forms a pseudo-CMOS inverter (solid line) and the simulation result (dashed line). (**C**) Measured I_d-V_d curves of the transistor and the simulation results (dashed line).

Figure S16: PSpice simulation and experimental results of the pseudo-CMOS inverter. (**A**) PSpice schematic showing a circuit diagram of pseudo-CMOS inverter and its design parameters utilized for simulations. (**B**) Characteristic curve of the pseudo-CMOS inverter. Several parameters (V_{OH} = voltage output high; V_{OL} = voltage output low; V_{IL} = voltage input low; V_{IH} = voltage input high; V_M = voltage midpoint) are indicated on the plot. (**C**) Noise margins (NM_L = noise margin low; NM_H = noise margin high) of the pseudo-CMOS inverter as a function of V_{SS}.

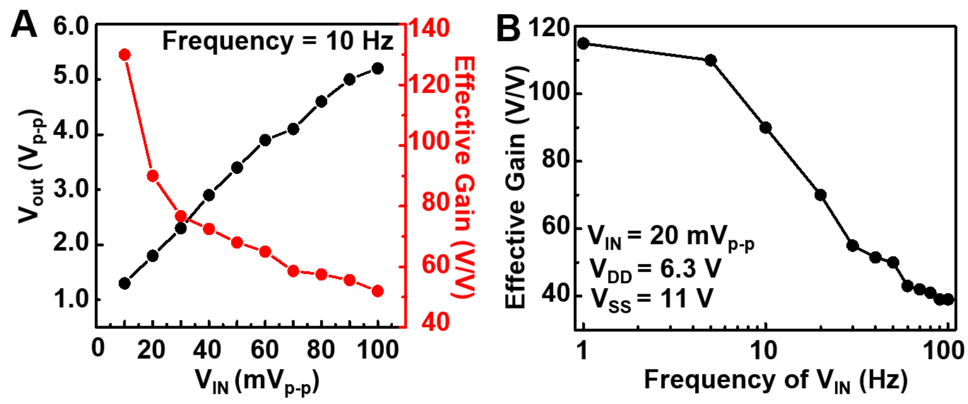

Figure S17: Effective gain and frequency response of the pseudo-CMOS inverter. (A) Effective gain of the pseudo-CMOS inverter as a function of the amplitude of the sinusoidal input signal (10 Hz). **(B)** Frequency response of the effective gain of the pseudo-CMOS inverter when the input signal is sinusoidal and its amplitude is 20 mV_{p-p}.

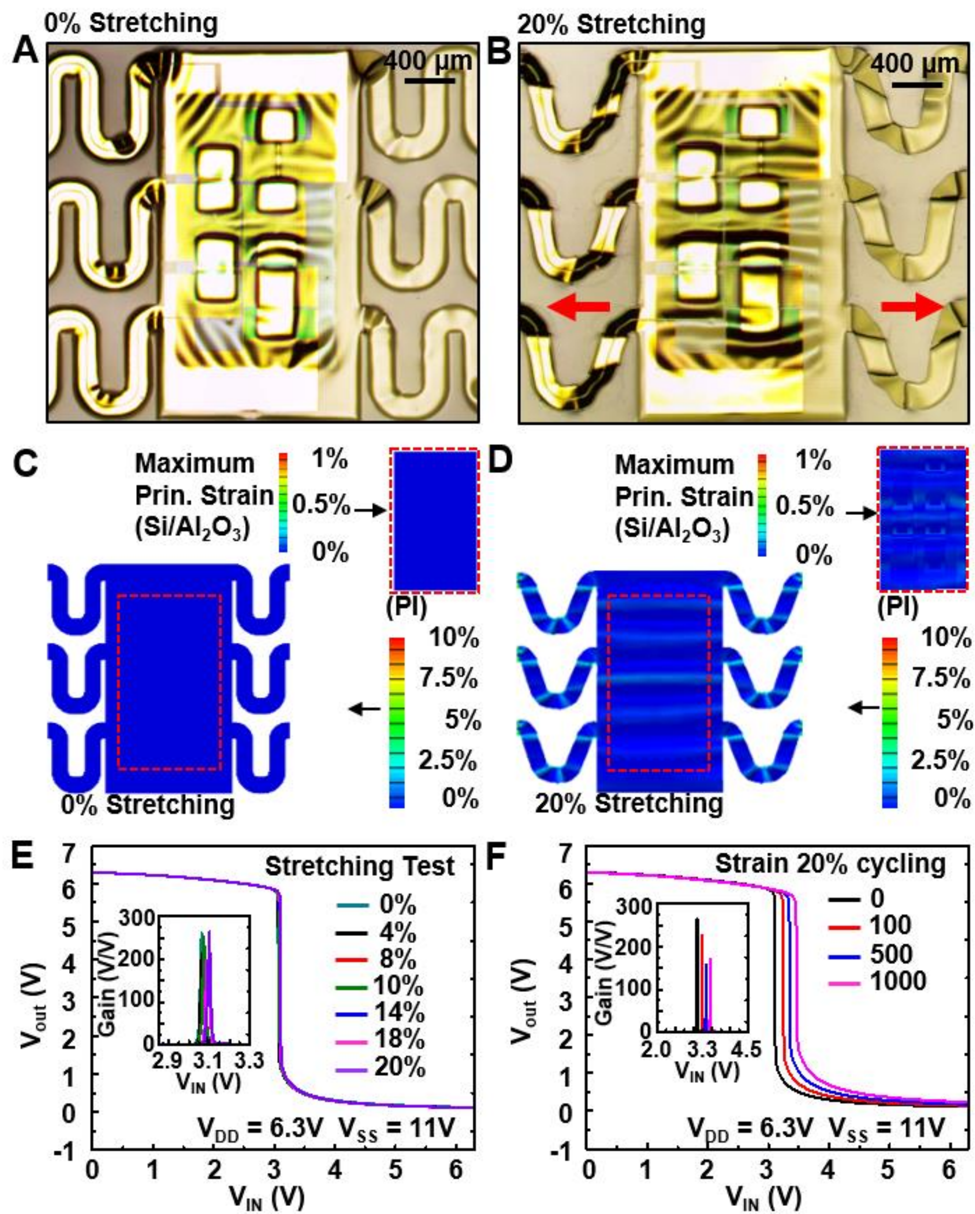

Figure S18: Stretching test of the pseudo-CMOS inverter. Photographs of (**A**) not stretched (0%) and (**B**) stretched (20%) pseudo-CMOS inverter. (**C**,**D**) FEA results showing distribution of maximum principle strain on the entire structure and active region (inset) of the pseudo-CMOS inverter (strain of (**C**), 0%; (**D**), 20%). (**E**,**F**) Voltage transfer characteristics and corresponding gain (inset) of a pseudo-CMOS inverter measured under (**E**) various strains and (**F**) various stretched cycles of 20% strain.

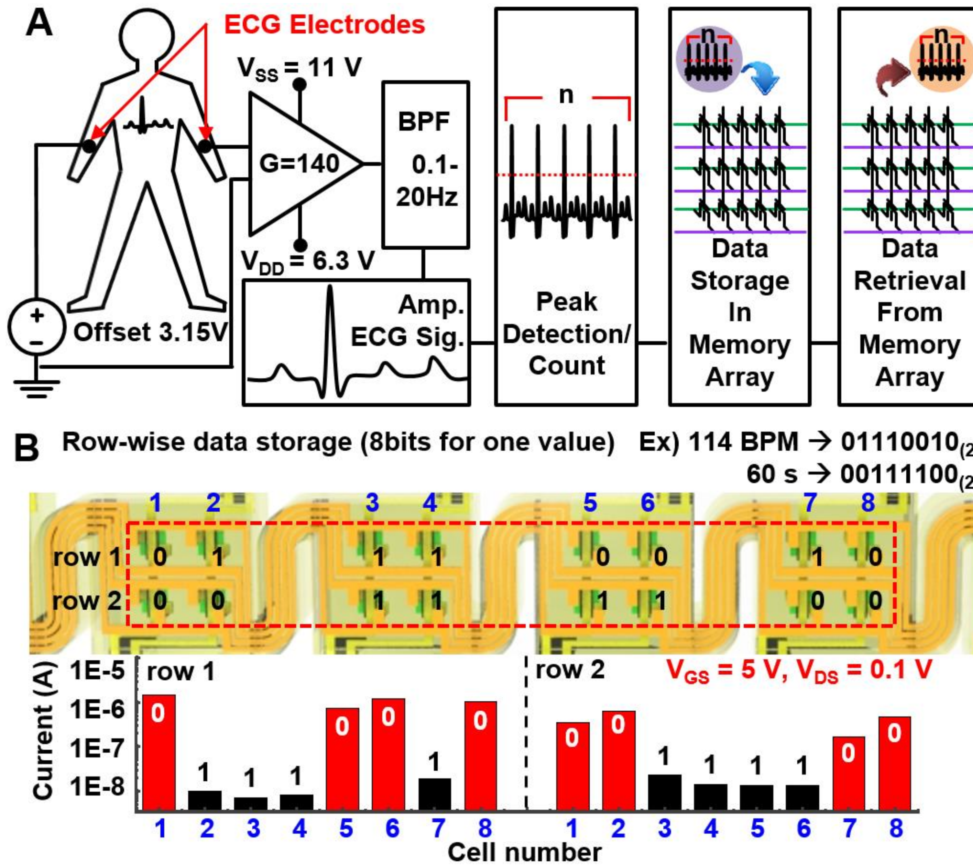

Figure S19: Demonstration procedures and data storage scheme. (**A**) Diagram of overall demonstration process: ECG measurement, amplification, heart rate detection, and data storage and retrieval. (**B**) Schematic showing the scheme of data storage in the CTFM array (top) and the drain current of each memory pixel when a heart rate of 114 BPM and elapsed time of 60 s are stored.

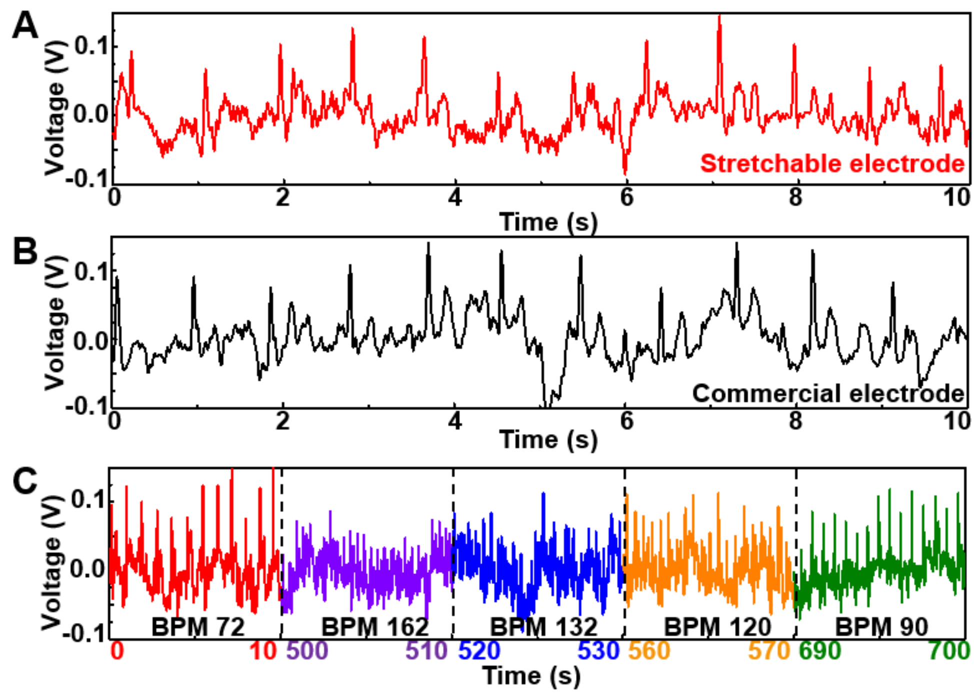

Figure S20: Real-time monitoring of amplified ECG signals. (**A,B**) Amplified ECG signals measured by (**A**) stretchable electrode array; (**B**) commercial electrodes. (**C**) Amplified ECG signals measured before exercise (red) and after exercise (purple, blue, orange, green) showing heart rate recovery.

V_{SS}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	NM_L	NM_H	V_M
6	1.94	3.29	0.00	6.05	3.29	4.11	2.90
8	2.50	3.28	0.00	6.28	3.28	3.78	3.13
10	2.90	3.28	0.00	6.29	3.28	3.39	3.16
12	3.03	3.27	0.00	6.29	3.27	3.26	3.15

Table S1: Noise margins of pseudo-CMOS inverter. Important voltages for calculating noise margins and the calculated noise margins according to V_{SS} when V_{DD} is fixed to 6.3 V.