Soft, Thin Skin-Mounted Power Management Systems and Their Use in Wireless Thermography

Jung Woo Lee[1,2,†], Renxiao Xu[3,†], Seungmin Lee[1,†], Kyung-In Jang[1], Yichen Yang[1], Anthony Banks[1], Ki Jun Yu[1], Jeonghyun Kim[1,2], Sheng Xu[4], Siyi Ma[1], Sung Woo Jang[1,5], Phillip Won[1], Yuhang Li[6], Bong Hoon Kim[1], Jo Young Choe[1], Soojeong Huh[1,7], Yong Ho Kwon[1], Yonggang Huang[3,*], Ungyu Paik[2,*], John A. Rogers[1,*]

[1]Department of Materials Science and Engineering, Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA.

[2]Department of Energy Engineering, Hanyang University, Seoul, 133-791, Republic of Korea.

[3]Department of Mechanical Engineering, Civil and Environmental Engineering, Materials Science and Engineering, and Skin Disease Research Center, Northwestern University, Evanston, IL 60208, USA.

[4]Department of NanoEngineering, Center for Wearable Sensors, Sustainable Power and Energy Center, Materials Science and Engineering Program, University of California, San Diego, La Jolla, CA 92093, USA

[5]Department of Chemical and Biomolecular Engineering (BK21 Program), Korea Advanced Institute of Science and Technology, Daejeon, 305-701, Republic of Korea.

[6]The Solid Mechanics Research Center, Beihang University (BUAA), Beijing 100191, China.

[7]Samsung Display Co. Display R&D Center, Yongin-city, Gyeongki-do 446-711, Republic of Korea.

†These authors contributed equally to this work.

*Correspondence: jrogers@illinois.edu (J.A.R.), upaik@hanyang.ac.kr (U.P.), y-huang@northwestern.edu (Y.H.)

Keywords: solid state lithium ion battery, multi-junction solar cell, stretchable electronics, energy harvest/storage/management, wearable technology

Supplementary Information

Supplementary Note 1: Materials and Methods

Interconnect fabrication. A ~100 μm thick layer of polydimethylsiloxane (PDMS, Sylgard 184) spin-cast on a glass slide and cured on a hotplate at 180 ˚C for 30 min served as a temporary substrate for circuit fabrication. Placing this substrate in an ultraviolet/ozone generator for 4 min created a hydrophilic surface on the PDMS. A polyimide (PI, HD MicroSystems, 4.8 μm) layer spin-cast on top of the PDMS substrate, pre-baked on a hot plate at 150 ˚C for 5 min and then hard-baked in the vacuum oven at 250 ˚C for 75 min formed the base layer for the device. A 500 nm thick layer of Cu deposited with an electron beam evaporator (e-beam evaporator, AJA) formed the active metallization. Photolithography (AZ P4620, AZ 400K) and etching (Type CE-100) defined patterns of electrodes and interconnects in this layer. Another PI (4.8 μm) layer coated on the Cu encapsulated these traces. Deposition of SiO_2 (50 nm) by plasma enhanced chemical vapor deposition (PECVD, Plasma-Therm) yielded a layer for a hard etching mask. Photolithography and reactive ion etching of the SiO_2 (RIE, Plasma-Therm, 20 SCCM CF_4, 100 W, 50 mT) and PI (RIE, March, 20 SCCM O_2, 150 W, 195 mT) and then the PI defined features to match the geometry of the underlying Cu traces. Immersion in buffered oxide etchant removed the remaining SiO_2. A water soluble tape (Aquasol, USA) facilitated transfer of the resulting stack to a stretchable substrate.

Substrate preparation and encapsulation. Mixing a base and curing agent for a silicone elastomer (Ecoflex, Smooth-on inc., E~60 kPa) at a weight ratio of 1:2 and then spin casting

at 250 rpm for 3 min and curing at room temperature overnight yielded a soft, stretchable substrate with thickness of ~300 µm. An ultra-low modulus silicone material (Silbione 4717, Bluestar, E~3 kPa) also mixed in a 1:2 (A:B) weight ratio spin-coated at 300 rpm for 6 min on top of this substrate defined the based layer of the soft core for the devices. After transfer printing the electrode/interconnect stack and bonding the components, another layer of ultra-low modulus silicone material and silicone elastomer encapsulated the system to complete the fabrication.

Component assembly. The solid state battery components are in a bare die format (Enerchip CBC005 and Enerchip CBC050, Cymbet, ~ 200 µm thick) with Au ball bumps on both anode/cathode electrodes to enable contacts via wire ball bonding (4524 Wire Ball Bonder, Kulicke & Soffa). An impregnable insulation resin (IR0001, TEMCO) applied at the edge of the solar cells (GaAs/InGaP dual junction, MicroLink, ~ 32 µm thick) and cured at 150 °C for 3 hr passivated the p-type contacts. A flip-chip method allowed assembly of components on the metal electrodes using $In_{97}Ag_3$ alloy solder paste (Indalloy 290, Indium Corporation) with heating at 190 °C for 1 min.

Mechanical testing of the device. An array of circular disks (200 µm radius) of chromium (100 nm thick) deposited on the substrate through a shadow mask by electron beam evaporation facilitated optical analysis of the distributions of strain. A customized uniaxial/biaxial stretcher provided means for inducing controlled deformations. A single-lens reflex camera captured images at different deformation levels. A dynamic mechanical analyzer (TA instruments, Q800) yielded the stress/strain curves, under uniaxial tensile loading. In addition, a DC sourcemeter (model 2400, Keithley) allowed measurement of the *I-V* characteristics under biaxial stretching to confirm the mechanical/electrical integrity of

the contact pads and interconnects. A flexural endurance tester (CK Trade, Korea) enabled cyclic testing through sets of 1000 cycles at 0.5 Hz. Measurements of the solar cell and battery array performance occurred before deformation and after 1, 100, 500, 1000 cycles of uniaxial stretching.

Characterization of the device performance. An AM 1.5G solar simulator (91192, Oriel) combined with a DC sourcemeter (model 2400, Keithley) allowed measurements of the *I-V* characteristics of the solar cell array. A Gamry Reference 600 (Gamry Instruments, Warminster, PA) in a two-electrode cell configuration enabled galvanostatic evaluation at room temperature. The cut-off voltage was between 4.1 and 3.0 V during charge/discharge steps. Chronopotentiometry methods yielded information on the solar cell and battery integrated in a folded geometry. The working and counter/reference electrodes connected to positive and negative output voltage pads of the system, respectively.

NFC Data-logging. Photolithographic patterning techniques applied to Cu foils (18 μm) yielded stretchable NFC coils. A commercial NFC chip (RF430FRL152H 15xH NFC ISO 15693 Sensor Transponder, Texas Instruments) provided for temperature sensing, data storage and voltage regulation, with a releasable battery backup as a power module. The regulated working voltage ranges from 1.45 to 1.65 V. The chip includes a microcontroller (MSP430), with 2kB, 4kB and 8kB of FRAM, SRAM and ROM, respectively. A customized NFC reader collected and recorded temperature data wirelessly after measurement with data-logging. An impedance analyzer (4291A RF impedance/material analyzer, Hewlett Packard) was used for electromagnetic characterization. As a control experiment, the NFC (SL13A, AMS) device collected data every 1 min with operation of a standard, NFC equipped smartphone (Galaxy Note 4, Samsung).

Mechanical Analyses of Fully-encapsulated/ Fully-bonded Cell Arrays: FEA. Full three-dimensional (3D) FEA was used to analyze the post-buckling deformation, plastic yielding and fracture of serpentine interconnects under uniaxial/biaxial stretching and compression. The results also defined the elastic stretchability (or interchangeably used "reversibility") and total stretchability for interconnects with different geometric patterns and cross-section. The simulation results presented in this work used commercial FEA software (ABAQUS). In each FEA model, elastomeric composite silicone (Ecoflex/Silbione) substrates and superstrates, as well as the comparatively thick battery cells were modeled employing 8-node hexahedral brick solid elements (C3D8R), while the thin PI (4.8 um)/Cu (0.5 um)/PI (4.8 um) -layered serpentine interconnects and solar cells employed quadrilateral shell elements S4R, defined by composite layups. Refined meshes yielded accurate results. Since the adhesion between the PI and elastomeric surfaces was good, FEA models assumed that the serpentine interconnects were perfectly bonded to the elastomer. The material properties, namely effective elastic modulus (E) and Poisson's ratio (ν) were $E_{Silbione}$=0.003 MPa and $\nu_{Silbione}$=0.499 for Silbione; $E_{Ecoflex}$=0.06 MPa and $\nu_{Ecoflex}$=0.499 for Ecoflex; E_{Cu}=119 GPa and ν_{Cu}=0.34 for copper; E_{PI}=2.5 GPa and ν_{PI}=0.34 for PI; and $E_{Semiconductor}$=85.9 GPa and $\nu_{Semiconductor}$=0.34 for semiconductor components like solar cells and batteries.

Since both solar cell and battery arrays and their interconnects have periodicity in two planar directions x and y, a representative "unit cell" was initially studied in design optimization for maximum elastic stretchability. For serpentine interconnects, the elastic stretchability (or reversibility) $\varepsilon_{ict-elastic-stretch}$ was defined as the maximum applied strain before plastic yielding. Total stretchability $\varepsilon_{ict-total-stretch}$, on the other hand, was similarly defined for the fracture strain ~5% of the material. After iterative FEA-based design

optimization, the final interconnect geometry was found to be a simple serpentine pattern connecting the edge mid-points of two adjacent cells, with parameters detailed in Supplementary Fig. S6a. Since the much more rigid component (solar cell or battery) islands remain almost unaffected during deformation, interconnect stretchability (both elastic and total) can be converted to their corresponding system-level stretchability via:

$$\varepsilon_{sys-elastic-stretch} = \left(1 - \sqrt{\eta}\right) * \varepsilon_{ict-elastic-stretch}$$

$$\varepsilon_{sys-total-stretch} = \left(1 - \sqrt{\eta}\right) * \varepsilon_{ict-total-stretch}$$

, where η is the areal coverage of electronic components.

Supplementary Note 2: Fabrication procedures.

1) Energy device fabrication

Carrier substrate preparation

1. Clean a glass slide with acetone, IPA, and DI water.
2. Spin coat polydimethylsiloxane (PDMS; Sylgard 184) at 1500 rpm, 1 min.
3. Cure on a hot plate at 180 °C for 30 min.

Metal deposition and patterning

4. Expose PDMS/glass substrate to UV-ozone for 4 min.
5. Spin coat twice poly(pyromellitic dianhydride-co-4,4'-oxydianiline) amic acid solution (PI, PI 2545, HD Microsystems) at 1500 rpm for 1 min.
6. Soft-bake the substrate on a hot plate at 150 °C for 5 min.
7. Cure in a hot oven at 250 °C for 75 min.
8. Deposit 500 nm thickness of Cu using an e-beam evaporator (AJA International Inc.).
9. Spin coat photoresist (AZ 4620) at 3000 rpm for 30 s.
10. Cure on a hot plate at 110 °C for 3 min.
11. Align iron oxide mask and expose UV for 300 mJ cm^{-2}.
12. Develop in aqueous developer (AZ 400 K).
13. Etch Cu with Cu etchant (CE-100, Transense).
14. Remove photoresist with acetone and IPA.
15. Spin coat twice poly(pyromellitic dianhydride-co-4,4'-oxydianiline) amic acid solution (PI, PI 2545, HD Microsystems) at 1500 rpm for 1 min.
16. Soft-bake the substrate on a hot plate at 150 °C for 5 min.
17. Cure in a hot oven at 250 °C for 75 min.

Device Isolation

18. Deposit 50 nm thickness of SiO_2 using an e-beam evaporator (AJA International Inc.).
19. Spin coat photoresist (AZ 4620) at 3000 rpm for 30 s.

20. Cure on a hot plate at 110 °C for 3 min.

21. Align iron oxide mask and expose UV for 300 mJ cm^{-2}.

22. Develop in aqueous developer (AZ 400 K).

23. Remove SiO_2 with reactive ion etching (RIE, Plasma-Therm) at 50 mTorr, 20 SCCM CF_4, 100 W, 10 min.

24. Remove PI with reactive ion etching (RIE, March) at 195 mTorr, 20 SCCM O_2, 150 W, 1500 s.

25. Clean with acetone and IPA.

26. Remove oxide with buffered oxide etch.

Retrieval and transfer printing

27. Retrieve the patterns using water soluble tape (Aquasol, USA).

28. Transfer the patterns on the Core/Shell substrate.

29. Remove water soluble tape with water.

Component assembly

30. Ball bond bare die components with wire ball bonder(4524 Wire Ball Bonder, Kulicke & Soffa) and passivate the components with impregnable insulation resin (IR0001, TEMCO).

31. Remove native oxide from the surface of the patterns with oxide remover.

32. Solder using $In_{97}Ag_3$ alloy solder paste (Indalloy 290, Indium Corporation) with heating at 190 °C for 1 min.

33. Encapsulation with Core/Shell superstrate.

2) NFC device fabrication

Carrier substrate preparation

1. Spin coat poly(pyromellitic dianhydride-co-4,4’-oxydianiline) amic acid solution (PI, PI 2545, HD Microsystems) at 4000 rpm for 1 min on Cu foil (18 μm thick, Oak Mitsui Micro-thin series).

2. Soft-bake the substrate on a hot plate at 150 °C for 5 min.

3. Cure in a hot oven at 250 °C for 75 min.

4. Clean a glass slide with acetone, IPA, and DI water and spin coat polydimethylsiloxane (PDMS; Sylgard 184) at 1500 rpm, 1 min. Cure it at room temperature overnight.

5. Laminate PI coated Cu foil.

#1 Metal layer patterning

6. Spin coat photoresist (AZ 4620) at 3000 rpm for 30 s and cure on a hot plate at 110 °C for 3 min.

7. Align iron oxide mask and expose UV for 300 mJ cm^{-2} and develop in aqueous developer (AZ 400 K).

8. Etch Cu with Cu etchant (CE-100, Transense) and remove photoresist with acetone and IPA.

Via hole patterning

9. Spin coat poly(pyromellitic dianhydride-co-4,4'-oxydianiline) amic acid solution (PI, PI 2545, HD Microsystems) at 4000 rpm for 1 min on it.

10. Soft-bake the substrate on a hot plate at 150 °C for 5 min and cure it in a hot oven at 250 °C for 75 min.

11. Spin coat photoresist (AZ 4620) at 3000 rpm for 30 s and cure it on a hot plate at 110 °C for 3 min.

12. Align iron oxide mask and expose UV for 300 mJ cm^{-2} and develop in aqueous developer (AZ 400 K).

13. Remove PI with reactive ion etching (RIE, March) at 195 mTorr, 20 SCCM O_2, 150 W, 600 s.

14. Remove photoresist with acetone and IPA.

#2 Metal layer patterning

15. Deposit 1 μm thickness of Cu using an e-beam evaporator (AJA International Inc.).

16. Spin coat photoresist (AZ 4620) at 3000 rpm for 30 s and cure it on a hot plate at 110 °C for 3 min.

17. Align iron oxide mask and expose UV for 300 mJ cm^{-2} and develop in aqueous developer (AZ 400 K).

18. Etch Cu with Cu etchant (CE-100, Transense).
19. Clean with acetone and IPA.
20. Spin coat poly(pyromellitic dianhydride-co-4,4'-oxydianiline) amic acid solution (PI, PI 2545, HD Microsystems) at 4000 rpm for 1 min on it.
21. Soft-bake the substrate on a hot plate at 150 °C for 5 min and cure it in a hot oven at 250 °C for 75 min.

Device Isolation

22. Deposit 50 nm thickness of SiO_2 using an e-beam evaporator (AJA International Inc.).
23. Spin coat photoresist (AZ 4620) at 3000 rpm for 30 s.
24. Cure on a hot plate at 110 °C for 3 min.
25. Align iron oxide mask and expose UV for 300 mJ cm^{-2}.
26. Develop in aqueous developer (AZ 400 K).
27. Remove SiO_2 with reactive ion etching (RIE, Plasma-Therm) at 50 mTorr, 20 SCCM CF_4, 100 W, 10 min.
28. Remove PI with reactive ion etching (RIE, March) at 195 mTorr, 20 SCCM O_2, 150 W, 1500 s.
29. Clean with acetone and IPA.
30. Remove oxide with buffered oxide etch.

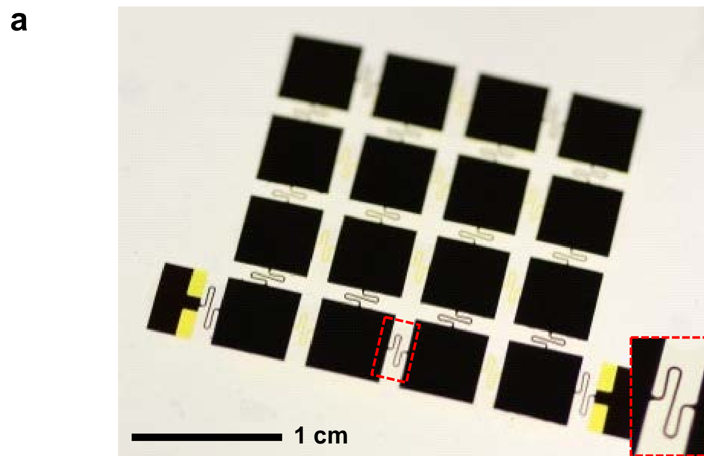
Retrieval and transfer printing

31. Retrieve the patterns using water soluble tape (Aquasol, USA).
32. Transfer the patterns on the Core/Shell substrate.
33. Remove water soluble tape with water.

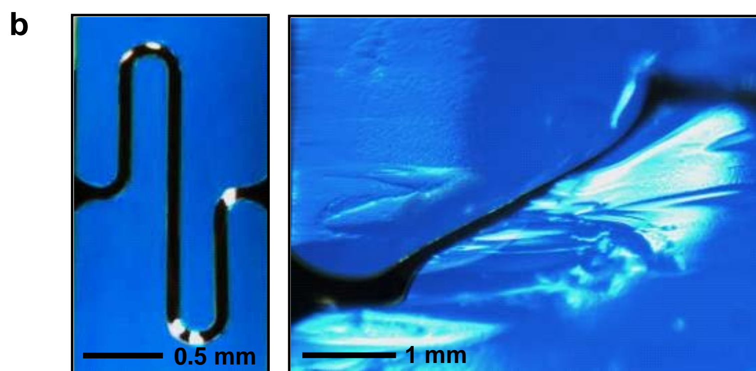
Component assembly

34. Remove native oxide from the surface of the patterns with oxide remover.
35. Solder using $Sn_{42}Bi_{58}$ alloy solder paste (SMDLTLFP-ND, Chip Quik Inc.) with heating at 190 °C for 1 min.

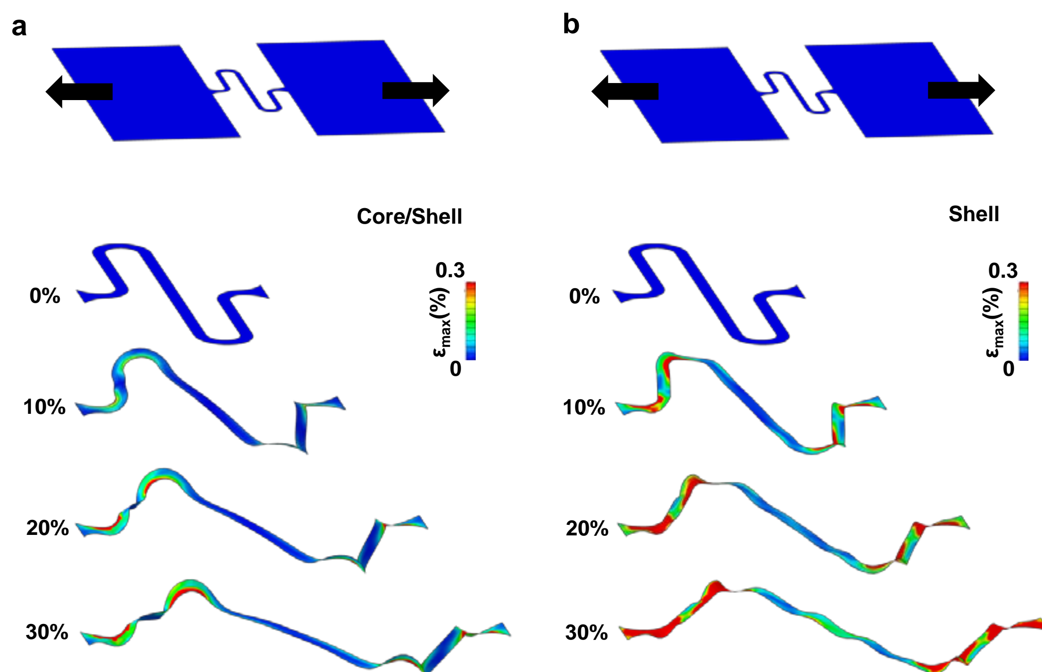
a



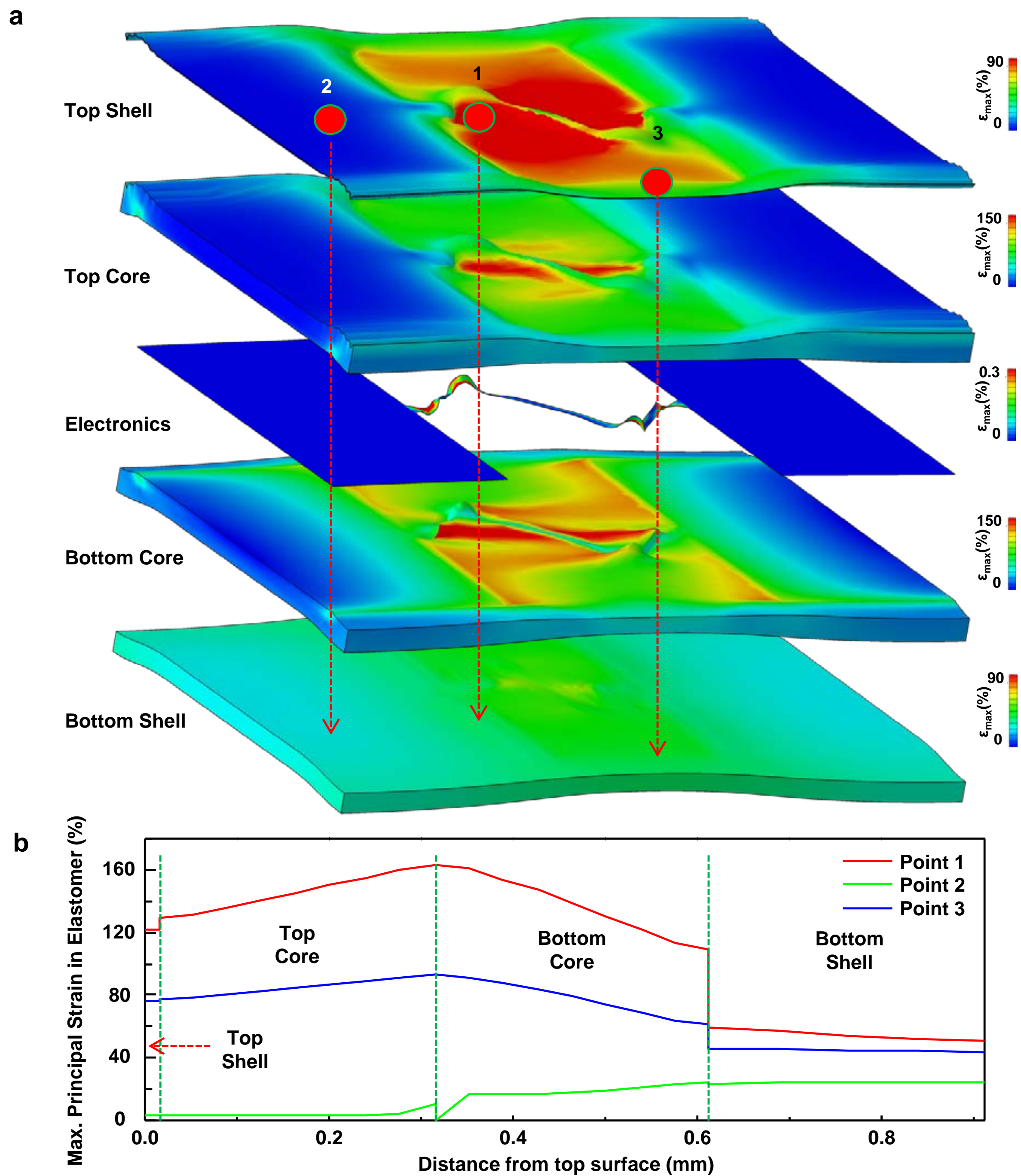
b



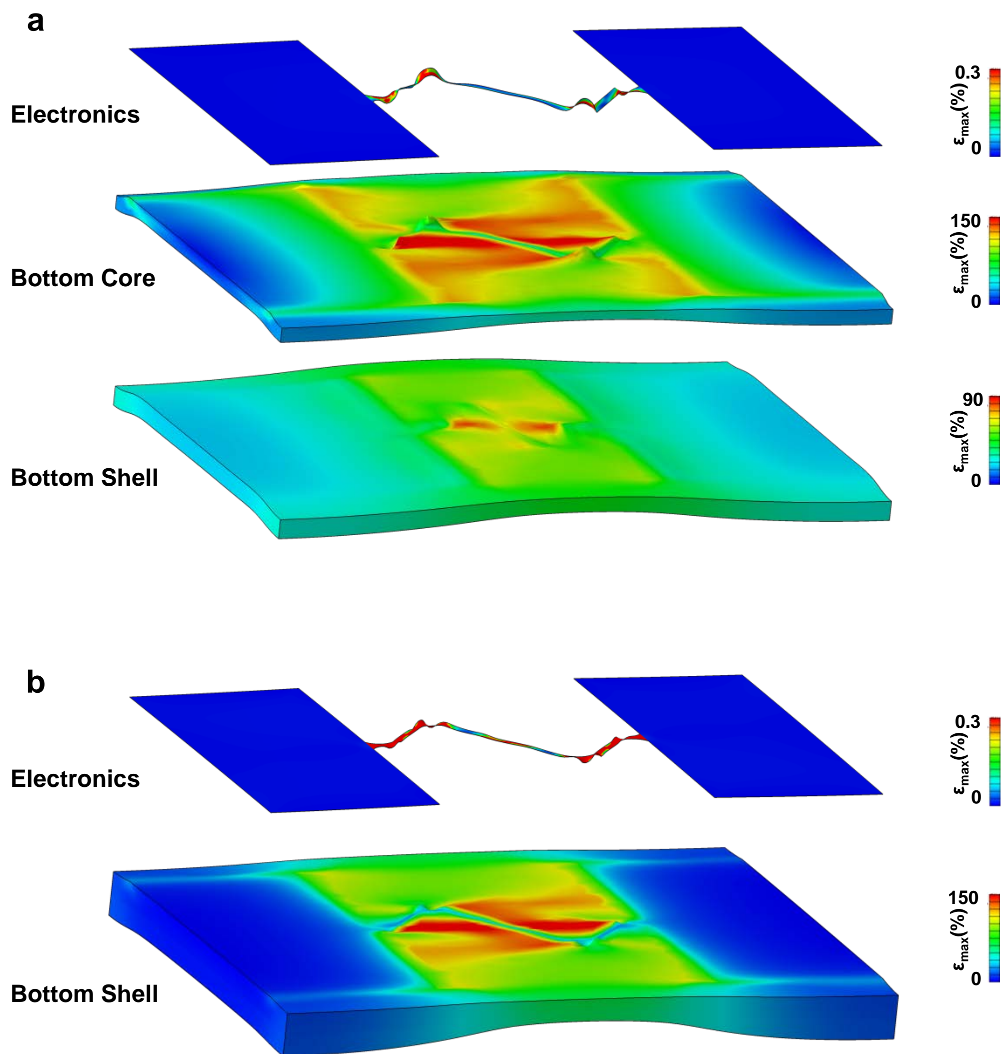
Supplementary Figure S1 | Images of a system that includes a 4x4 array of 2J solar cells and magnified view of one of the interconnects during stretch. (a) 4 X 4 array of solar cells and interconnect (inset). (b) Deformation of an interconnect on a layer of core material from an initial (0%) to a stretched (30%) state.



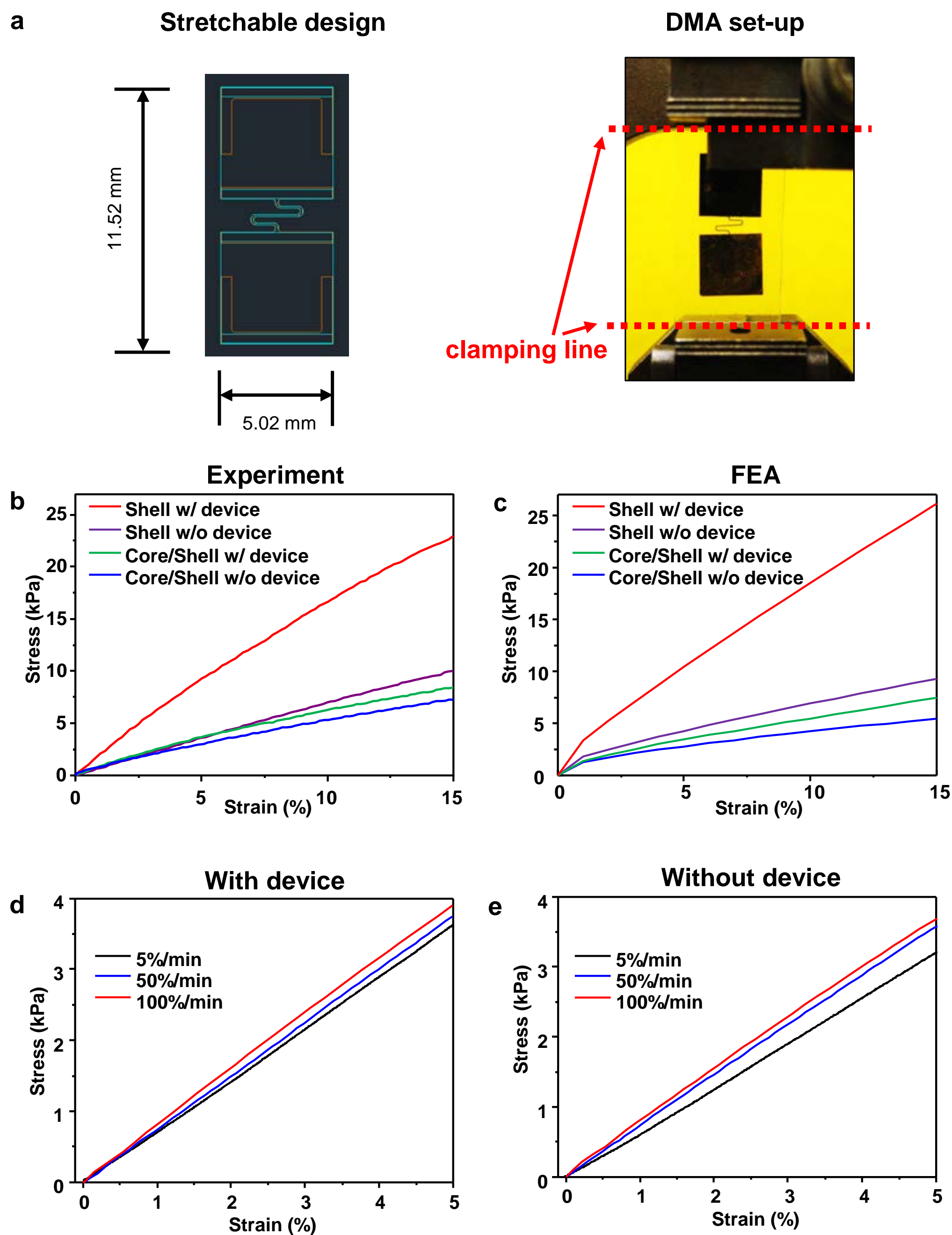
Supplementary Figure S2 | Comparison of 3D-FEA modeling of a unit cell during uni-axial tension. Stretchable units with (a) core-shell encapsulation and (b) encapsulation only with the shell material, both stretched from 0% to 30%. The results highlight strains in the metal layer of the interconnect structure.



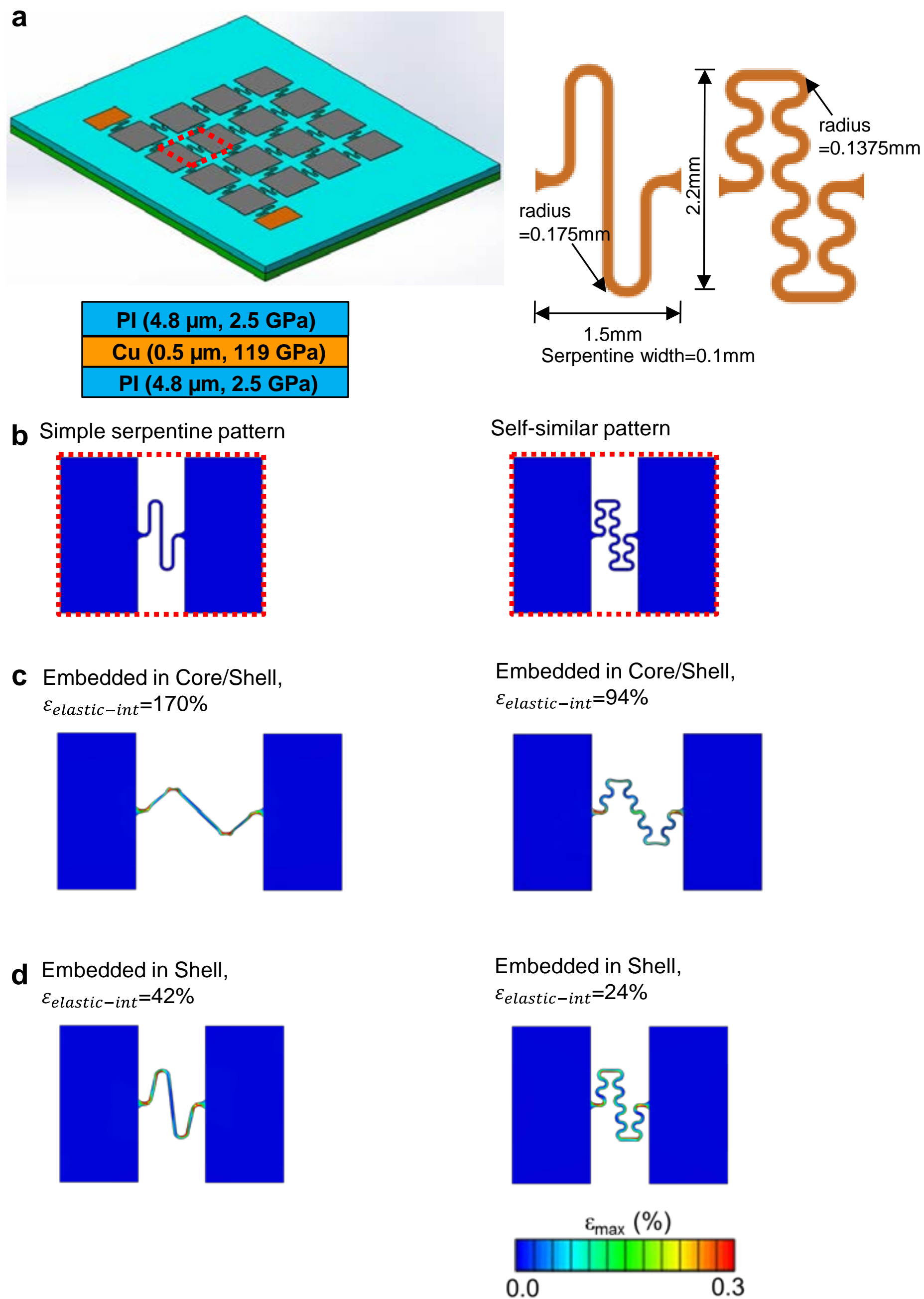
Supplementary Figure S3 | 3D-FEA results of the device components z-axis strain distribution with spatial mapping. (a) Full geometry view of 3D-FEA results of Fig. 1e and (b) maximum principal strain across the thickness direction for three different locations across a system with core-shell design. The strain in the elastomer reaches a peak value in the plane of electronics for the most severely deformed location



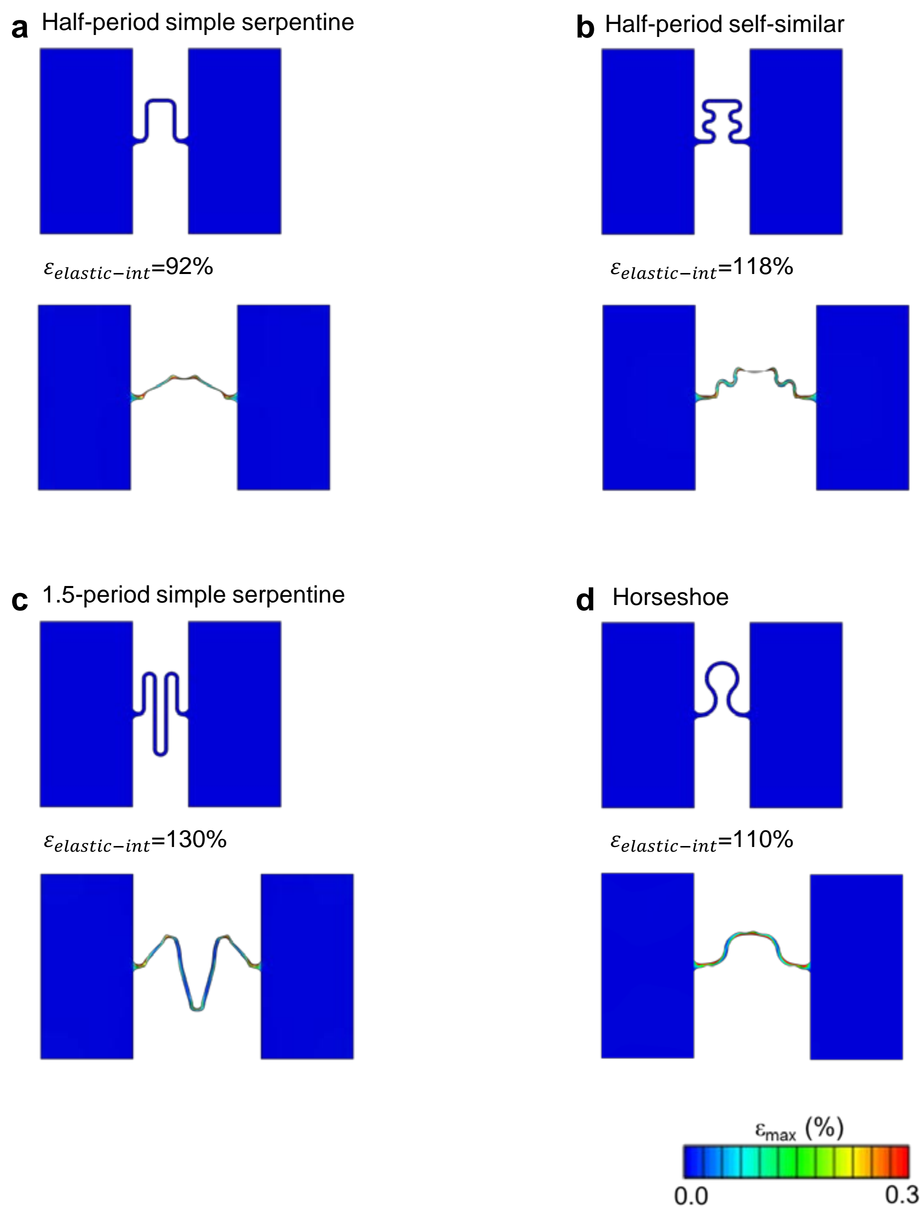
Supplementary Figure S4 | 3D-FEA modeling results for the distribution of strains in different layers of a single unit cell upon uniaxial elongation. The two cases correspond to (a) core-shell encapsulation with insufficient core thickness (200 µm with t_{PI}=4.8 µm; Fig. 1e) and (b) encapsulation only with the shell material, both stretched to ~39%, corresponding to an elongation of 170% in the interconnects.



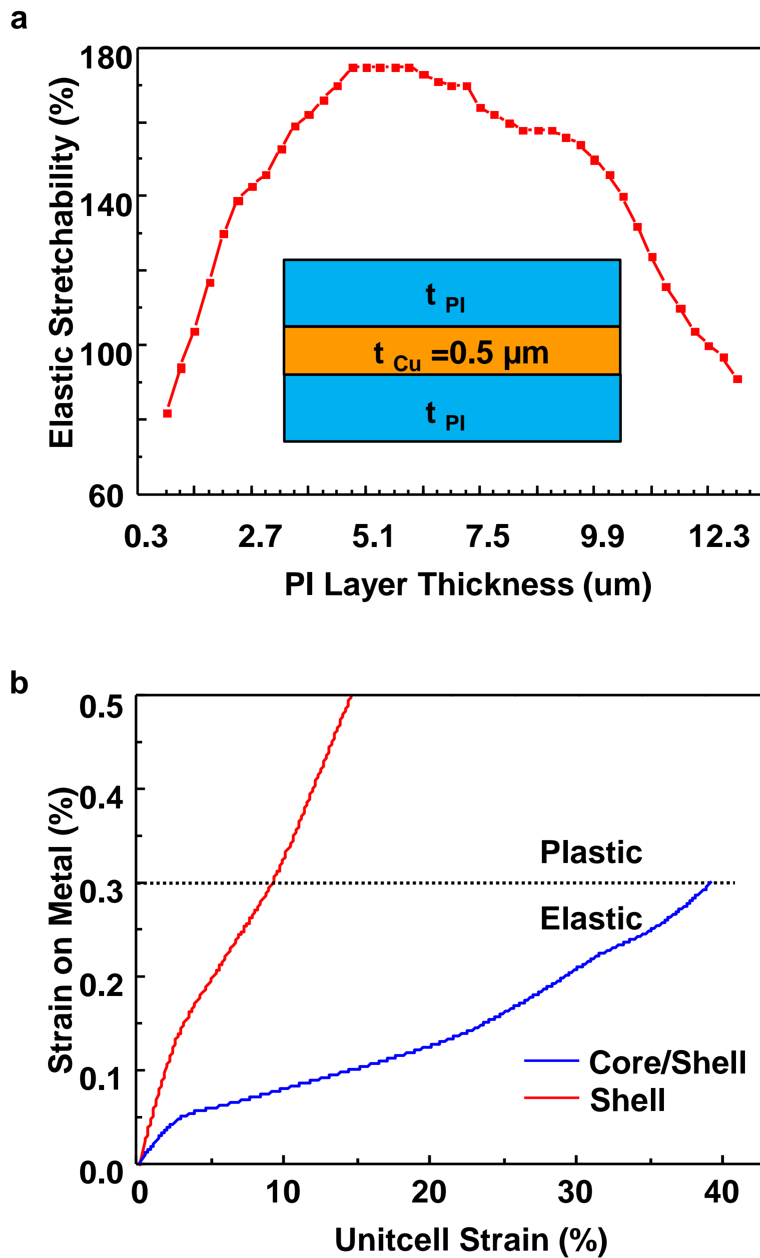
Supplementary Figure S5 | Experimental and computational studies of strain decoupling, and rate dependent moduli. (a) Layout of the test structure and image of a corresponding device mounted in a clamp used for DMA measurements. Stress/strain curves from (b) experiment and (c) 3D-FEA. Stress/strain curves of the Core/Shell (d) with and (e) without the device components at different strain rates (5% / min, 50% / min, 100% / min).



Supplementary Figure S6 | 3D-FEA modeling results for different interconnect designs. (a) Schematic illustration and dimensions of an overall system (left), and simple and self-similar interconnect geometries (right). (b) Interconnect patterns in their initial, unloaded states. Simple interconnects show higher elastic stretchability than self-similar interconnects in both with (c) core-shell encapsulation and (d) shell-only encapsulation.

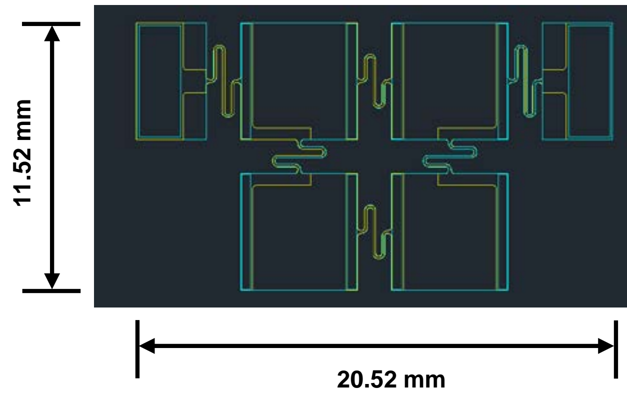


Supplementary Figure S7 | Elastic stretchability evaluated by 3D-FEA for various types of interconnects with core/shell encapsulation. The geometries include (a) half-period simple serpentine, (b) half-period self-similar, (c) 1.5-period simple serpentine, and (d) horseshoe curve, all with the same core-shell encapsulation. All cases show inferior interconnect stretchability compared to the simplest design (170%).

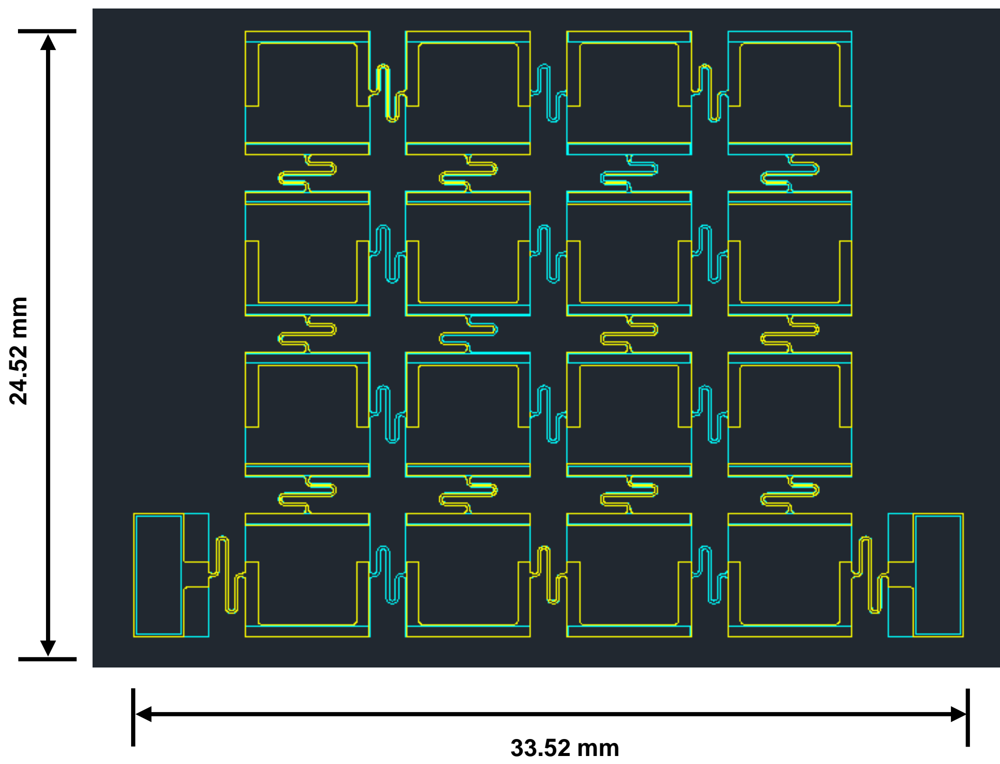


Supplementary Figure S8 | Computational mechanics studies of interconnects with various cladding geometries and encapsulation configurations. (a) Elastic stretchability as a function of PI cladding layer thickness showing a non-monotonic dependence of interconnect elastic stretchability $\varepsilon_{ict\text{-}elastic\text{-}stretch}$ on PI thickness, where the maximum $\varepsilon_{ict\text{-}elastic\text{-}stretch}$ obtains at a thickness of 4.8 μm. (b) Maximum principal strains in the metal as a function of unit cell elongation with (blue) and without (red) the core material.

2X2 array

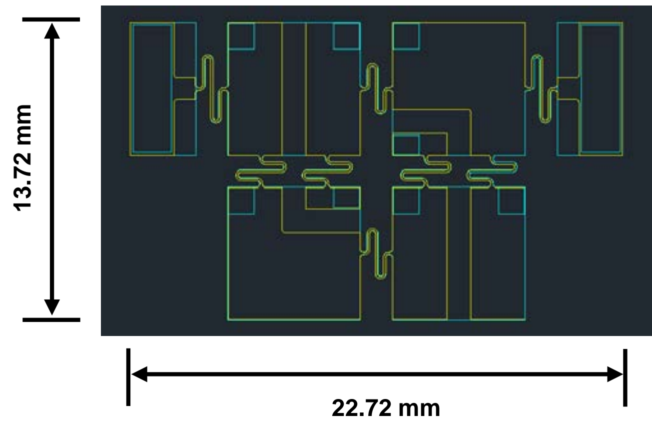


4X4 array

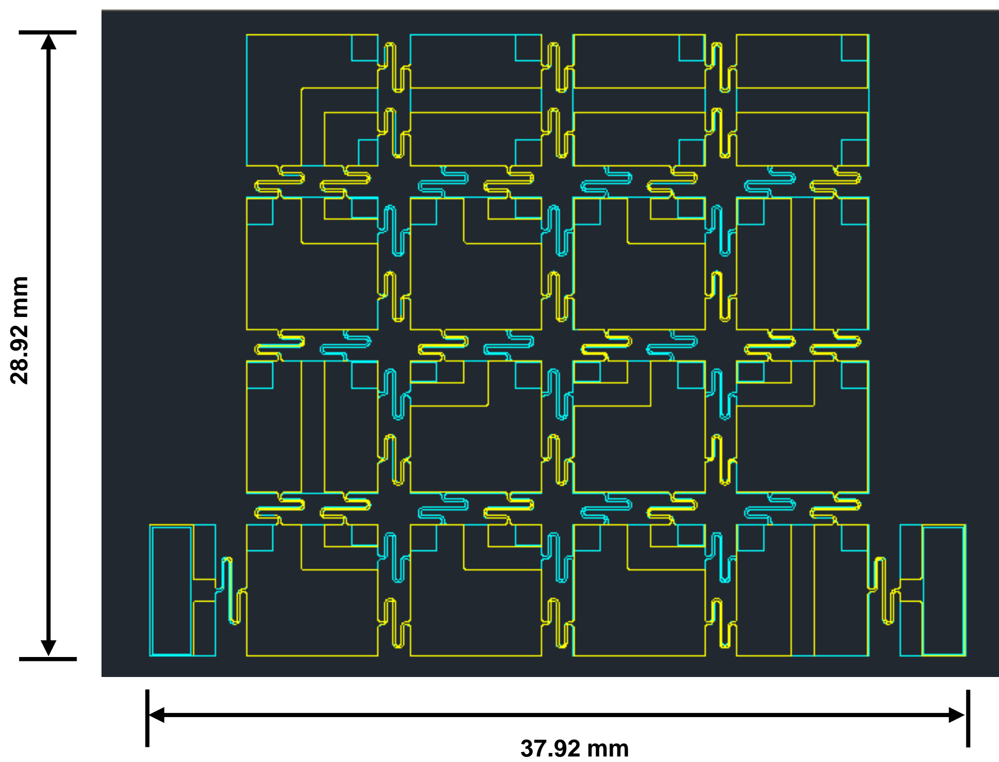


Supplementary Figure S9 | System layouts that consist of 2X2 and 4X4 arrays of 2J solar cells.

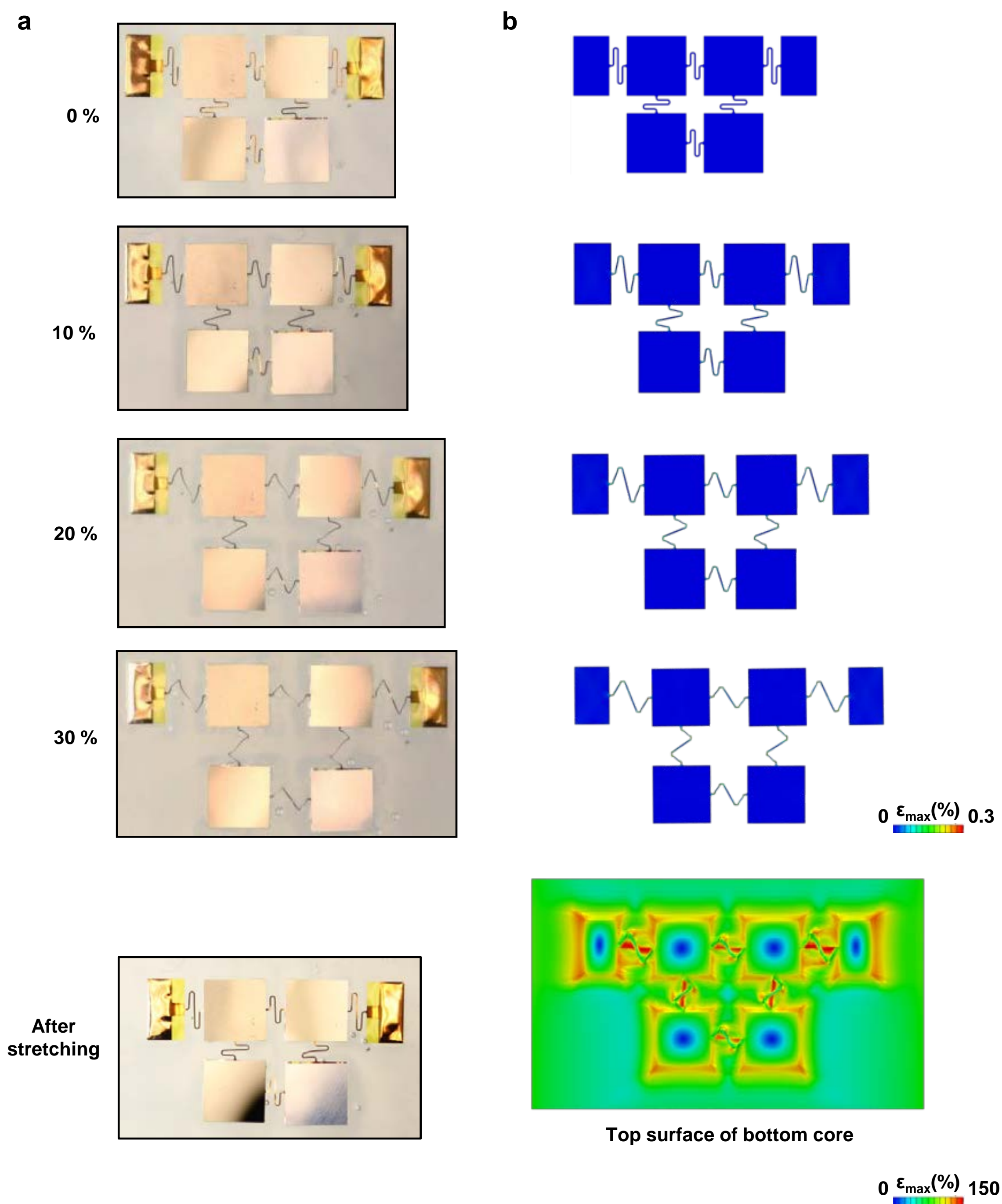
2X2 array



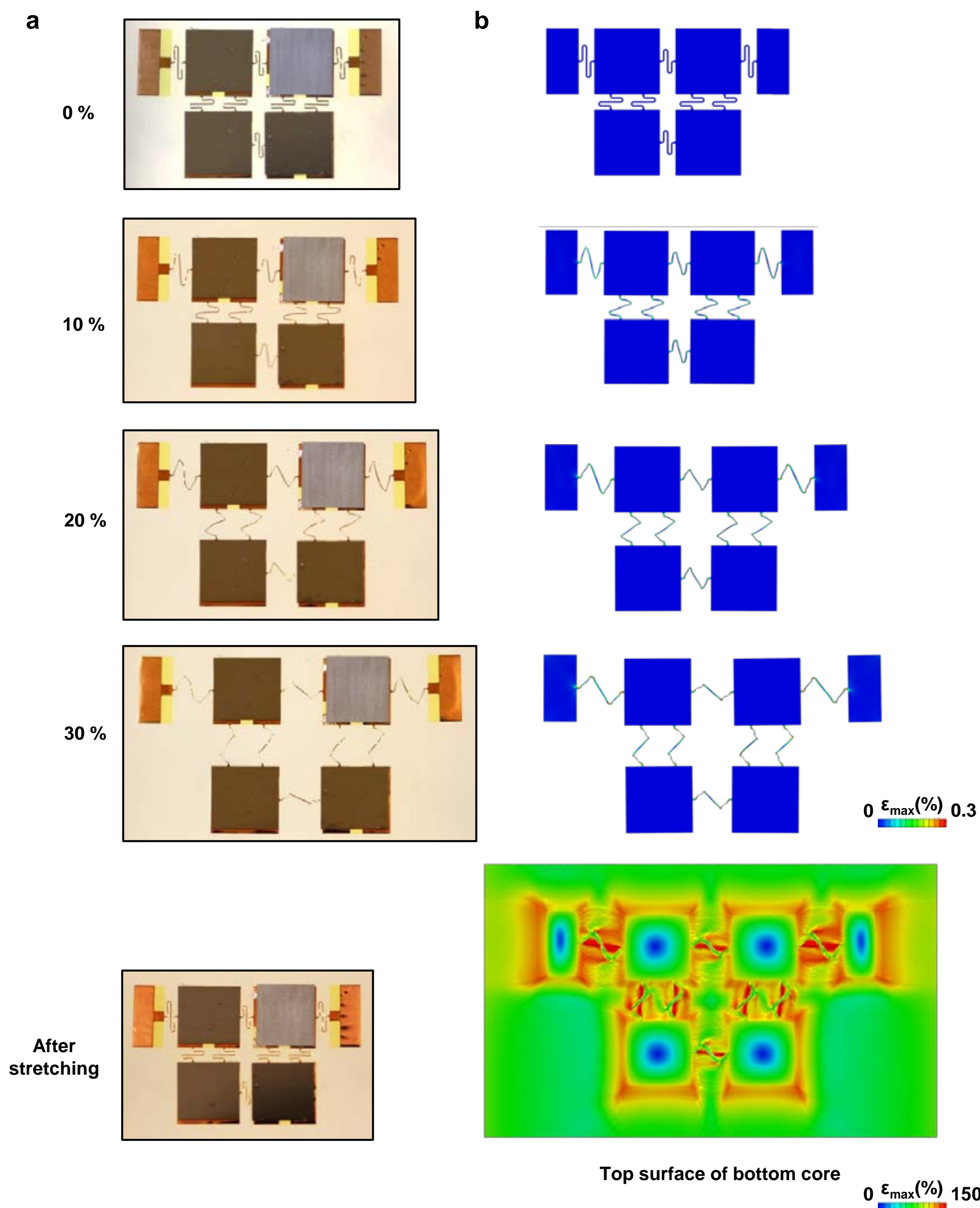
4X4 array



Supplementary Figure S10 | System layouts that consist of 2X2 and 4X4 chip-scale batteries.



Supplementary Figure S11 | Computational and experimental studies of a system with a 2X2 array of 2J solar cells on core material. (a) Optical images and (b) 3D-FEA modeling of the array at different levels of bi-axial stretching. The strains in the metal and in the core material are highlighted.

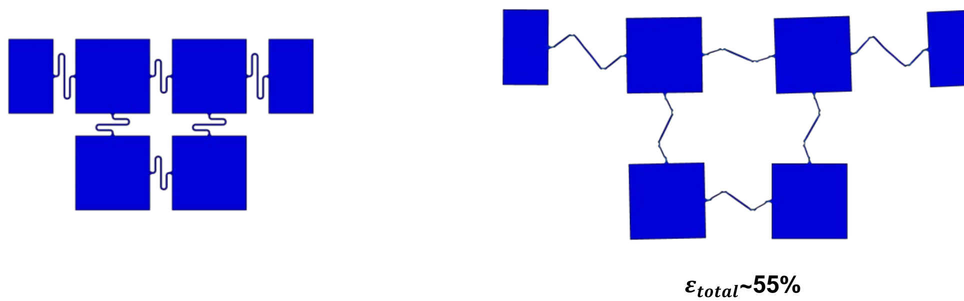


Supplementary Figure S12 | Computational and experimental studies of a system with a 2X2 array of chip-scale batteries on core material. (a) Optical images and (b) 3D-FEA modeling of the array at different bi-axial stretching levels. The strains in the metal and in the core material are highlighted.

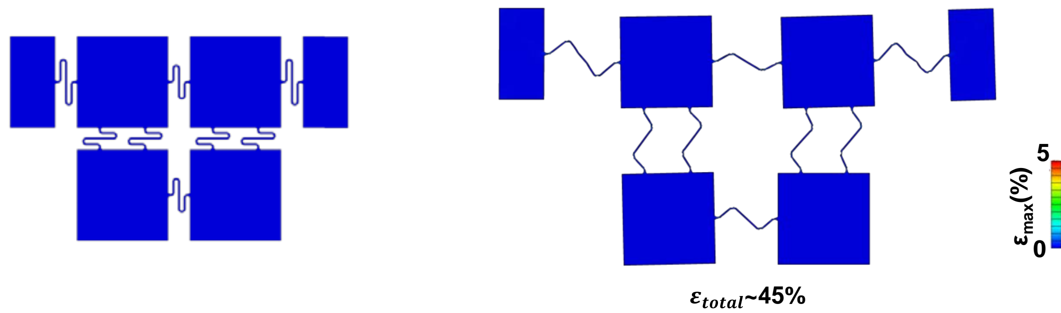
a

b

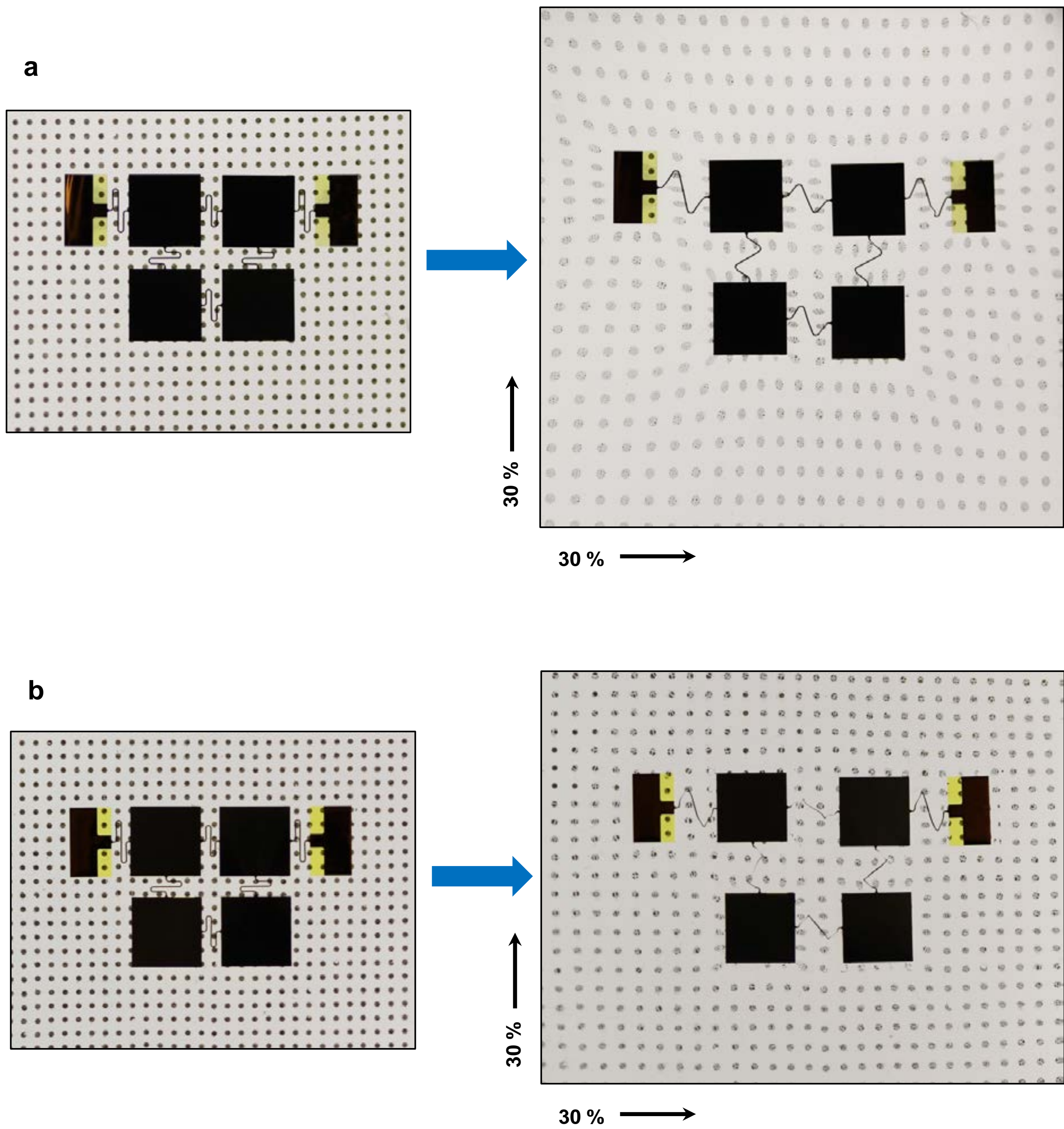
c



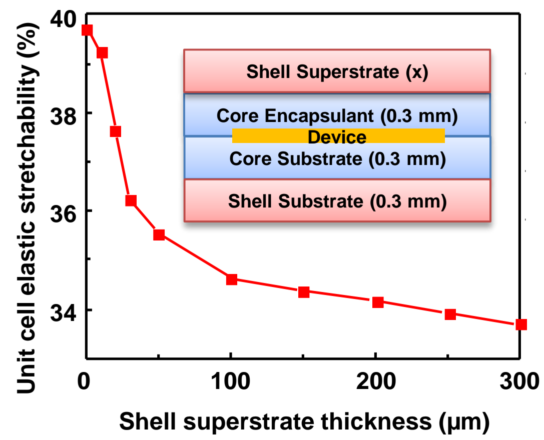
d



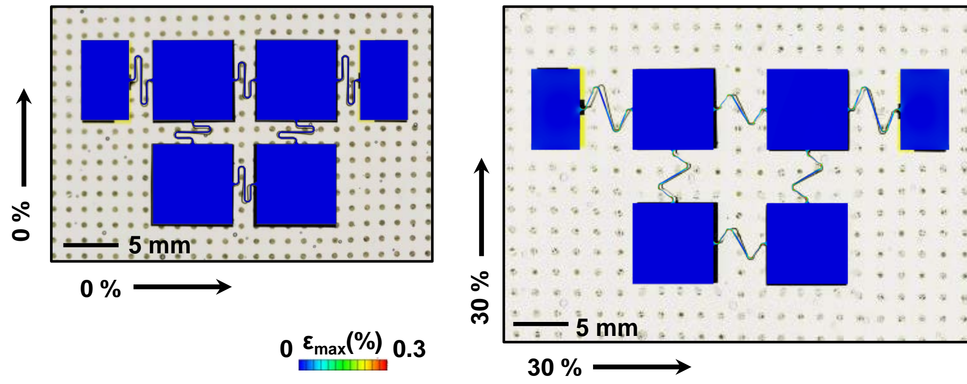
Supplementary Figure S13 | 3D-FEA results with a focus on total stretchabilities for bi-axial tensile loading of a unit cell embedded in a core/shell encapsulation. Simple serpentine unit cell structures (a) without and (b) with the use of pre-strain. Systems composed of 2X2 arrays of (c) 2J solar cells and (d) chip-scale batteries.



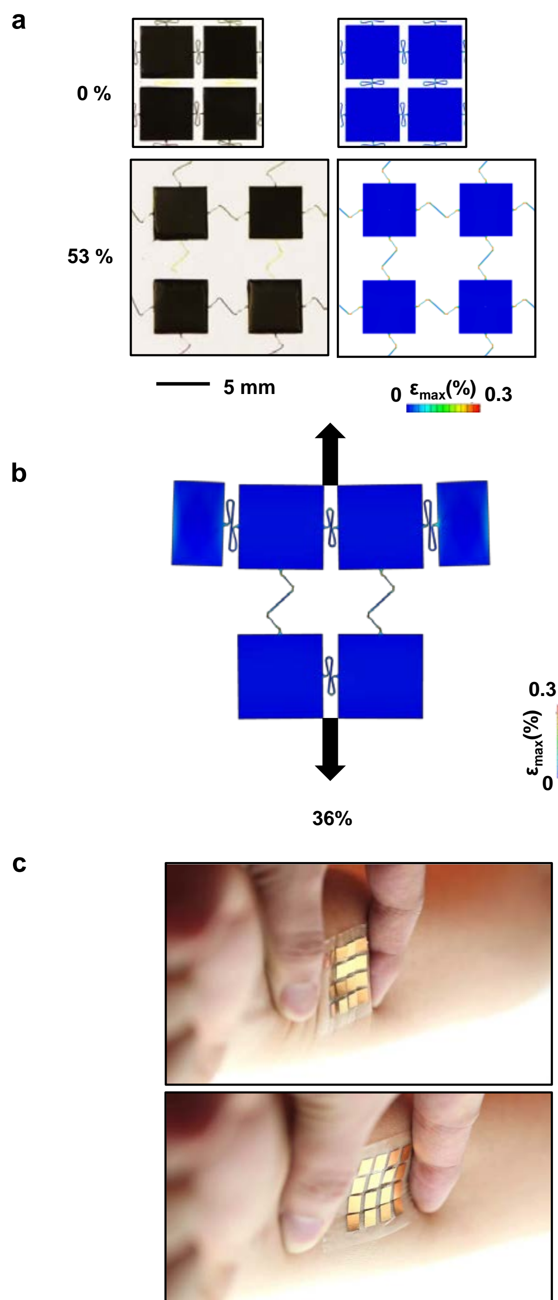
Supplementary Figure S14 | Optical images of strain mapping associated with bi-axial stretching (to 30%) applied to a system consisting of a 2X2 array of 2J solar cells (a) without and (b) with core material.



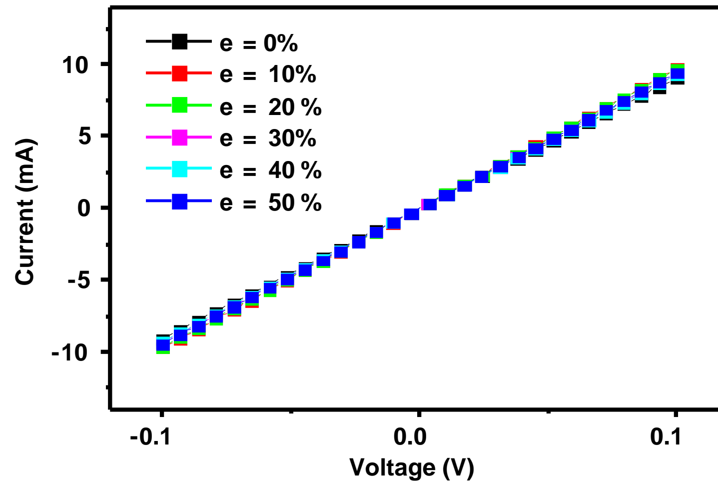
Supplementary Figure S15 | 3D-FEA results for stretchability as a function of the thickness of the top layer shell of the encapsulation thicknesses.



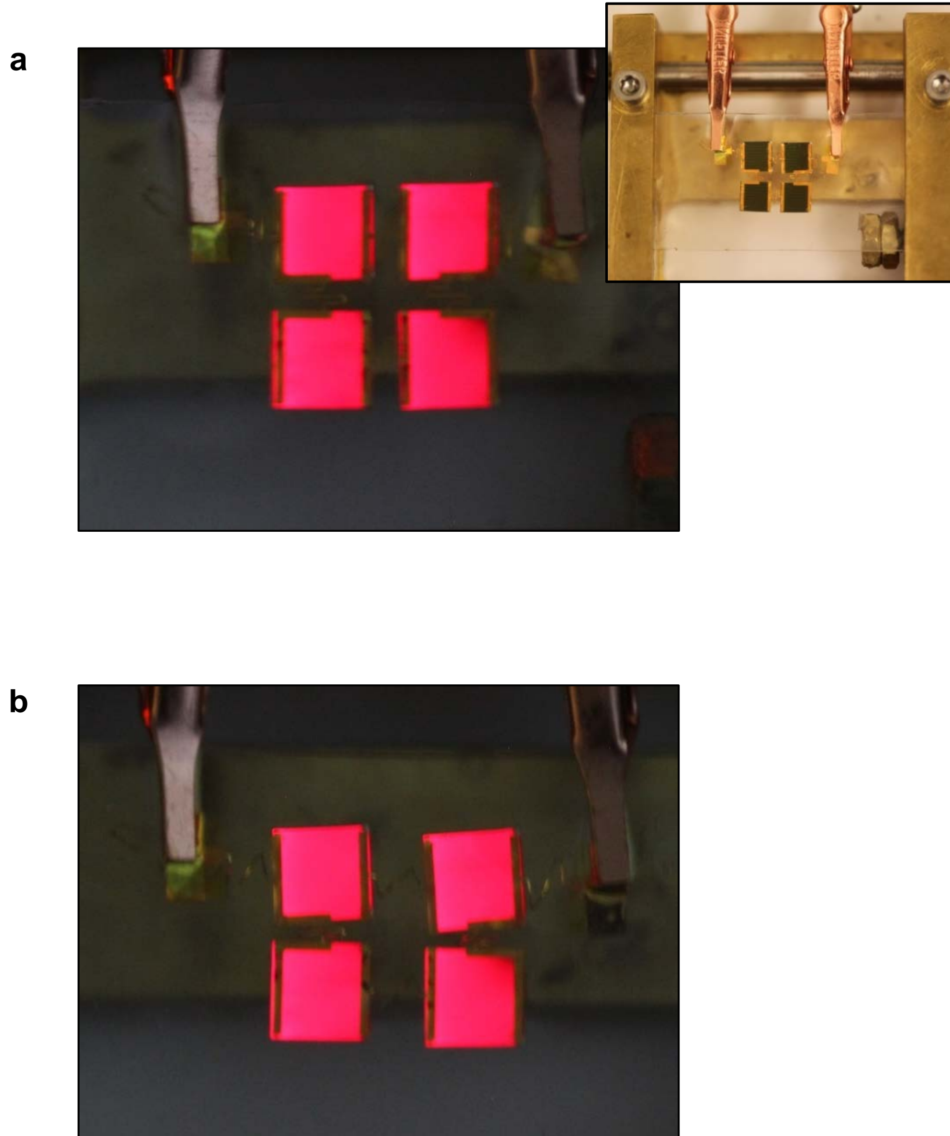
Supplementary Figure S16 | Computed and experimentally observed deformation of a system that consist of a 2X2 array of 2J solar cells with core-shell encapsulation under 30% biaxial load.



Supplementary Figure S17 | Mechanics of a system consisting of 2X2 and 4X4 of 2J solar cells. (a) Computational and experimental studies of a device formed using a pre-strain strategy, stretched bi-axially up to the limit of elastic stretchability (53%). (b) 3D-FEA result for stretching along the vertical direction. (c) Photos of a system that consists of a 4X4 array of 2J solar cells mounted near the wrist and deformed with compressing and stretching.

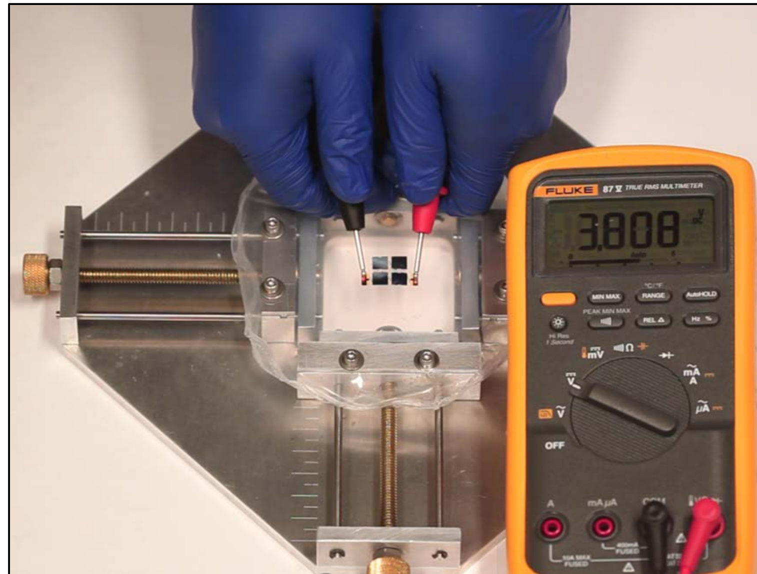


Supplementary Figure S18 | Current – Voltage curves measured from the serpentine interconnects under different levels of biaxial strain (0% - 50%). The resistance value is almost consistent with ~10.6 Ω.

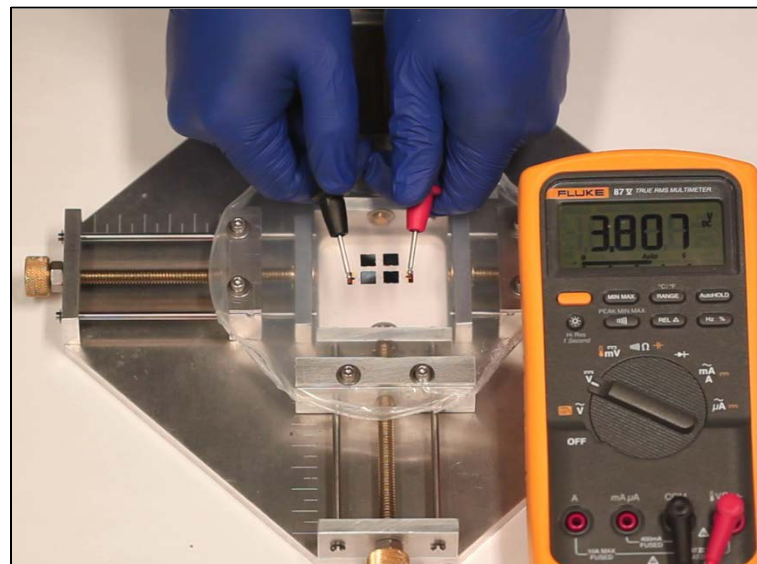


Supplementary Figure S19 | Electroluminescence from a system that consists of a 2X2 array of 2J solar cells, measured before and during deformation. Optical images of electroluminescence at (a) 0% (before application of bias; right panel) and (b) 20% uni-axial stretching.

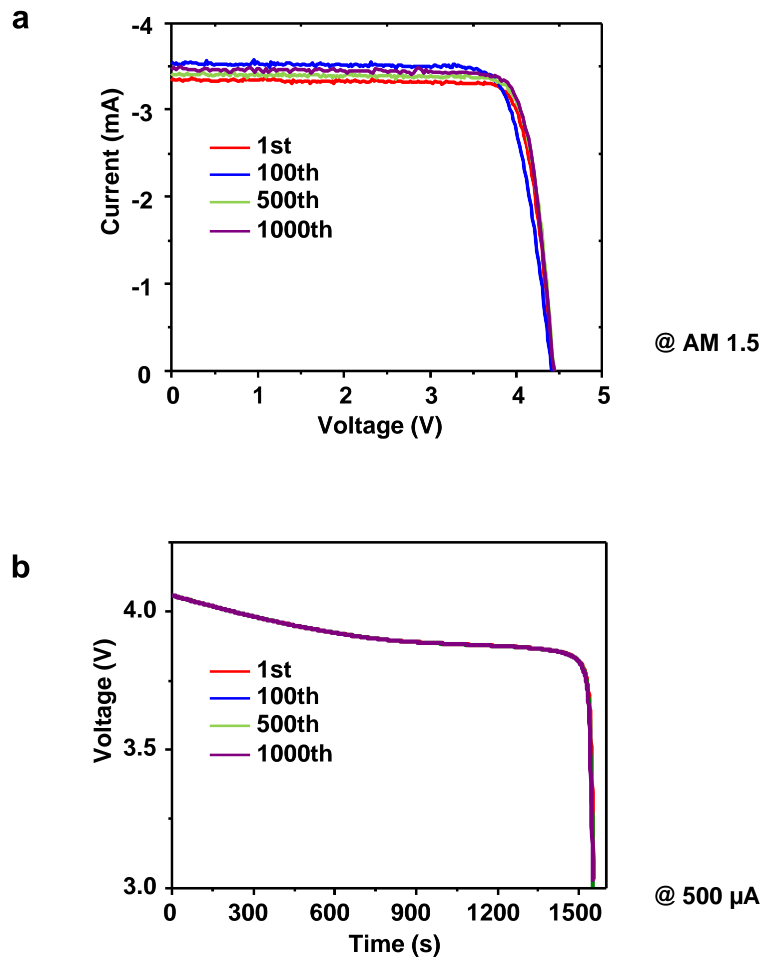
a



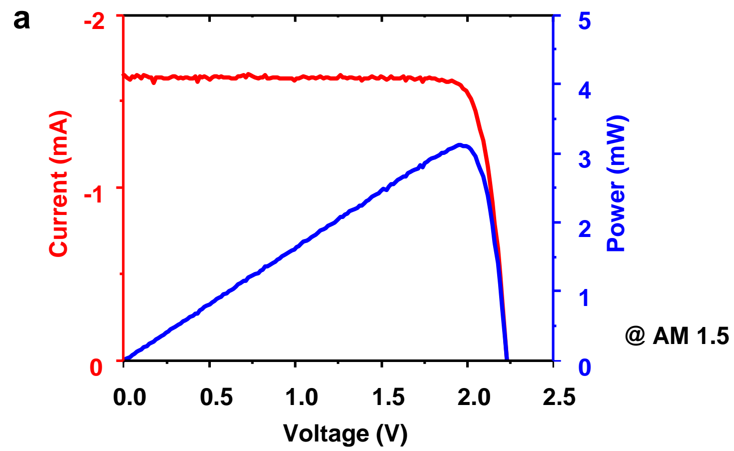
b

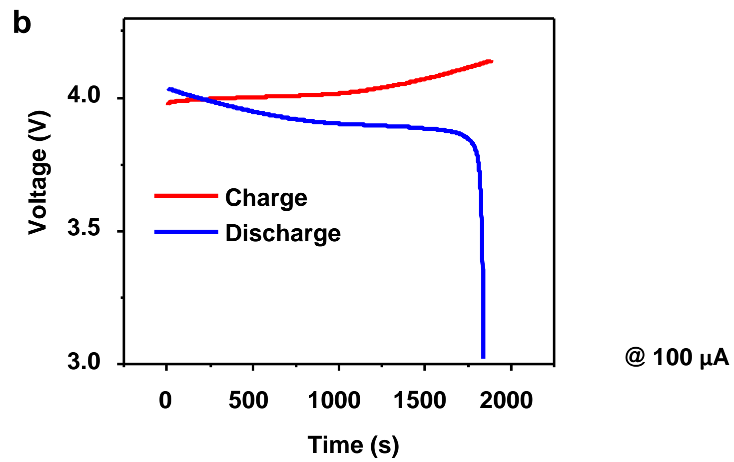


Supplementary Figure S20 | Output voltage from a system that consists of a 2X2 array of chip-scale batteries, measured before and during deformation. Optical images of output voltage at (a) 0% and (b) 30% of bi-axial stretching.

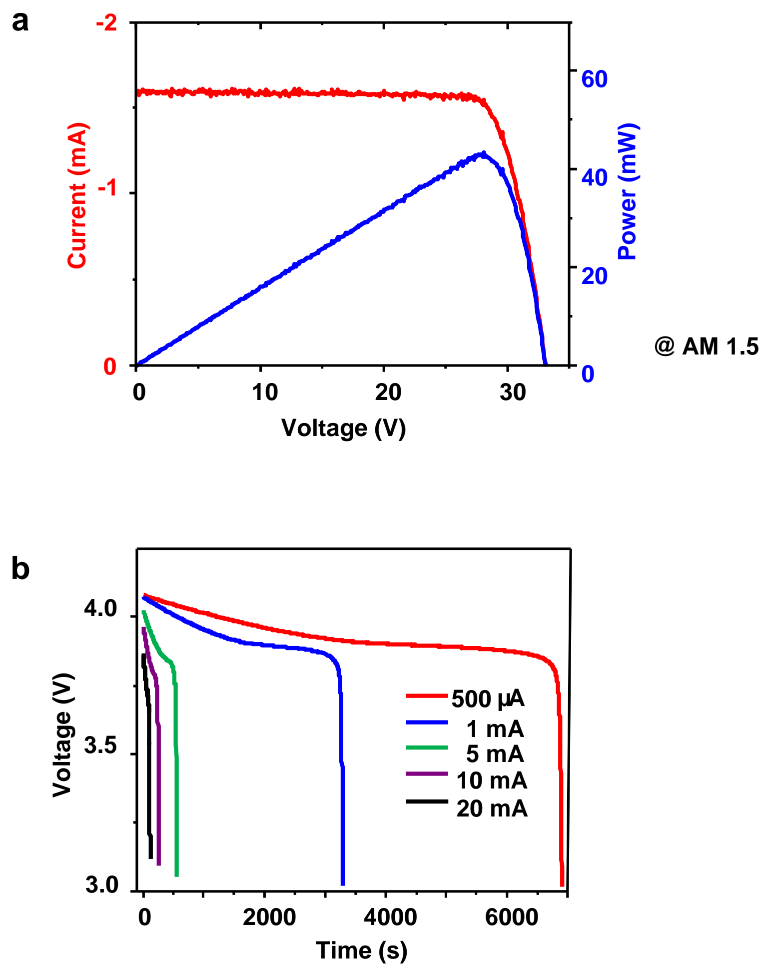


Supplementary Figure S21 | Performance for solar cell and battery systems under cyclic deformation. Performance of systems that consist of 2X2 arrays of (a) 2J solar cells under AM 1.5 illumination and (b) chip-scale batteries during 500 μA of discharge current. The data shown here were collected after application of 1st, 100th, 500th, and 1000th cycle of 15 % uni-axial tensile strain.



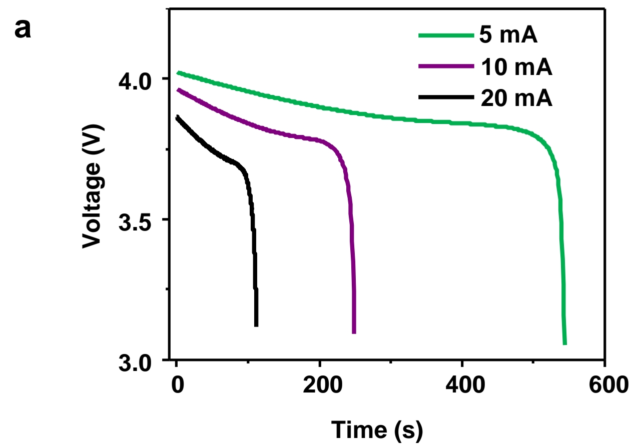


Supplementary Figure S22 | Isolated component performance for 2J solar cells and batteries. Performance for (a) 2J solar cell under AM 1.5 illumination and (b) chip-scale battery under 100 µA of discharge current.

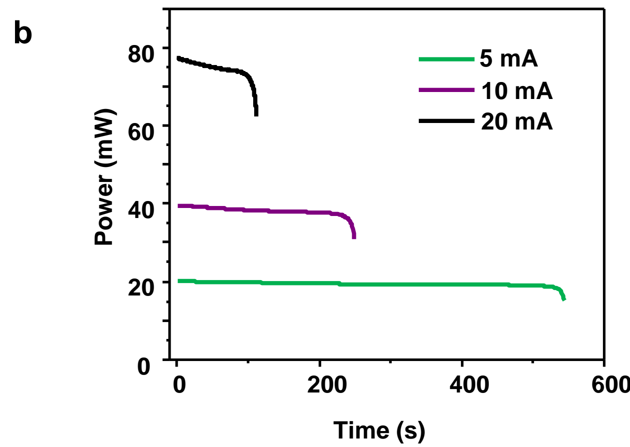


Supplementary Figure S23 | Array performance of interconnected 2J solar cells and chip-scale batteries. Performance of systems that consist of 4X4 arrays of (a) 2J solar cells under AM 1.5 illumination and (b) chip-scale batteries at 500 μA, 1 mA, 5 mA, 10 mA, and 20 mA of discharge current.

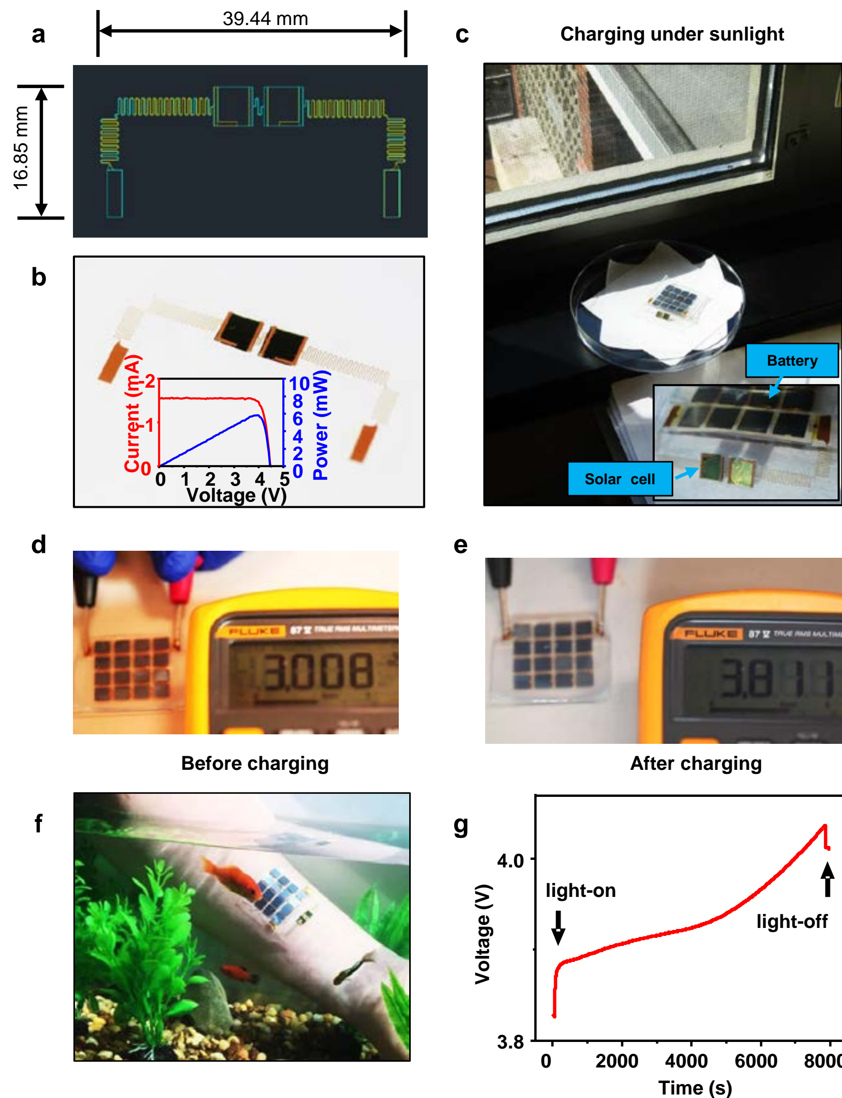
a



b

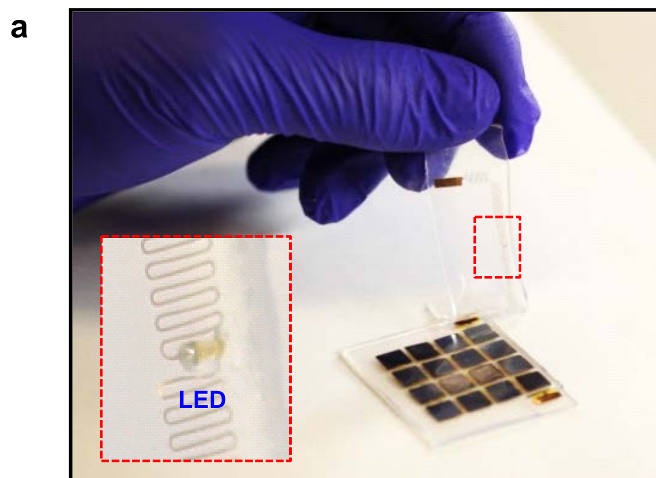


Supplementary Figure S24 | Enlarged graphs of battery module performance at high power operation. Performance of a system that consist of a 4X4 array of chip-scale battery at 5 mA, 10 mA, and 20 mA as (a) voltage (V) vs. time (s) and (b) power (mW) vs. time (s).

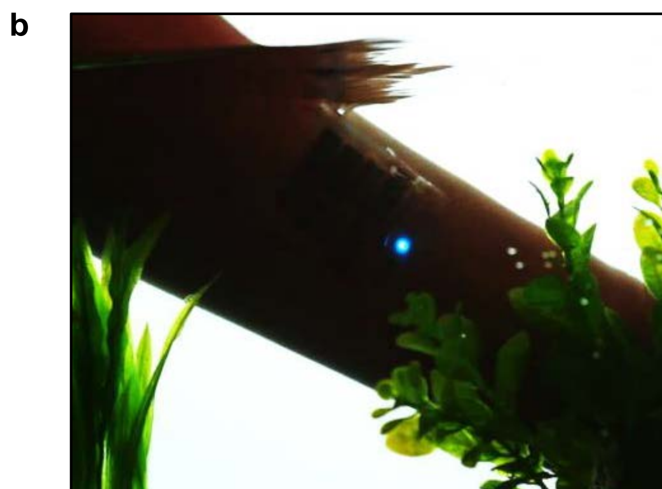


Supplementary Figure S25 | Re-charging of a battery module by use of a releasable solar cell module. (a) Layout of the releasable solar cell module and (b) an optical image of the actual device and its performance under AM 1.5 illumination. (c) A photo of a battery module and solar cell module laminated together for battery charging under sunlight. Changes in output voltage of a battery module (d) before and (e) after re-charging using the procedure shown in (c). (f) Image of battery re-charging in water. (g) A graph of output voltage as a function of time during battery re-charging under room light.

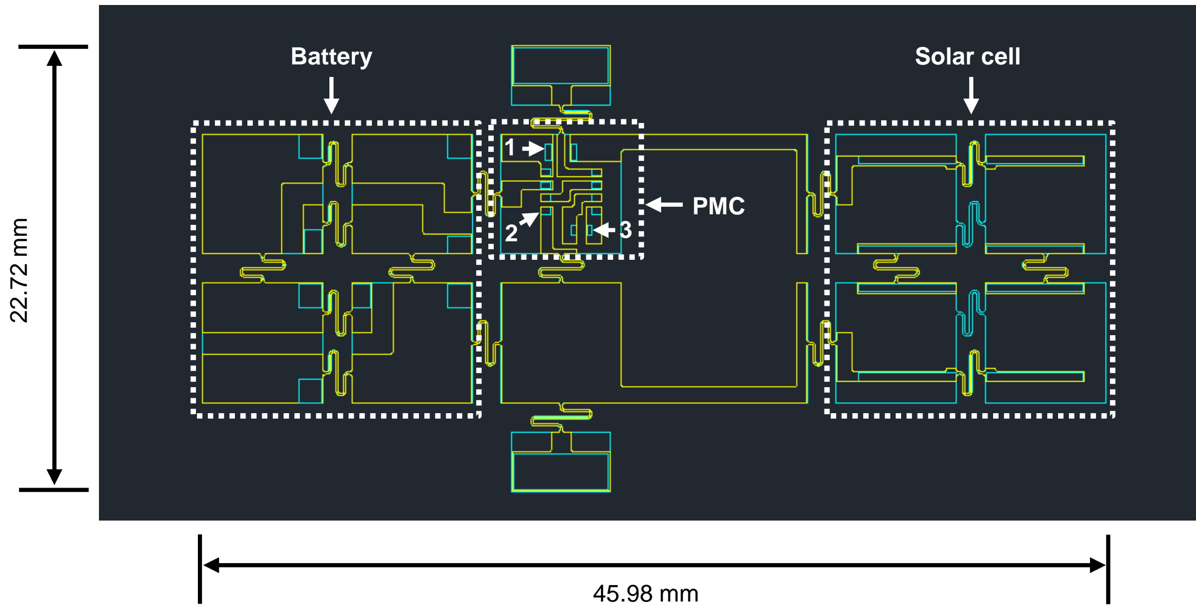
a



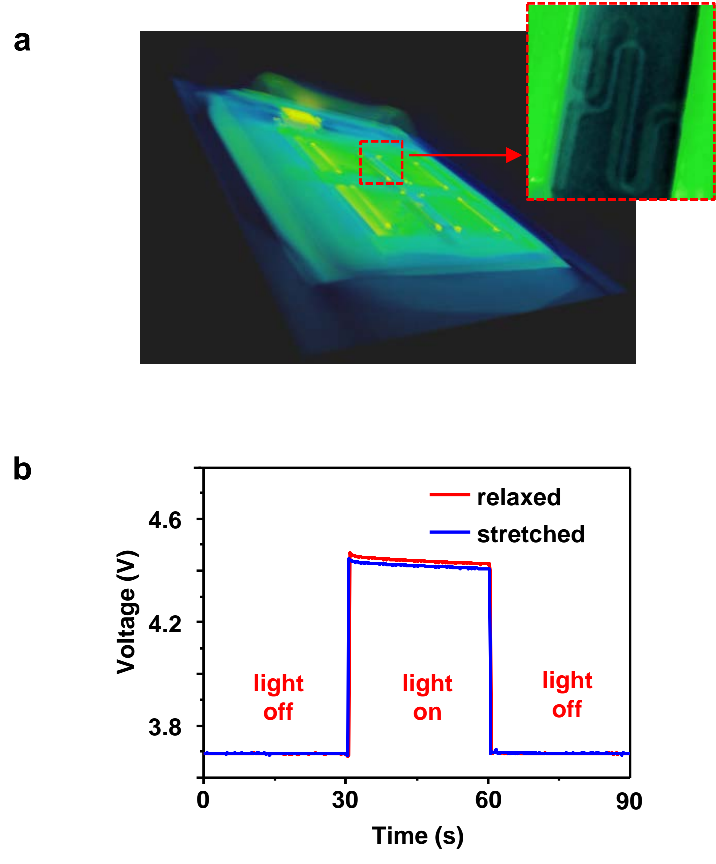
b



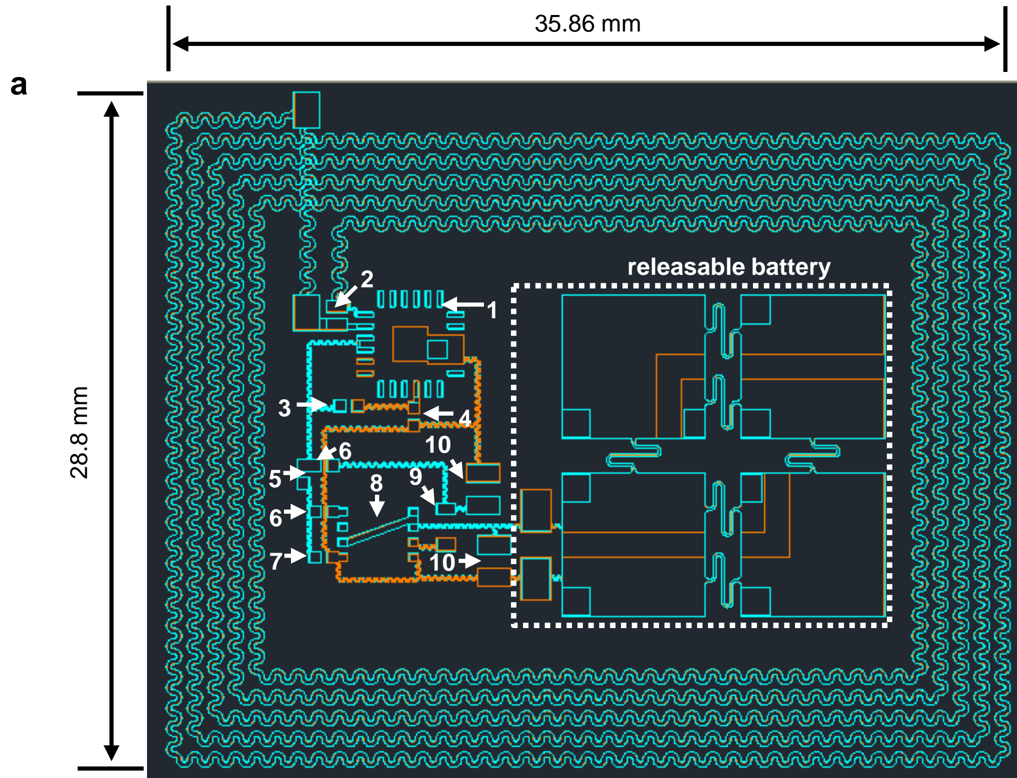
Supplementary Figure S26 | An integrated system consisting of an LED module laminated onto a battery module. (a) Image of integration of a stretchable LED module and a battery module. (b) Operation of the LED module using power supplied underwater and mounted on a human forearm.

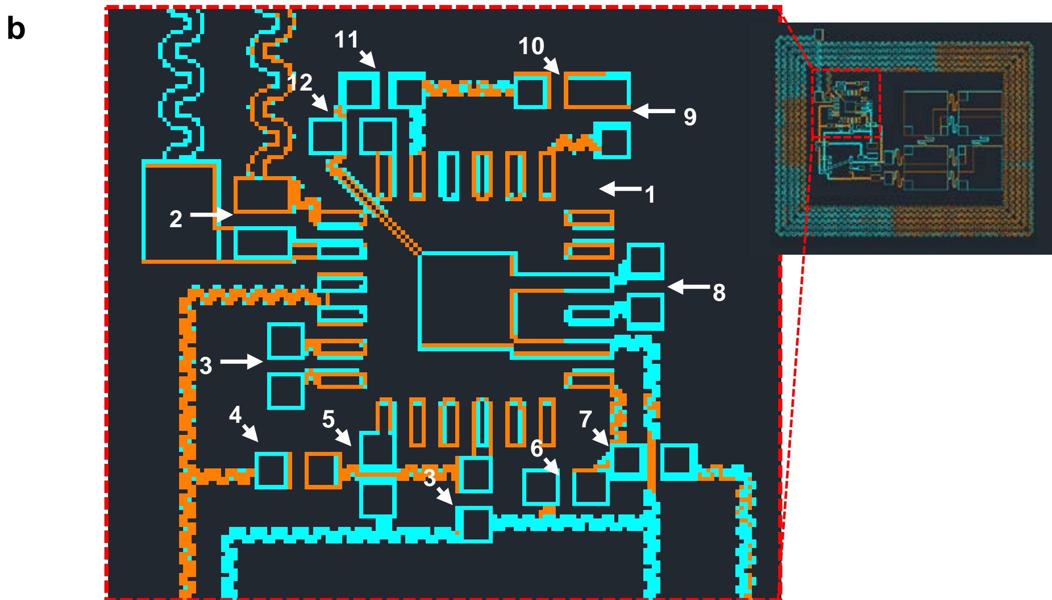


Supplementary Figure S27 | Layout of a foldable solar cell/power management circuit/battery integrated device.

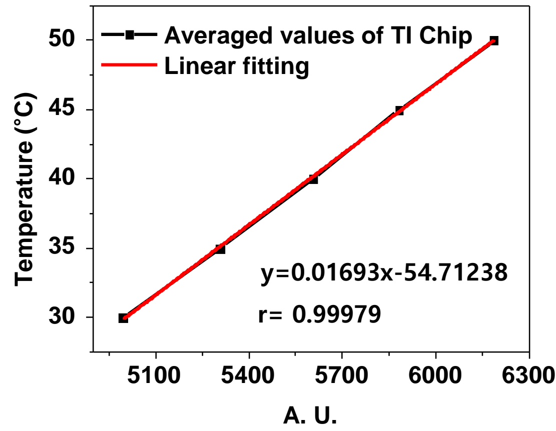


Supplementary Figure S28 | Geometry and performance of a foldable solar cell/power management circuit/battery integrated device. (a) X-ray computed tomography images of the folded system, with magnified view of overlapped interconnect. (b) Output voltage as a function of time under constant uni-axial strain (15%) for conditions with and without exposure to light.



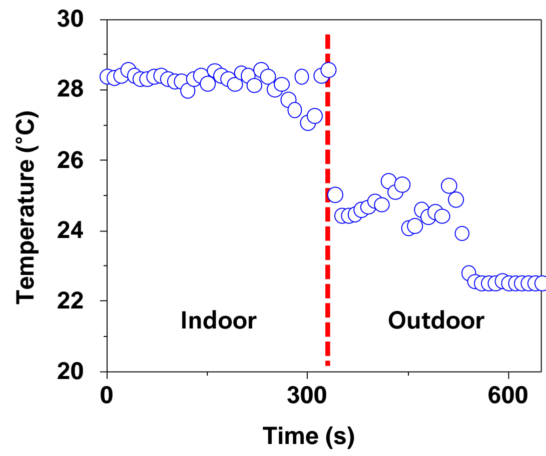


Supplementary Figure S29 | Layout of (a) battery-integrated NFC device and (b) the system with integrated LED alarm.

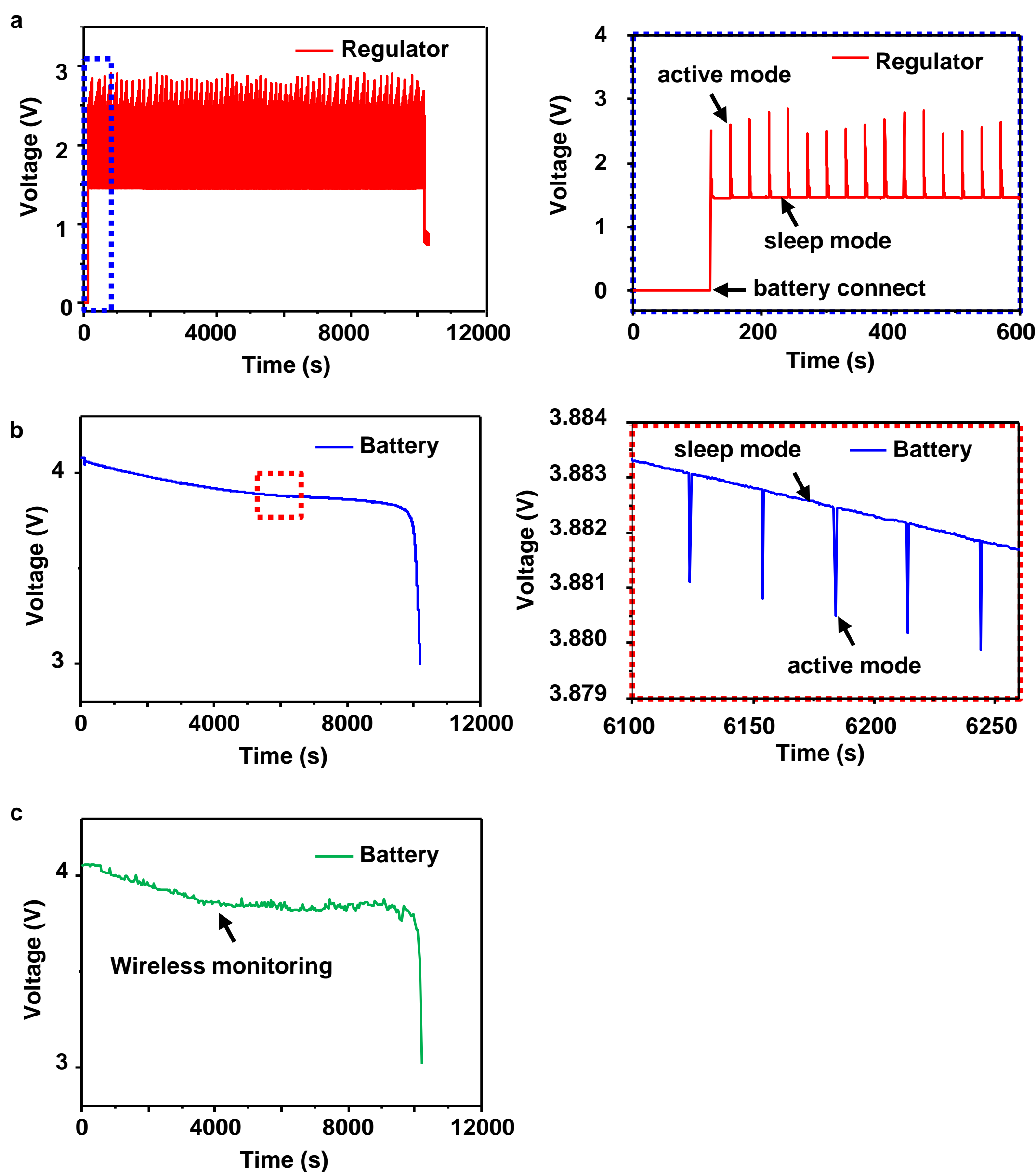


$$r = \frac{\sum_{i=1}^{n}(x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\sum_{i=1}^{n}(x_i - \bar{x})^2}\sqrt{\sum_{i=1}^{n}(y_i - \bar{y})^2}}$$

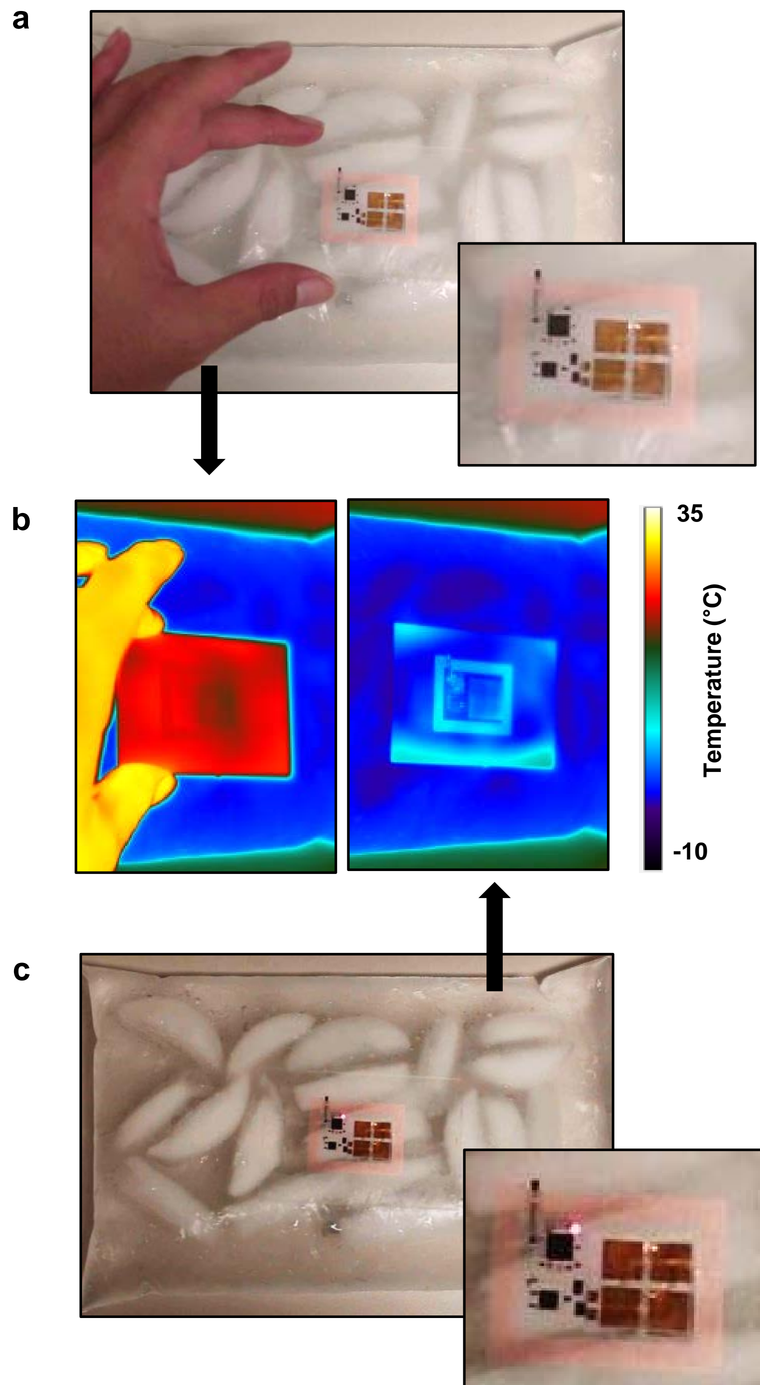
Supplementary Figure S30 | Sensor calibration. Each point represents the averaged value of the wireless output of an NCF system at different temperatures (30, 35, 40, 45, and 50 °C). The plot shows a linear relationship with r (Pearson's correlation coefficient) ~99.9%, where x_i and y_i correspond to the ith sample, and $\bar{x} = \frac{1}{n}\sum_{i=1}^{n} x_i$ and $\bar{y} = \frac{1}{n}\sum_{i=1}^{n} y_i$, respectively.



Supplementary Figure S31 | Atmospheric temperature logging using a battery-integrated NFC device.



Supplementary Figure S32 | Voltage measured from the regulator and a battery module. Voltage monitoring by chronopotentiometry of (a) regulator and (b) battery module that consists of a 4X4 array of chip-scale batteries. The enlarged graphs on the right highlight the active and sleep modes of NFC device operation. (c) Voltage level of a battery module monitored via the NFC device.



Supplementary Figure S33 | Temperature alarm system that includes an LED integrated with a battery-NFC device. Optical images of (a) battery-NFC device and (c) application of ice pack to trigger the temperature alarm, seen through activation of the LED. (b) IR images before and after applying the ice pack.

a

Device number	Specification
1	Jumper
2	0.1 μF
3	CBC910

b

Device number	Specification
1	RF430FRL152H
2	10 pF
3	24 kΩ
4	0.01 μF
5	440 kΩ
6	Jumper
7	560 kΩ
8	BD9120
9	4.7 mH
10	10 μF

c

Device number	Specification
1	RF430FRL152H
2	10 pF
3	10 μF
4	24 kΩ
5	Jumper
6	196 kΩ
7	825 kΩ
8	100 Ω
9	625 nm, InGaAlP, LED
10	500 Ω
11	0.1 μF
12	1 μF

Supplementary Table S1 | Information on components used in the device. The specification of the chips for (a) foldable power management device (Supplementary Fig. 27), (b) battery integrated NFC device (Supplementary Fig. 29a), and (c) battery-integrated system with integrated LED alarm (Supplementary Fig. 29b).