Ultra-thin, Transferred Layers of Thermally Grown Silicon Dioxide as Biofluid Barriers for Bio-Integrated Flexible Electronic Systems

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Supplementary Information

Supplementary Note 1

Supplementary Figure Legends

Supplementary Figure S1-S25

Supplementary Table S1 and S2

Supplementary Note 1: Materials and Methods

Fabrication Methods for Devices and Test Structures with Thermal SiO_2 Barrier Layers

Fabrication of samples with layers of thermal SiO_2 as encapsulation began with wet oxidation (in O_2/H_2O) at high temperatures (typically at ~1150 ^oC) on the surfaces of standard silicon wafers (100-1000 nm thermal SiO_2, 500 μm Si substrate, 100 mm diameter, University Wafer). A mechanical grinding process (with an initial coarse grind and a final fine grind to achieve mirror like finish with thickness variance under 5 μm) reduced the thickness to 200 μm (Sygarus Systems). Photolithography and wet etching patterned layers of Ti/Mg (5 nm/100 nm) deposited by electron-beam evaporation into targeted resistor shapes (*SI Appendix*, Fig. S13A). For the capacitors (*SI Appendix*, Fig. S13B), sequential deposition and photolithography patterning of two layers of Cr/Au (5 nm/ 100 nm) between a dielectric layer of polyimide (1.5 μm, PI-2545, HD MicroSystems) yielded simple, parallel-plate designs (1 mm×1 mm capacitor plate). For the diodes and NMOS devices (*SI Appendix*, Fig. S13C and D), transfer printing delivered devices prefabricated on an SOI substrates using previously reported recipes onto the SiO_2/Si substrate, forming the Si nanomembrane diode and transistor (channel length L = 600 μm, width W = 20 μm, thickness t = 100 nm). A layer of Cr/Au (5 nm/100 nm) served as metal interconnects to reach probe pads outside the PDMS well (*SI Appendix*, Fig. S14A-C). For each type of device,

spin-coating, soft-baking and curing formed an overcoat of polyimide (PI-2545, HD MicroSystems) with a thickness of 3.5 μm. ALD produced a layer of Al_2O_3 on the polyimide, to facilitate bonding to a thick layer of polyimide (25.4 μm, Kapton, DuPont) coated with a bilayer of Ti/SiO_2 (5 nm/100 nm) deposited by electron-beam evaporation and laminated on a glass slide with a layer of PDMS. The bonding involved application of a commercial adhesive (Kwik-Sil, World Precision Instruments) applied at a pressure of ~50 kPa and cured at room temperature. Reactive ion etching (RIE) with SF_6/O_2 (Plasma Therm) followed by Inductively Coupled Plasma RIE (ICP-RIE, Surface Technology System) with SF_6 removed the Si substrate to leave a largely unaltered, pristine surface of the SiO_2 as a biofluid barrier and bio-interface.

Mg Test Structures for Evaluation of Water Barrier Performance of Conventional Materials

Photolithography with a positive photoresist (AZ nLOF 2070, MicroChemicals) formed 1 cm^2 square area on a clean glass substrate. Subsequent electron-beam evaporation and lift-off yielded a layer of Ti/Mg (5 nm/300 nm) in the pre-defined area. Various deposition techniques yielded different types of encapsulation layers for soak testing in PBS (*SI Appendix,* Table S1 and Table S2). Spin coating then prepared a photo-definable epoxy (SU-8 2000, MicroChem), polyimide (PI-2545, HD MicroSystems) and PDMS. PECVD formed SiO_2 and SiN_x both with deposition frequencies of 13.56 MHz. Al_2O_3 and HfO_2 were grown by ALD at 150 ^oC.

SI Appendix, Table S1 and S2 summarizes all of the Mg test results. Popular organic passivation materials, for instance, SU-8 and PDMS, failed within 1 day at body temperature, indicating poor water barrier quality. Inorganic/organic multilayers can be more effective than simple bilayers with the same overall thickness due to the tortuous paths for water permeation through defects and interfaces in multiple layers. In certain cases, however, such as with

Parylene C, the multilayer yields poor results, possibly due to non-trivial thickness dependent effects for permeation through Parylene C.

Impedance Measurements and Modeling

Impedance measurements used a Gamry Reference 600 potentiostat system (Gamery Instrument). The SiO_2 coated Au electrodes individually connected as the working electrode, with the Ag/AgCl as the reference electrode and a Pt wire as the counter electrode. The experiments used an AC potential of 10 mV with a frequency range of 1 Hz to 1 MHz, and a DC bias of 1 V. PBS solution served as the electrolyte at room temperature. Analysis used an equivalent circuit model shown in *SI Appendix,* Fig. S3, where R_s is the solution resistance, C_c represents the capacitance of pristine material, and R_{po} is the cumulative resistance of all pores, pinholes, microcracks and other defects. Additional liquid/metal interfaces form as the solution penetrates the coating. R_{CT} corresponds to the charge transfer resistance and C_{dl} is the double-layer capacitance associated with these interfaces. In all three types of SiO_2 materials:

$$C_c = \frac{\varepsilon_r \varepsilon_0 A}{t} \approx 0.86\, nF$$

where the coating area $A = 0.25\, cm^2$, thickness $t = 1\, \mu m$, relative permittivity $\varepsilon_r = 3.9$ and vacuum permittivity $\varepsilon_r = 8.854 \times 10^{-12}\, F \cdot m^{-1}$. Non-linear least squares fitting yielded values for the various parameters.

Results for SiO_2 formed by electron beam evaporation and PECVD interpreted using similar methods suggest pore resistances and charge transfer resistances that originate from defect sites (*SI Appendix,* Fig. S3). Moreover, in these material systems, C_{dl} cannot be ignored. As expected from the EIS model, the phase response is characterized by two valleys both for these cases. The

lower valley (~10^2 Hz for evaporated and ~10^3 Hz for PECVD materials) can be attributed to R_{po} and R_{CT} in parallel with C_{dl}. The valley at 10^6 Hz arises from the oxide capacitance and the solution resistance. Discrepancies between theory and experiment likely reflect limitations of the assumption that the pore/pinhole regions and the rest of the otherwise undamaged regions can be treated as parallel branches for charge transfer. In practice, the flow may be two-dimensional. In addition, the complexity of the electrode surface may require a modified representation for C_{dl} (ref. 1). Nonetheless, the simple compact model captures the general trends of the experimental findings, and it is sufficiently sophisticated to identify qualitative differences between thermally grown and deposited forms of SiO_2, and their critical role in barrier performance.

Electrical Leakage Tests

Measurements of electrical leakage for different thicknesses of thermal SiO_2 and other conventional oxides as an additional comparison involved application of a voltage, comparable to that relevant for operation of standard electronics, between a surrounding bath of PBS and an underlying doped silicon wafer, as in *SI Appendix,* Fig. S4A and Fig. S5. These studies involved PECVD or ALD to form thin layers of SiO_2 or Al_2O_3 on n-type Si wafers (1-10 Ω.cm), and SiO_2 grown thermally. In these tests, the wafer connects to the cathode to prevent the possibility of anodizing the silicon; the anode is a wire of platinum in the PBS solution. A well structure made of poly(dimethylsiloxane) (PDMS) confines the PBS to the central regions of the layers (~1 cm^2), thereby eliminating any effects of the edges of the samples. Ultraviolet ozone (UVO) treatment of the surfaces of these materials and the bottom surfaces of PDMS well (~1 cm in depth) structures enabled strong bonding upon physical contact, thereby yielding a waterproof seal around an exposed area of 1 cm^2. The well formed in this way confined the PBS solution during

the course of the testing. A Platinum (Pt) electrode dipped into the PBS served as an anode and the n-type Si substrate served as the cathode for measurements with the potentiostat system with two-terminal configuration under a constant 3 V DC bias.

As shown in *SI Appendix,* Fig. S4, at a pH of 7.4 and a temperature of 37 ^{o}C, leakage currents quickly (within 60 hours) reach levels that significantly exceed 10^{-6} A/cm^2 for 100 nm thick layers of PECVD SiO_2, and ALD Al_2O_3. Most polymers, including photocurable epoxies (SU-8) and elastomers such as PDMS exhibit leakage almost instantaneously after immersion in PBS solution (*SI Appendix,* Fig. S5). At the same thickness, thermal SiO_2 exhibits zero leakage, to within measurement uncertainties, throughout the 350-hour duration of the experiment. Leakage current here is a function of applied voltage for different organic layers at room temperature.

Measurement and Modeling of Rates of Dissolution of Thermal SiO_2

These measurements used pieces of Si wafers (1 cm× 2 cm dies) with thermal SiO_2 layers (100 nm thickness) grown across the top and bottom surfaces and the edges. Soaking occurred in plastic bottles containing PBS solution (25-30 ml) at room temperature, 37 ^{o}C, 50 ^{o}C, 70 ^{o}C and 90 ^{o}C separately. Ellipsometry defined the thickness of the SiO_2 as a function of soaking time.

Measurement results were also utilized to validate multiphysics models of the dissolution process coupling of all relevant continuum-scale physics: chemical species transport (using the Nernst-Planck equations), chemical reaction kinetics, electrostatics, and moving boundaries. Reaction kinetics were modeled using the Arrhenius form, with rate constant and activation energy for the primary SiO_2 dissolution reaction calculated from measurements and those of other reactions (forward and backward ionization of salts, PBS and water self-ionization) estimated to proceed much more quickly than SiO_2 dissolution. As seen in *SI Appendix,* Fig. S9A,

the dissolution rate is dominated by a half-order dependence on hydroxide concentration. The moving boundary velocity was calculated based on a mass balance at the boundary interface based on the local dissolution rate and assuming a baseline density of 2.19 g/cm^3. This model allows the time-dependent evolution of a SiO_2 layer with arbitrary initial thickness to be directly calculated and visualized for arbitrary pH and temperature, and the lifetime to be predicted (*SI Appendix,* Fig. S9B). Simulations were performed on both 2-D and 3-D geometries using COMSOL Multiphysics®.

Reactive Molecular Dynamics (RMD) Simulations

Reactive Molecular Dynamics (RMD) simulations provided molecular insights into the effects of temperature and defects/oxide density on the dissolution process. The RMD used the Reaxff potential, integrated in a Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS) package(2, 3). Previous work establishes the accuracy of this potential for interactions between SiO_2 and H_2O, through comparison to the macroscale experimental properties of these interfaces(4). The calculations involved initially pristine slabs of SiO_2 (density of 2.33 g/cm^3 and thickness of 2 nm, in lateral dimensions of 5 nm×5 nm) solvated in water (Fig. 3*A*). Removing a few SiO_2 molecules from the center of the slab yielded effective oxide densities of 2.27, 2.19, 2.06 and 1.95 g/cm^3, each of which was then solvated again in water (Fig. 3*B*). The pH of the solution was fixed at 7.4 by balancing the number of protons in the system. Periodic boundary conditions were applied in all the directions. Energy minimization of the system was performed for 1,000,000 steps. The time step was 0.1 fs(ref. 5). The Nosé-Hoover thermostat(6) held the temperature constant. Simulations included 10 runs at temperatures between 10 ˚C-100 ˚C at intervals of 10 ˚C, for each oxide density. To generate statistical data, five replicas were

performed for each set. The presented data correspond to the average of five simulation runs, each for a total of 35 ns with data collection a 0.1 ps intervals.

The root mean square displacement (RMSD) of each Si atom in each simulation step defined the dissociation events. In particular, the RMSD of bound Si atoms is 1.56 Å. Upon dissociation, this value sharply increased to >10 Å. The molecular species associated with the dissociated Si was defined by the atoms that exist within a distance of 3.2 Å from the center of the Si.

Similar simulations can yield results on the influence of mass density and the density of pinhole defects (Fig. 3*B* and *SI Appendix,* Fig. S11). As might be expected, the number of Si dissolution events is highest for the lowest density (1.95 g/cm^3) and the highest temperature (100 ˚C) (*SI Appendix,* Fig. S11A). Specifically, the dissolution process increases exponentially with temperature (for temperatures between 10 ^{o}C and 100 ^{o}C) and density (for densities between 1.95 and 2.33 g/cm^3, at 80 ^{o}C and 100 ^{o}C), respectively (*SI Appendix*, Fig. S11). The rate of dissociation from defective sites greatly exceeds that from pristine sites, thereby suggesting that most dissolution occurs at defective/low density regions (*SI Appendix,* Fig. S12A). This phenomenon is consistent with the defect-assisted dissolution mechanisms presented elsewhere(7, 8). Although the modeling involves many simplifying assumptions, both of these trends are qualitatively consistent with experimental results. The dissolution rates, for all densities, increase with temperature in an Arrhenius manner, consistent with the previous studies(9, 10, 11).

In addition to these qualitative insights, the results allow quantitative extraction of weighted activation energies of dissolution for different densities, based on the ratio of the population of dissolution events (P and P_0) at corresponding temperatures (T and T_0) according to the Boltzmann distribution law, $E = -Kln(\frac{P}{P0})/(\frac{1}{T} - \frac{1}{T0})$, where K is a constant. *SI Appendix,*

Fig. S12B summarizes the results normalized by the maximum *E*. The findings suggest that the energy needed to dissociate Si atoms from oxide layers with densities of 1.95 g/cm^3 is 70% of that for layers with densities 2.33 g/cm^3. The energy for dissociation increases with the density. This trend is consistent with previous experimental observations on deposited/grown oxides(11). Previously mentioned multiphysics models coupling reactive diffusion kinetics with electrostatics and moving boundaries can capture certain aspects based on continuum, non-atomistic effects(11). The results presented here complement the continuum modeling work by suggesting that low-density oxides present additional Si-OH dangling sites and therefore accelerated chemical reaction rates.

In order to see the intermediates and final products of Si in the solution, the simulation tracked the molecular identity of each Si which is dissolved in different temperatures. Simulations show that Si first forms $Si(OH)_2^{2+}$ and dissolves into solution. In the solution $Si(OH)_2^{2+}$ forms bonds with two more OH^- groups to yield $Si(OH)_4$(ref. 12). The timescale for the reaction $Si(OH)_2^{2+} \rightarrow Si(OH)_4$ is 60-70 ns at 37 ˚C(ref. 12). Results did not indicate any $Si(OH)_2^{2+}$ conversions for temperatures below 80 ˚C within the simulation time i.e. 35 ns while at 80 ˚C and 90 ˚C, the simulation observed the $Si(OH)_2^{2+} \rightarrow Si(OH)_3^+$ (*SI Appendix,* Figure S12). For 100 ˚C, we the reaction $Si(OH)_2^{2+} \rightarrow Si(OH)_3^+ \rightarrow Si(OH)_4$ occurs in 32 ns. The hypothesis is that high temperatures boost the conversion of intermediates and the formation of $Si(OH)_4$.

Cyclic Bending of Active Electronics with Thermal Oxide Encapsulation

As shown in *SI Appendix,* Fig. S25, cyclic bending test was applied to the flexible electronic system with dual-side thermal oxide encapsulation by bending the device to a radius of 5 mm for

10,000 cycles. Yield, gain and mean noise RMS remain nearly unchanged after 10,000 bending cycles.

Sodium Ion Transport Simulations

Modeling of sodium ion transport processes used the drift-diffusion equation and Poisson's equation. These equations were solved on a one-dimensional domain shown in *SI Appendix*, Fig. S19 using COMSOL Multiphysics®. A value of the diffusivity (D) of Na^+ in wet thermal SiO_2 from previous reports allowed calculation of the corresponding ion migration mobility (μ) using the Nernst-Einstein relation(13). Physically, $x = 0$ and $x = h$ correspond to the PBS/SiO_2 and SiO_2/Si interfaces, respectively, where h is the thickness of thermal SiO_2. The boundary condition for the drift-diffusion equation is $[Na^+] = 2 \times 10^{25} m^{-3}$ at $x = 0$. This value corresponds to the solid solubility limit of Na^+ in wet thermal SiO_2 because the concentration of Na^+ in PBS solution is a very large $[8.24 \times 10^{25} m^{-3} (137 mmol/L)]$. At $x = h$, the simulation used a reflective boundary condition based on the assumption that Na^+ diffusivity inside the underlying Si is so low that most Na^+ ions are reflected at the SiO_2/Si interface. The boundary conditions for the electrostatic potential are $V = V_{app}$ at $x = 0$ and $V = 0$ at $x = h$. The assumption is that the resistance of SiO_2 is much larger than the PBS solution. The voltage drops primarily across the oxide layer.

SI Appendix, Fig. S20 shows the Na^+ concentration and potential distribution within a thick ($h = 900\ nm$) SiO_2 layer at 37 °C after 2 years of operation. The potential bias V_{app} swept from 0 V to 2 V with an increment of 0.5 V. The Na^+ concentration decreases significantly near $x = 0$ and Na^+ accumulates at the other side, namely, at $x = 900\ nm$. A time-dependent rise in the potential barrier retards the Na^+ transport process. In this simulation, failure corresponds to the

point at which the shift in the threshold voltage ΔV_T for an $100\ nm$ equivalent oxide thickness (EOT) reaches 1 V. ΔV_T can be expressed as a function of spatially distributed Na^+ density(14):

$$\Delta V_T(t) = \frac{1}{C_0}[\frac{1}{h}\int_0^h x \cdot \rho_{Na^+}(x,t)dx]$$

where C_0 is the gate capacitance.

SI Appendix, Fig. S21A shows ΔV_T as a function of time with different bias voltages. The red dashed horizontal lines correspond to the failure criteria of threshold voltage shift. In *SI Appendix*, Fig. S21B, a normalization of the time to $\tau_{trans} = \frac{h}{\mu\xi} = \frac{h^2}{\mu V} = \frac{kTh^2}{DqV}$ corresponds to the drift-dominated ion transport with time-independent linear potential drop. In other words, this transport time does not account for charge accumulation self-consistently. If self-consistent were unimportant, the lines would be scaled to a universal curve which cross the horizontal threshold voltage line at $t/\tau_{trans} = 1$. However, the curves in *SI Appendix*, Fig. S21B all shift to the right, i.e. a longer failure time. This non-linear electric field dependency arises from changes in the potential associated with spatially distributed Na^+.

References

1. Miller JR, Outlaw RA, Holloway BC (2010) Graphene double-layer capacitor with ac line-filtering performance. Science 329(5999):1637–9.

2. Van Duin AC, Dasgupta S, Lorant F, A. GW (2001) ReaxFF: A Reactive Force Field for Hydrocarbonds. *Journal of Physical Chemistry A* 105(41):9396–9409.

3. Plimpton S (1995) Fast Parallel Algorithms for Short-Range Molecular Dynamics. *Journal of Computational Physics* 117(1):1–19.

4. Fogarty JC, Aktulga HM, Grama AY, Van Duin AC, Pandit SA (2010) A reactive molecular dynamics simulation of the silica-water interface. *The Journal of Chemical Physics* 132(17):174704.

5 Van Duin AC, et al. (2003) ReaxFFSiO reactive force field for silicon and silicon oxide systems. *The Journal of Physical Chemistry A* 107(19):3803–3811.

6. Evans DJ, Holian BL (1985) The Nose–Hoover thermostat. *The Journal of Chemical Physics* 83(8):4069.

7. Dove PM, Han N, De Yoreo JJ (2005) Mechanisms of classical crystal growth theory explain quartz and silicate dissolution behavior. Proceedings of the National Academy of Sciences 102(43):15357–15362.

8. Dove PM, Han N, Wallace AF, De Yoreo JJ (2008) Kinetics of amorphous silica dissolution and the paradox of the silica polymorphs. Proceedings of the National Academy of Sciences 105(29):9903–9908.

9. Worley WG (1994) Dissolution kinetics and mechanisms in quartz- and grainite-water systems. Doctoral Dissertation, Massachusetts Institute of Technology

10. Icenhower JP, Dove PM (2000) The dissolution kinetics of amorphous silica into sodium chloride solutions: effects of temperature and ionic strength. Geochimica et Cosmochimica Acta 64(24):4193–4203.

11. Kang S-K, et al. (2014) Dissolution Behaviors and Applications of Silicon Oxides and Nitrides in Transient Electronics. Advanced Functional Materials 24(28):4427–4434.

12. Yin L, et al. (2015) Mechanisms for Hydrolysis of Silicon Nanomembranes as Used in Bioresorbable Electronics. Advanced Materials 27(11):1857–1864.

13. Mecha J & Steinmann J (1979) Mobility of Sodium Ions in Silica Glass of Different OH Content. *Journal of the American Ceramic Society* 62(7-8):343–346.

14. Sze SM (2008) Semiconductor devices: physics and technology (2nd edition). John Wiley & Sons, p. 183.

Supplementary Figure Captions

Fig. S1. The SEM image in a 45° view of a ~100-nm-thick thermal SiO_2 above the polyimide layer, of the test vehicle shown in Fig. 1*B*.

Table S1. Summary of Mg soak tests for different candidate barrier materials.

Table S2. Summary of properties of all different encapsulation strategies examined.

Fig. S2. Mg soak test of a 50-μm-thick stainless steel foil in 70 °C PBS solution throughout 84 days.

Fig. S3. Theoretical modeling of EIS measurement of different SiO_2. (*A*) Equivalent circuit consists of both pristine and defective parts. (*B*) Parameters used for SiO_2 produced by evaporation, PECVD and thermally grown.

Fig. S4. (*A*) Schematic illustration of the two-terminal potentiostat system (*left*) used to measure leakage current through 100-nm-thick layers of PECVD SiO_2, ALD Al_2O_3 and thermal SiO_2 at 37 °C. Measurements involved a 3V DC bias continuously applied between a Pt electrode immersed in the PBS solution and a highly doped n-type silicon substrate using a two-electrode configuration. The results (*right*) highlight that thermal SiO_2 maintained leakage current below 100 nA throughout 360 hours while both PECVD SiO_2 and ALD Al_2O_3 failed within 50 hours. (*B*) Leakage currents associated with thermal SiO_2 encapsulation layers with different thickness at 96 °C.

Fig. S5. Leakage current as a function of applied voltage for different organic layers with a thickness of 1 μm, tested at room temperature.

Fig. S6. The SEM image in a 45° view of a 1000 nm thermal SiO_2 dissolved after accelerating PBS soak test at 96 °C, compared with unchanged thickness in the area of PDMS covered side.

Fig. S7. A sequence of SEM images in a 45° view illustrate dissolution of the 50-μm-thick stainless steel foil in accelerating PBS soak test at 96 °C throughout 60 days.

Fig. S8. The edge effect in thermal SiO_2 dissolution rate test.

Fig. S9. Multiphysics simulations of thermal SiO_2 dissolution. (*A*) Dissolution rate dependence on pH (Order 1: $k_0=3.85\times10^9$ $m^4mol^{-1}s^{-1}$, Order 0.5: $k_0=6.11\times10^7$ $m^{2.5}mol^{-0.5}s^{-1}$, Order 0.25: $k_0=7.68\times10^6$ $m^{1.75}mol^{-0.25}s^{-1}$). (*B*) Visualization of layer after 0 and 300 days separately (pH = 7.4, T = 50 ^{o}C).

Fig. S10. Number of reaction products during simulation of Si dissolution at 100 ^{o}C.

Fig. S11. Theoretical analysis of density and temperature effect on Si dissolution. (*A*) Number of Si dissolved in different temperatures and for different oxide densities. (*B*) Number of Si dissolved for different oxides at temperatures 80 ^{o}C and 100 ^{o}C.

Fig. S12. (*A*) The probability of SiO_2 dissolved from defective sites versus pristine regions. (*B*) Weighted activation energy associated with reaction of SiO_2 dissolution as a function of oxide density. (*C*) Number of Si compounds that exist in the solution at different temperatures.

Fig. S13. (*A-D*) Cross-sectional sketch of resistors, capacitors, diodes and NMOS transistors.

Fig. S14. Optical microscope images of capacitor (*A*), p-n diode (*B*) and MOSFET (*C*) encapsulated with 1,000-nm-thick thermal SiO_2 for accelerating soak test. Device part sealed in PDMS well, with gold metal wire extended to contact pad.

Fig. S15. Electrical characteristics of control devices including capacitor (*A*), p-n diode (*B*) and MOSFET (*C*) in PBS soak test at 96 ^{o}C.

Fig. S16. Cross-section illustrations of Mg device with double-sided thermal SiO_2 encapsulation layers (*A*), and control device (*B*).

Fig. S17. 70 ^{o}C PBS soak test of Mg device with double-sided thermal SiO_2 encapsulations (*A*), and control device (*B*).

Fig. S18. Bending the Mg device with double-sided thermal SiO_2 encapsulations to a radius of 5 mm exhibits high flexibility.

Fig. S19. Set up of sodium ion transport simulation with constant boundary condition at $x = 0$ and reflective boundary condition at $x = h$.

Fig. S20. Na^+ concentration and potential distribution within thermal SiO_2 (h = 900 nm) layer at the end of 2-years simulation at T = 37 ^{o}C.

Fig. S21. ΔV_T threshold voltage shift as a function of time (*A*) and normalized time (*B*) with different SiO_2 bias voltage at T = 37 ºC.

Fig. S22. Exploded-view schematic illustration of sensing system with top and bottom side thermal SiO_2.

Fig. S23. Images of active multiplexed electronics in four key fabrication steps: 1. isolated Si transistors above thermal SiO_2; 2. photolithographic patterning of 1st metallization for source, drain, gate (connected to sensing electrode pad) and row wires for multiplexing; 3. 2nd metallization of the column wires for signal output; 4. final device layout after removing Si substrate with exposed thermal SiO_2 as frontside encapsulation.

Fig. S24. Si transistor performances of the active multiplexed electronics. (*A*) Optical microscope image of a test transistor layout. (*B*) Transfer characteristics in both linear and semi-log scale, with supply voltage V_{DS}=0.1 V. (*C*) Output characteristics, V_{GS} ranging from -1 V to 4 V with a step of 1 V.

Fig. S25. (*A*-*C*) Yield, gain and mean noise RMS remain unchanged after 10^4 bending cycles. Inset in the left figure shows a photograph of a device bent to a radius of ~5 mm on a glass tube.

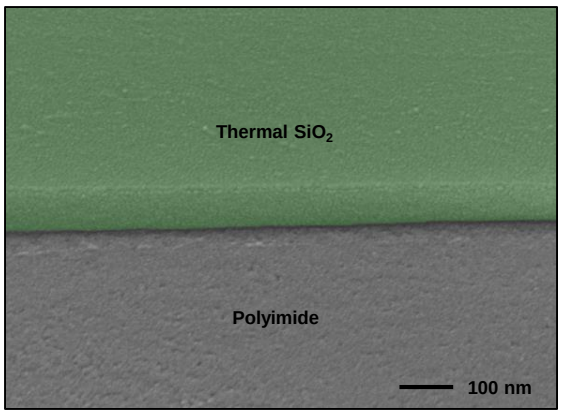


Figure S1

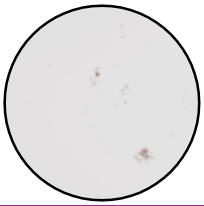
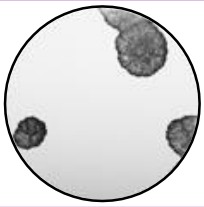
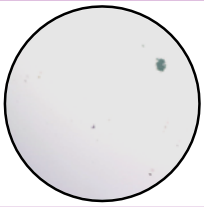
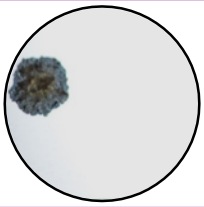
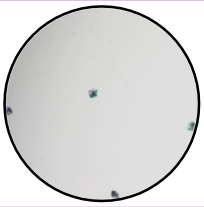
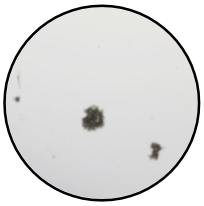
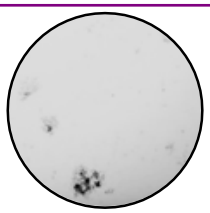
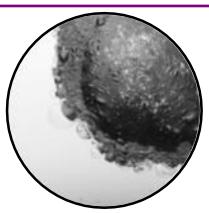
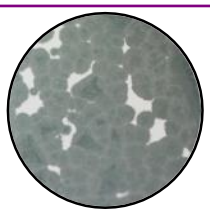
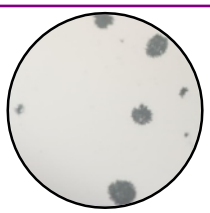
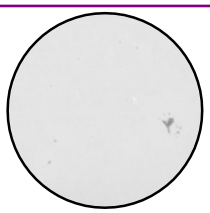
SU-8 1μm 37°C, 20min	PI2545 1μm 37°C, 20.5hr	Parylene C 1μm 37°C, 1.5hr	PDMS 1μm 37°C, 65min	LCP 25 μm 70ºC, 9d
				
PECVD low-dep SiO_2 1μm 37°C, 15min	PECVD SiN_x 1μm 37°C, 25min	ALD Al_2O_3 100nm 37°C, 10min	ALD HfO_2 100nm 37°C, 80min	SiO_2/SiN_x×3 16.6/16.6nmx3 37°C, 15min
				
Al_2O_3/HfO_2×3 16.6/16.6nmx3 37°C, 37min	Al_2O_3/Parylene C 50/1000nm 70°C, 7.5hr	Al_2O_3/Parylene C 50/6000nm 70°C, 12hr	Al_2O_3/Parylene C×3 50/283.3nm x3 37°C, 50min	Al_2O_3/PI2545 50/950nm 37°C, 30min
				
Al_2O_3/PI2545×3 50/283.3nm×3 37°C, 13.5hr	HfO_2/Parylene C 50/950nm 70°C, 250hr	HfO_2/Parylene C x3 50/283.3nm x3 70°C, 46min	HfO_2/PI2545 50/950nm 37°C, 5hr	HfO_2/PI2545×3 50/283.3nm×3 37°C, 10hr
				
SiN_x/Al_2O_3/Parylene C 50/50/900nm 37°C, 62.5hr	Ti/Pt 5/100nm 37°C, 5min	Cr/Au 5/100nm 37°C, 5min	Cr/Au 5/1000nm 37°C, 75min	
				5 mm

Table S1

Category	#	Material	Deposition method	Thickness for Mg test	Barrier lifetime (at 37 °C)	Leakage mode
Organic	1	SU-8	Spin coating	1 μm	< 1 day	Bulk
	2	Polyimide (PI)	Spin coating	1 μm	< 1 day	Bulk
	3	Parylene C	CVD	1 μm	< 1 day	Bulk
	4	PDMS	Spin coating	1 μm	< 1 day	Bulk
	5	LCP	--	25 μm	147 – 309 day*	Bulk
Inorganic	6	SiO_x	PECVD	1 μm	< 1 day	Bulk
	7	SiN_x	PECVD	1 μm	< 1 day	Bulk
	8	Al_2O_3	ALD	100 nm	< 1 day	Pinhole
	9	HfO_2	ALD	100 nm	< 1 day	Pinhole
Inorganic Multilayer	10	SiO_x/SiN_x x 3	PECVD	16.6/16.6 nm x3	< 1 day	Pinhole
	11	Al_2O_3/HfO_2 x 3	ALD	16.6/16.6 nm x3	< 1 day	Pinhole
Inorganic/organic Multilayer	12	Al_2O_3/Parylene C	ALD/CVD	50/950 nm	3 - 7 day*	Pinhole
	13	Al_2O_3/Parrlene C	ALD/CVD	50/6000nm	5 – 11 day	Pinhole
	14	Al_2O_3/Parylene C x3	ALD/CVD	50/283.3 nm x3	< 1 day	Pinhole
	15	Al_2O_3/PI	ALD/Spin coating	50/950 nm	< 1 day	Pinhole
	16	Al_2O_3/PI x3	ALD/Spin coating	50/283.3 nm x3	< 1 day	Pinhole
	17	HfO_2/Parylene C	ALD/CVD	50/950 nm	102 - 214 day*	Pinhole
	18	HfO_2/Parylene C x3	ALD/CVD	50/283.3 nm x3	22 - 39 day	Pinhole
	19	HfO_2/PI	ALD/Spin coating	50/950 nm	< 1 day	Pinhole
	20	HfO_2/PI x3	ALD/Spin coating	50/283.3 nm x3	< 1 day	Pinhole
	21	SiN_x/Al_2O_3/Parylene C	PECVD/ALD /CVD	50/50/900 nm	2 - 3 day	Pinhole
Thermal Oxide	22	SiO_2	Thermally grown	100 nm	6-7 years**	Slow dissolution

Permeability measured at 37°C, 90% Relative Humidity
*** Indicates data from accelerated soak test. Reaction Rate Factor Q10 = 2 - 2.5.**
**** Barrier lifetime defined as the soaking time period before any defect area on Mg pad reach 30mm^2.**

Table S2

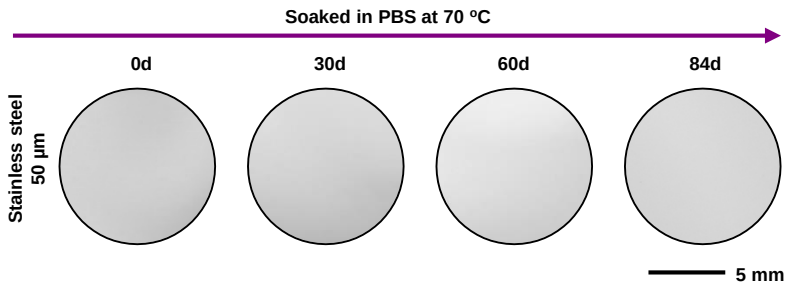
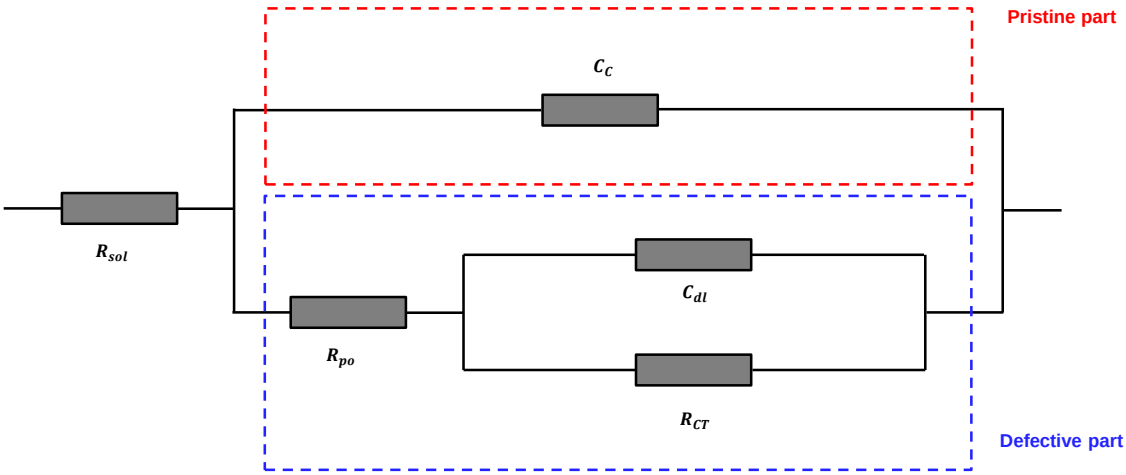


Figure S2

A



B

Circuit element	Physical Meaning	Expression of impedance	Evaporated SiO_x	PECVD SiO_2	Thermal SiO_2
R_{sol} / Ω	Solution resistance	R_{sol}	600	200	180
R_{po} / Ω	Pore resistance	R_{po}	600	2000	N/A
R_{CT} / Ω	Charge transfer resistance	R_{CT}	1800	48000	N/A
C_{dl} / μF	Double layer capacitance	$\frac{1}{j\omega C_{dl}}$	1.9	0.018	N/A
C_C / nF	Coating capacitance	$\frac{1}{j\omega C_C}$	0.3	0.86	1.17

Figure S3

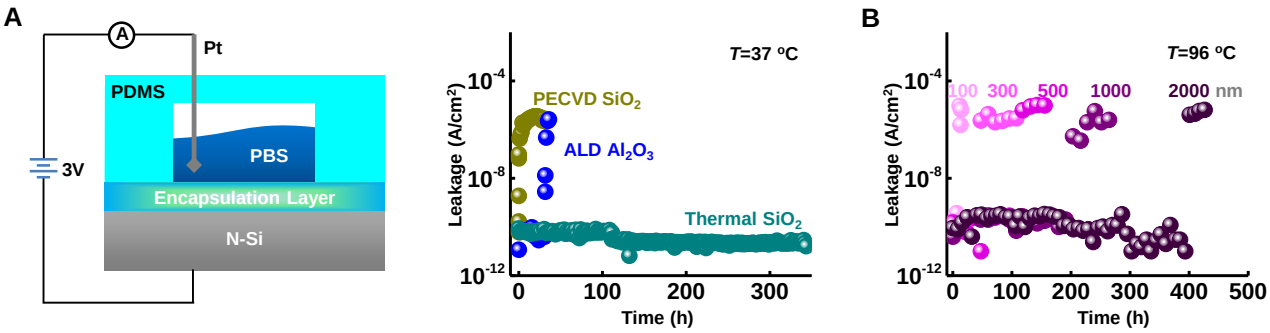

A
A
Pt
PDMS
PBS
3V
Encapsulation Layer
N-Si
T=37 °C
PECVD SiO2
ALD Al2O3
Thermal SiO2
Leakage (A/cm²)
10-4
10-8
10-12
0
100
200
300
Time (h)
B
T=96 °C
100
300
500
1000
2000 nm
Leakage (A/cm²)
10-4
10-8
10-12
0
100
200
300
400
500
Time (h)

Figure S4

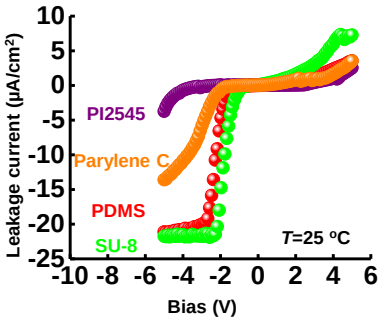

Leakage current (μA/cm²)
10
5
0
-5
-10
-15
-20
-25
-10 -8 -6 -4 -2 0 2 4 6
Bias (V)
PI2545
Parylene C
PDMS
SU-8
T=25 °C

Figure S5

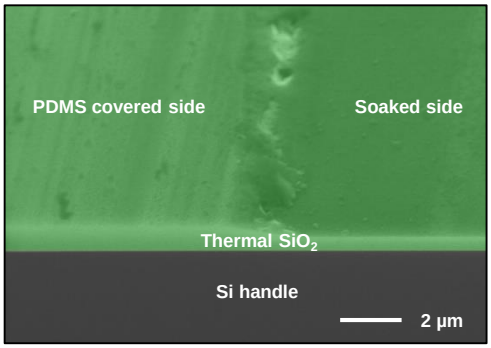


Figure S6

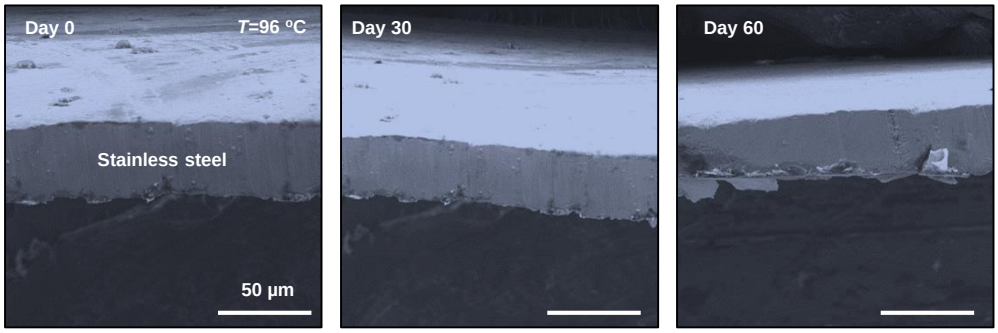


Figure S7

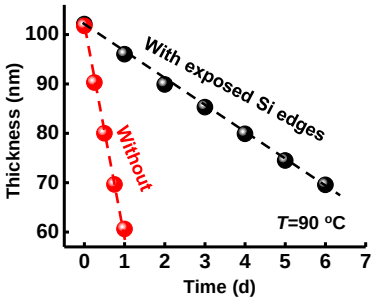

Thickness (nm)
100
90
80
70
60
0
1
2
3
4
5
6
7
Time (d)
With exposed Si edges
Without
T=90 °C

Figure S8

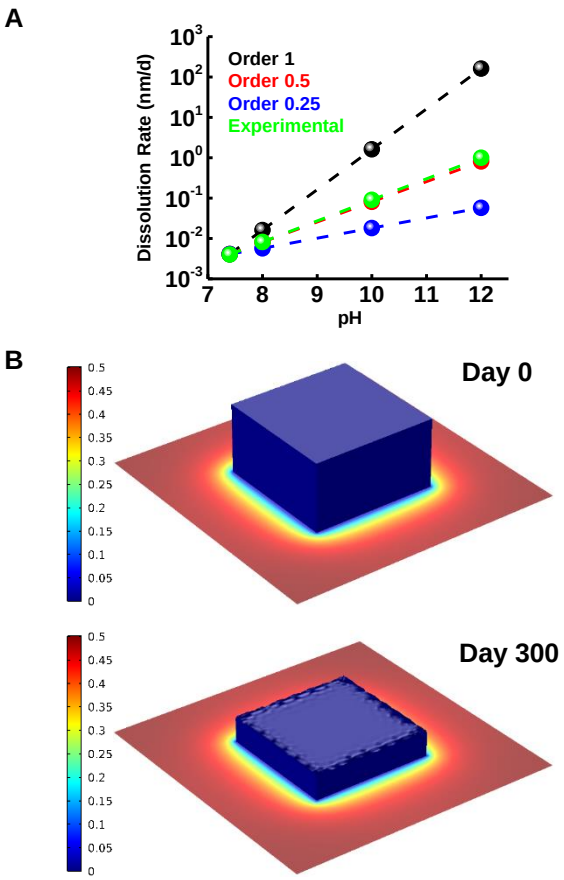

A
Dissolution Rate (nm/d)
Order 1
Order 0.5
Order 0.25
Experimental
pH
B
Day 0
Day 300
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0

Figure S9

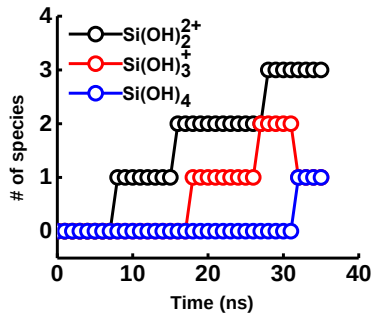


Figure S10

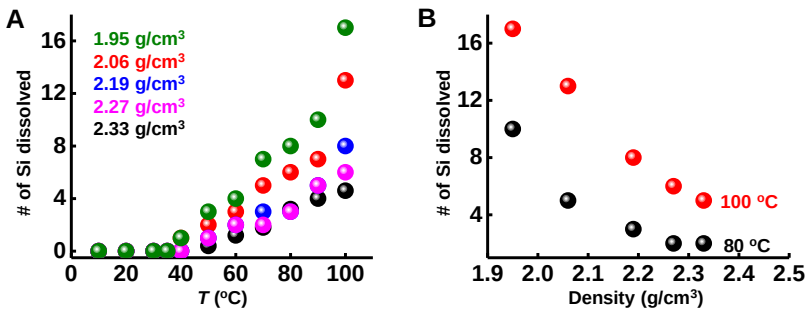

A
1.95 g/cm³
2.06 g/cm³
2.19 g/cm³
2.27 g/cm³
2.33 g/cm³
# of Si dissolved
0
4
8
12
16
0
20
40
60
80
100
T (°C)
B
# of Si dissolved
4
8
12
16
100 °C
80 °C
1.9
2.0
2.1
2.2
2.3
2.4
2.5
Density (g/cm³)

Figure S11

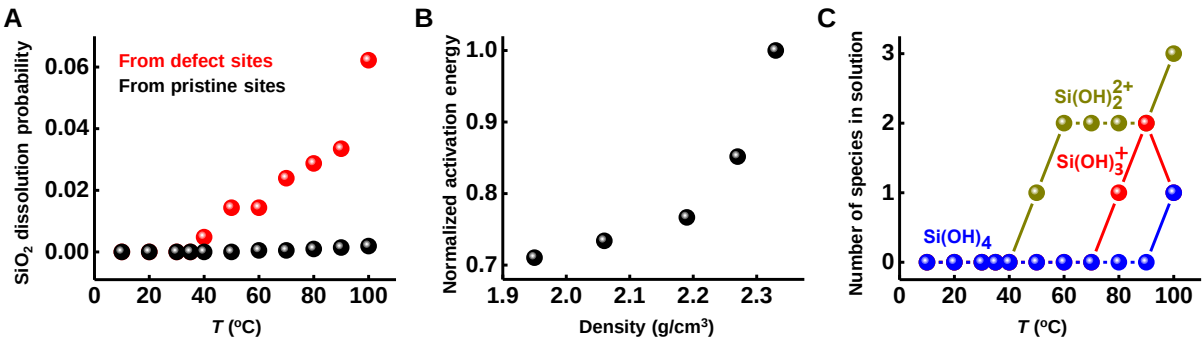

A
SiO2 dissolution probability
From defect sites
From pristine sites
0.06
0.04
0.02
0.00
0
20
40
60
80
100
T (°C)
B
Normalized activation energy
1.0
0.9
0.8
0.7
1.9
2.0
2.1
2.2
2.3
Density (g/cm3)
C
Number of species in solution
Si(OH)42+
Si(OH)3+
Si(OH)4
3
2
1
0
0
20
40
60
80
100
T (°C)

Figure S12

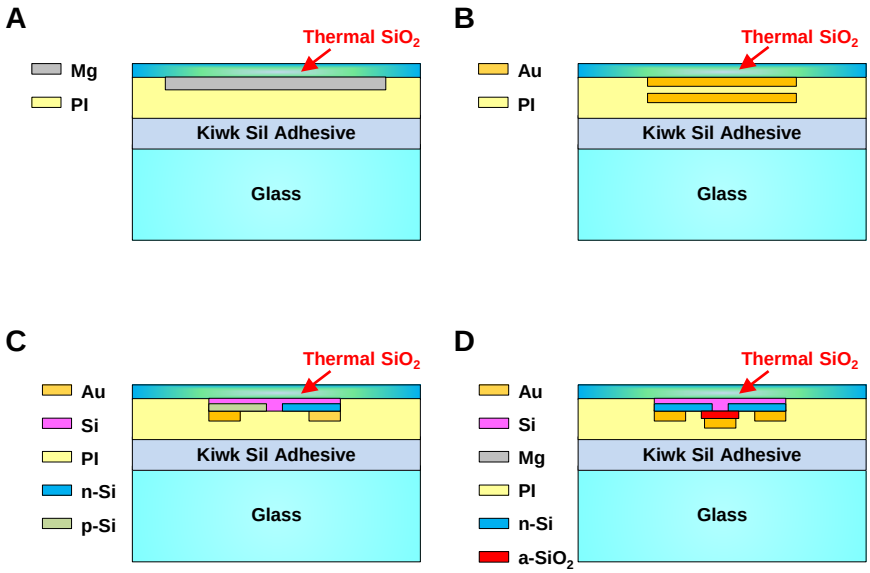

A
Mg
PI
Thermal SiO2
Kiwk Sil Adhesive
Glass
B
Au
PI
Thermal SiO2
Kiwk Sil Adhesive
Glass
C
Au
Si
PI
n-Si
p-Si
Thermal SiO2
Kiwk Sil Adhesive
Glass
D
Au
Si
Mg
PI
n-Si
a-SiO2
Thermal SiO2
Kiwk Sil Adhesive
Glass

Figure S13

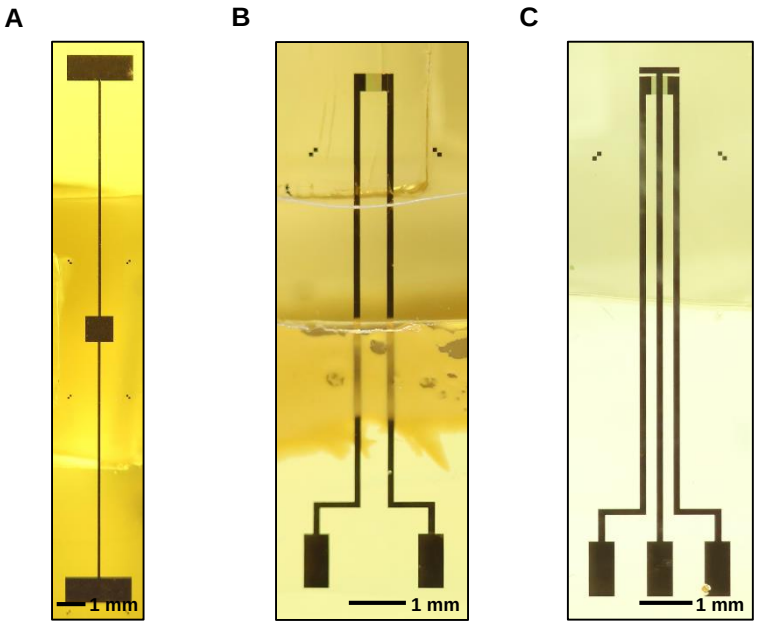


Figure S14

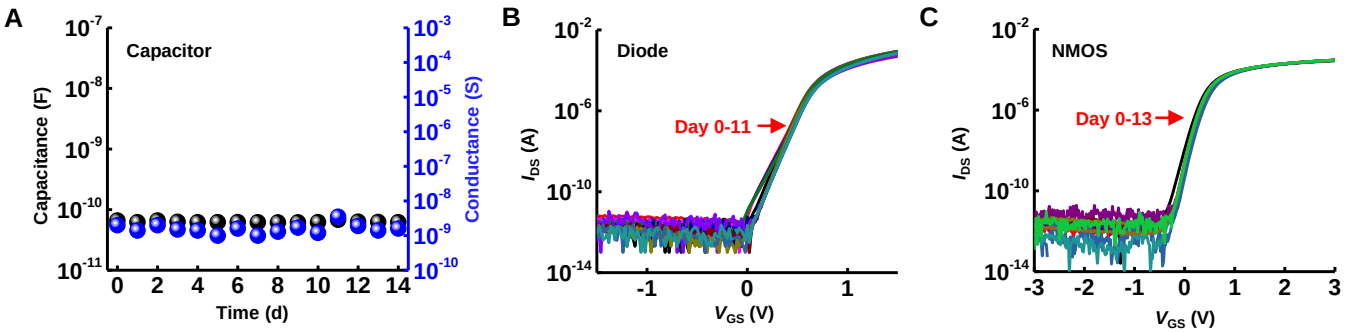
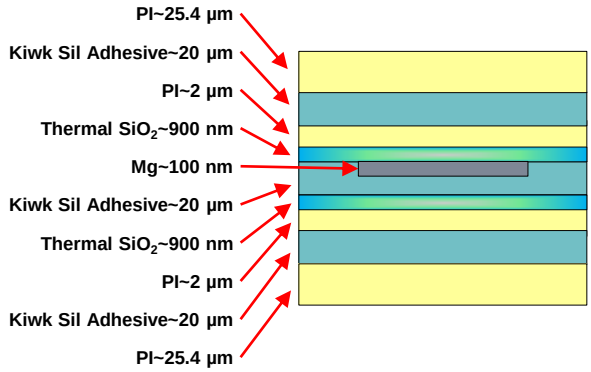

A
Capacitor
Capacitance (F)
Conductance (S)
Time (d)
B
Diode
Day 0-11
I_{DS} (A)
V_{GS} (V)
C
NMOS
Day 0-13
I_{DS} (A)
V_{GS} (V)

Figure S15

A



B

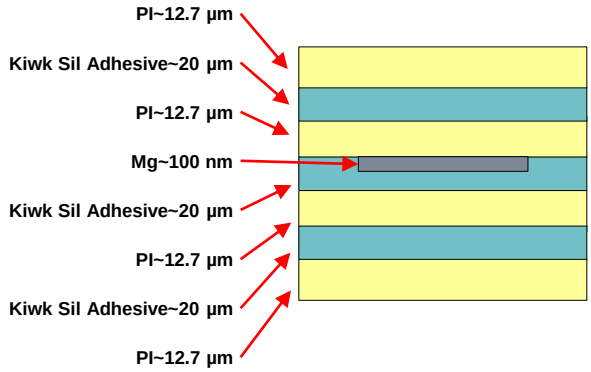


Figure S16

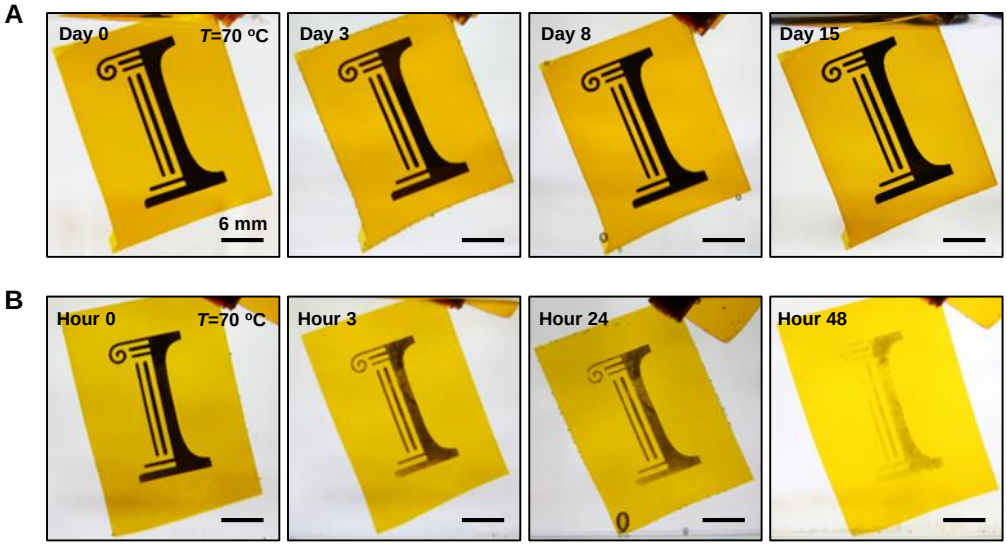

A
Day 0
T=70 °C
6 mm
Day 3
Day 8
Day 15
B
Hour 0
T=70 °C
Hour 3
Hour 24
Hour 48

Figure S17

Figure S18

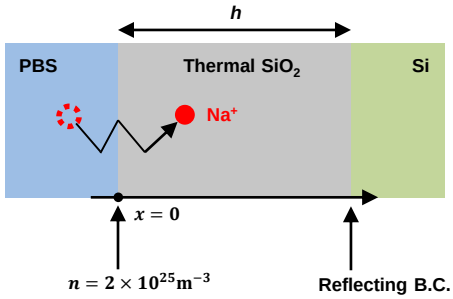


Figure S19

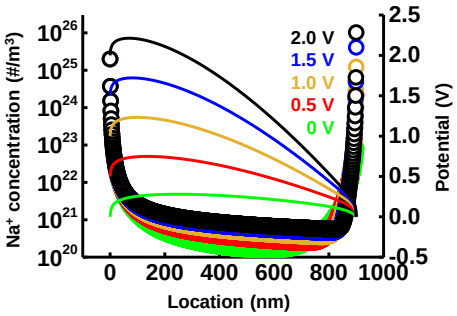

2.0 V
1.5 V
1.0 V
0.5 V
0 V
Na+ concentration (#/m3)
Potential (V)
Location (nm)
10^26
10^25
10^24
10^23
10^22
10^21
10^20
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0
200
400
600
800
1000

Figure S20

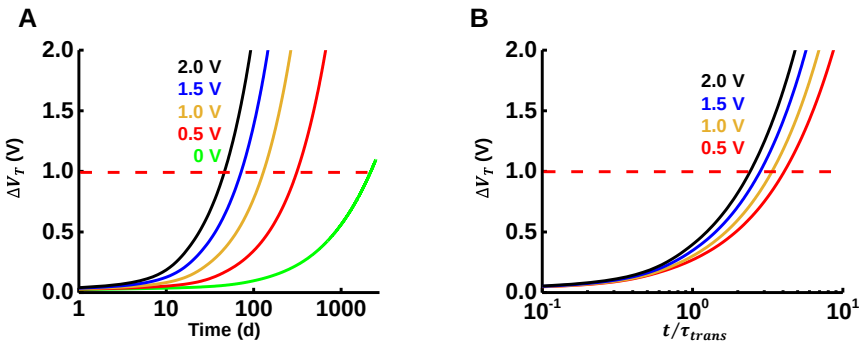

A
2.0
1.5
1.0
0.5
0.0
ΔV_T (V)
2.0 V
1.5 V
1.0 V
0.5 V
0 V
1
10
100
1000
Time (d)
B
2.0
1.5
1.0
0.5
0.0
ΔV_T (V)
2.0 V
1.5 V
1.0 V
0.5 V
10^{-1}
10^{0}
10^{1}
t/τ_{trans}

Figure S21

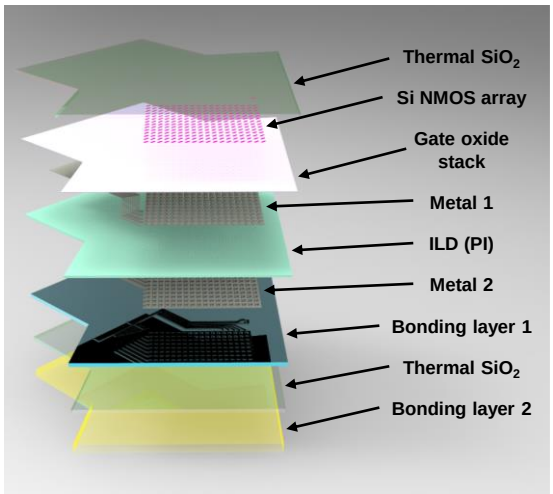

Thermal SiO_2
Si NMOS array
Gate oxide stack
Metal 1
ILD (PI)
Metal 2
Bonding layer 1
Thermal SiO_2
Bonding layer 2

Figure S22

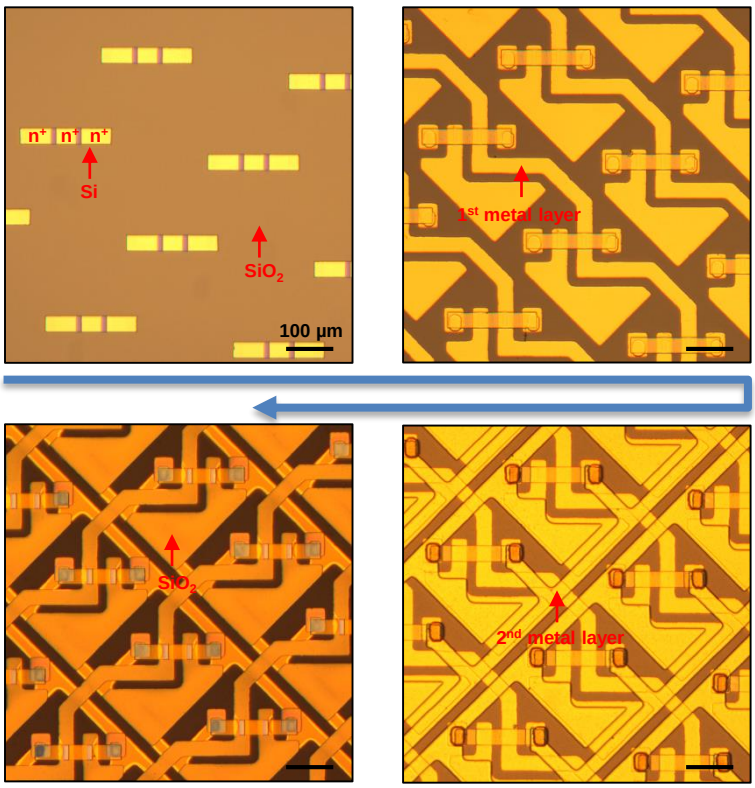


Figure S23

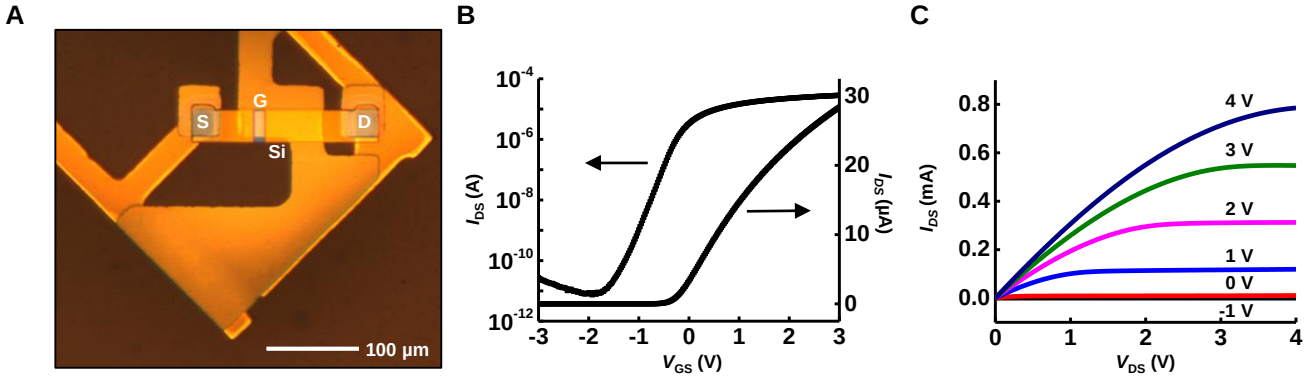

A
G
S
D
Si
100 μm
B
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
I_{DS} (A)
30
20
10
0
I_{DS} (μA)
-3
-2
-1
0
1
2
3
V_{GS} (V)
C
0.8
0.6
0.4
0.2
0.0
I_{DS} (mA)
4 V
3 V
2 V
1 V
0 V
-1 V
0
1
2
3
4
V_{DS} (V)

Figure S24

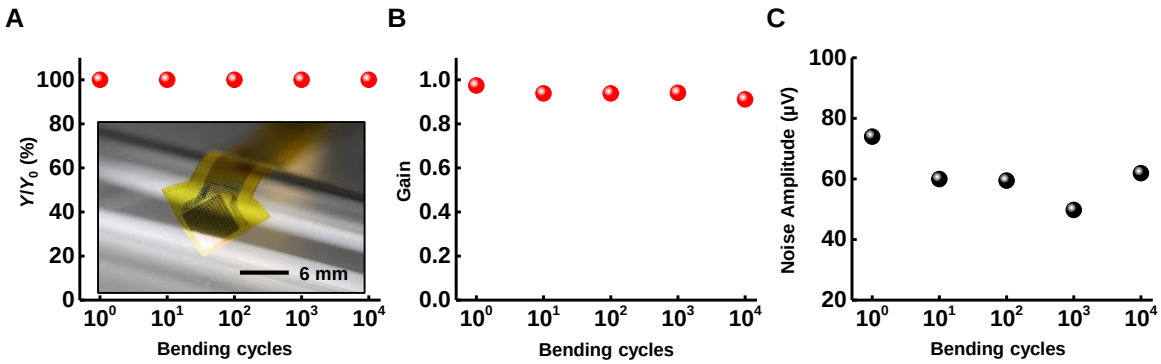

A
B
C
100
80
60
40
20
0
Y/Y0 (%)
6 mm
10^0
10^1
10^2
10^3
10^4
Bending cycles
1.0
0.8
0.6
0.4
0.2
0.0
Gain
Noise Amplitude (μV)

Figure S25