Supporting Information

Measurement of DNA translocation dynamics in a solid-state nanopore at 100-ns temporal resolution

Siddharth Shekar[1], *David Niedzwiecki*[2], *Chen-Chi Chien*[2], *Peijie Ong*[3], *Daniel Fleischer*[1], *Jianxun Lin*[4], *Jacob Rosenstein*[5], *Marija Drndic*[2], *Kenneth L. Shepard*[1*]

[*]Corresponding author: shepard@ee.columbia.edu

[1] Department of Electrical Engineering, Columbia University, New York, NY 10027

[2] Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, PA 19104

[3] Department of Applied Physics and Applied Mathematics, Columbia University, New York, NY 10027

[4] BGI-Shenzhen, Shenzhen, China

[5] School of Engineering, Brown University, Providence, RI 02912

1. Realization of large R_F on-chip

Fig. S1 shows a more detailed view of the simplified schematic shown in Fig. 1d. The red dashed box indicates components present on-chip while the black dashed box indicates the components used to realize the tunable, linear R_F. Diode-connected transistors M_D and $200M_D$ (at 200× the gate width of M_D) implement active current-division by a factor of 200. The effective R_F realized by this circuit has a value of $3.75 \times 10^3 \times 200 = 7.5$ MΩ.

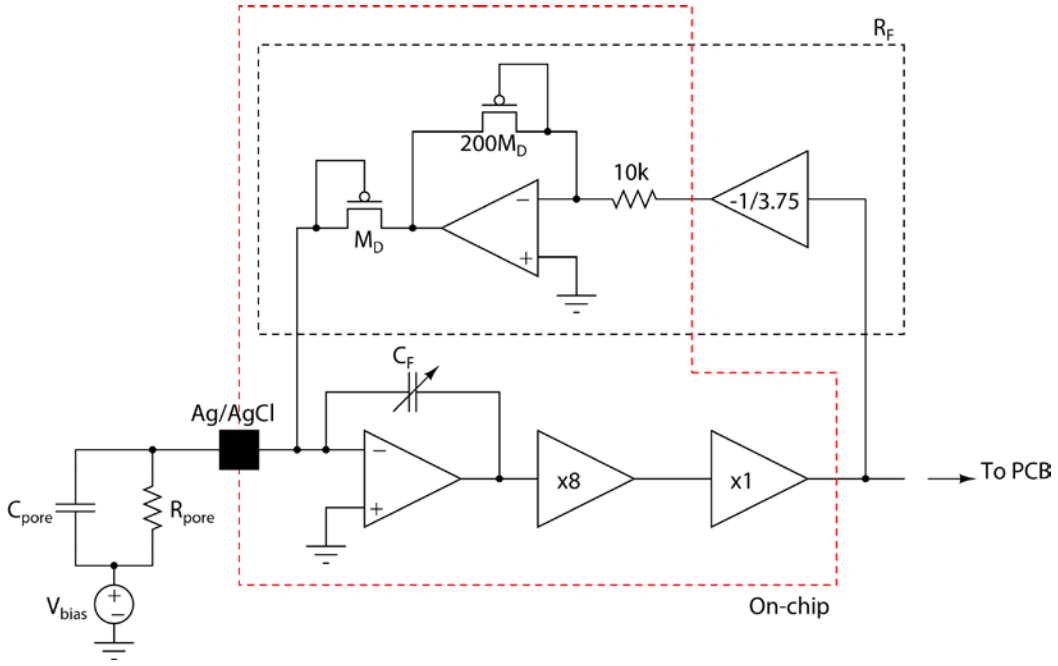

Figure S1. Detailed schematic showing the feedback network used to implement R_F

Assuming that the current-divider loop is fast enough and the integrator operational amplifier (op-amp) has an open-loop transfer function given by $A(s)$, we can show that the open-loop gain of the system in open-headstage configuration ($R_{pore} = \infty, C_{pore} = 0$) is given by $L(s) = \frac{A(s)}{1+A(s)} \times 8 \times \frac{1}{R_F} \times \frac{1}{sC_F}$. Note that this expression also neglects the effect of C_I (Fig. 1d). The closed-loop transimpedance gain is then given by

$$F(s) = \frac{\frac{A(s)}{1+A(s)}\frac{8}{sC_F}}{1+\frac{A(s)}{1+A(s)}\frac{8}{sC_F R_F}} = \frac{A(s)\frac{8}{sC_F}}{1+A(s)\left(1+\frac{8}{sC_F R_F}\right)}$$

Assuming $A(s) \gg 1$, the DC gain is R_F. Further, this expression implies a closed-loop 3-dB bandwidth set by $1/(2\pi R_F(C_F/8))$. In the low-gain setting, $C_F = 900$ fF and $R_F = 7.5$ MΩ, the pole is set at ≈ 200 kHz. For the high-gain setting, R_F is adjusted to be 45 MΩ and $C_F = 150$ fF such that the 3-dB bandwidth remains unchanged.

During actual experiments, $C_{pore} \neq 0$. In that case, the open-loop gain of the system is modified to $L(s) = \frac{A(s)\frac{C_F}{\sum C_i}}{1+A(s)\frac{C_F}{\sum C_i}} \frac{8}{sC_F R_F}$. Further, the closed loop gain becomes

$$F(s) = \frac{\frac{A(s)\frac{C_F}{\sum C_i}}{1 + A(s)\frac{C_F}{\sum C_i}} \frac{8}{sC_F}}{1 + \frac{A(s)\frac{C_F}{\sum C_i}}{1 + A(s)\frac{C_F}{\sum C_i}} \frac{8}{sC_F R_F}} = \frac{A(s)\frac{C_F}{\sum C_i}\frac{8}{sC_F}}{1 + A(s)\frac{C_F}{\sum C_i}\left(1 + \frac{8}{sC_F R_F}\right)}$$

In the case where $\sum C_i = C_F$, we obtain the expression for F(s) derived above. If $\sum C_i > C_F$, then an additional pole is introduced at $\omega_{UGB}\frac{C_F}{\sum C}$, where $A(s) = \omega_{UGB}/s$ and ω_{UGB} is the unity-gain bandwidth of the op-amp. Thus, if $C_F \ll \sum C_i$, then reducing C_F further affects system bandwidth without yielding significant noise improvement.

2. Frequency response normalization

The transimpedance amplifier schematic shown in Fig. S1 has a 3-dB bandwidth determined by $1/(2\pi R_F(C_F/8))$. The 20-dB/decade roll-off in the gain beyond this frequency is compensated by using active filters on the printed circuit board (PCB). Fig. S2 shows a schematic of the chip followed by two stages of "boosting filters" that restore flat frequency response up until 10 MHz. The boosting starts at 200 kHz and ends at 10 MHz; therefore, the net gain provided by the boosting filter at 10 MHz relative to that at 200 kHz is 10 MHz/200 kHz = 50. Realizing a gain of 50 at 10 MHz using an op-amp on a PCB would require a minimum unity gain bandwidth (UGB) of 500 MHz, which is difficult to achieve. Therefore, two stages are employed; the first stage boosts from 200 kHz to 1.4 MHz while the second boosts from 1.4 MHz to 10 MHz. The net UGB requirement for each stage is then reduced to ~70 MHz, which is more practical.

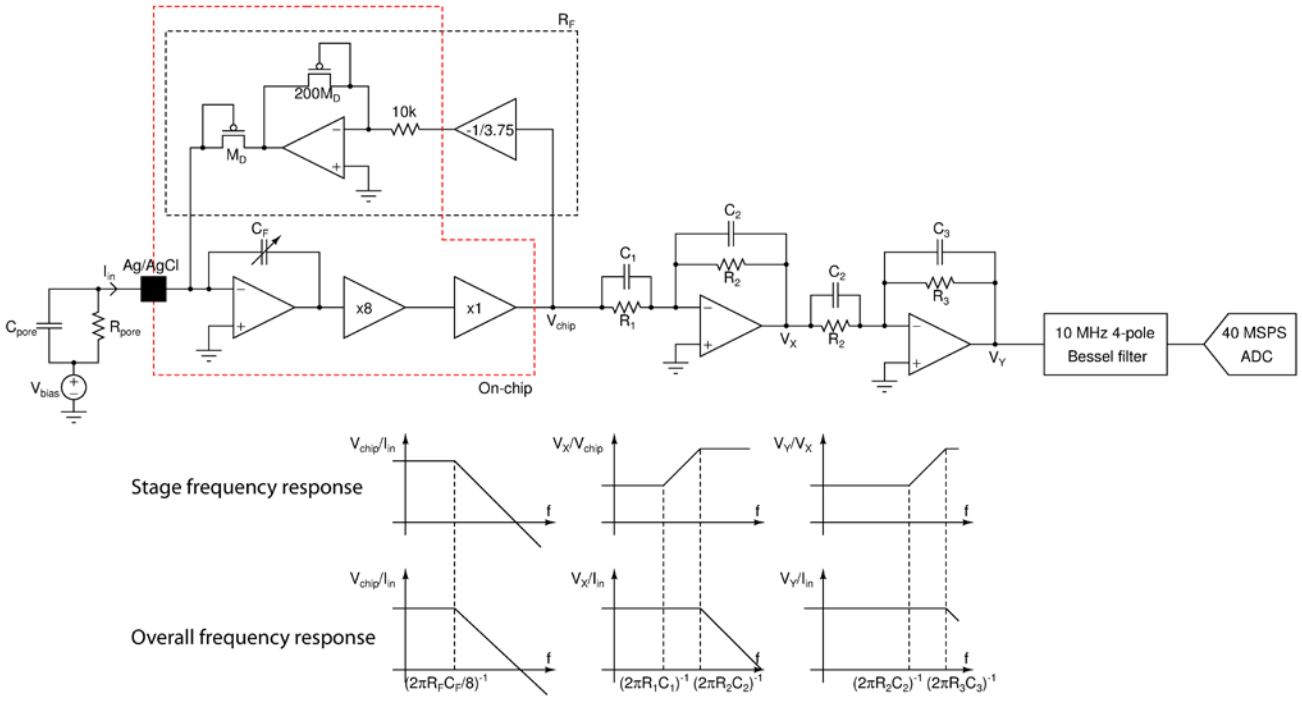

Figure S2. Active filters used to boost the CNP frequency response to 10 MHz.

3. Amplifier chip packaging and post-processing

The amplifier chips we received from the foundry were wirebonded to a 272-pin ball-grid array (BGA) package. In order to protect the gold wirebonds and the chip bondpads from experimental fluidics, the gold wirebonds were then covered using dam-and-fill doughnut epoxy encapsulation with Hysol FP4451TD dam and FP4450HF fill.

Chips encapsulated in this manner were then subjected to aluminum etchant (Al etchant Type A, Transene) in order to remove the top-metal aluminum from the exposed pads connected to the amplifiers. We then electroplated Ag onto these pads up to ~10 μm thickness using Ag electroplating solution (Standard silver solution, Transene). The Ag was then chemically chlorided to form the Ag/AgCl interface (Fig. S3).

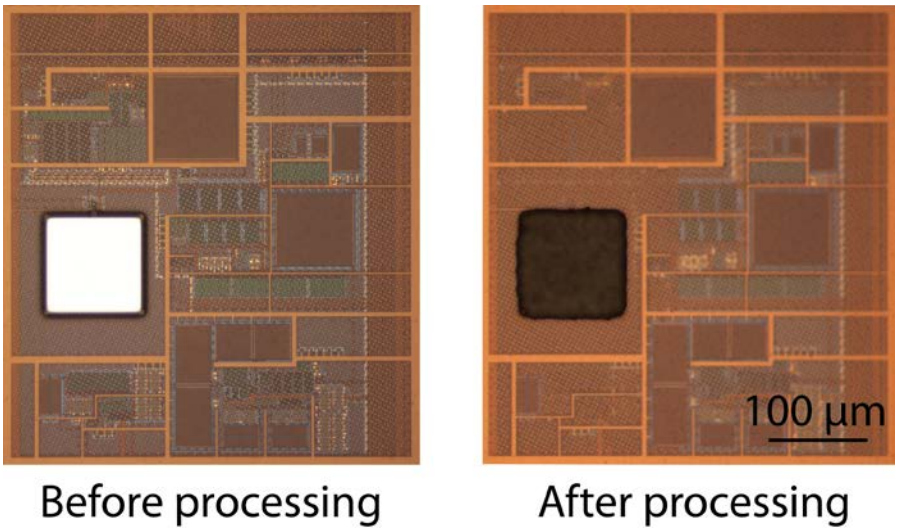

Figure S3. Micrograph of the CNP front-end amplifier before and after post-processing of the on-chip Ag/AgCl electrode.

The amplifier chip was then covered in KWIK-CAST silicone such that only ~200 µm × 200 µm area surrounding the electrode connected to the amplifier to be used was left exposed. This silicone layer was also used to mount a polyethylene trans chamber above the chip. The wiring capacitance, C_W, now associated with the setup is the parasitic capacitance from the liquid in the trans chamber to wiring on the surface of the chip, which we measured to be ~2 pF.

4. Nanopore chip packaging and integration

The nanopore chip (typically 5 mm × 5 mm) was mounted on a PDMS cell using KWIK-CAST silicone with the membrane side exposed. The silicone was then used to paint a thin layer of passivation on the membrane side to reduce parasitic capacitance. Since this operation was performed by hand, there was large variation in the silicone thickness and resulting membrane capacitance. A 100-µm thick silicone layer yields a capacitance per unit area of 0.354 pF/mm^2, but variations in this silicone layer thickness directly impact the membrane capacitance. The membrane window and the side exposed to the *trans* chamber contributed < 2 pF to C_{pore}.

The PDMS cell was then mounted on top of the polyethylene *trans* chamber formed on the amplifier chip. This approach is similar to one described previously to reduce wiring capacitance from the amplifier to the nanopore.[7]

5. Low-frequency noise contributions

The open-headstage integrated noise at 100 and 200 kHz for our CNP platform is 6.1 and 8.1 pA_{RMS} respectively. This flicker noise is primarily due to the amplifiers used in the "boosting filter" and not the transimpedance amplifier itself; this was confirmed by replacing the amplifiers with lower-noise, lower-bandwidth equivalents. We note that, despite these higher flicker noise levels, the low-frequency noise contribution at the bandwidths of interest in this work is negligible, as shown in Table S1.

	Noise up to 100 kHz		**Noise up to 1 MHz**		**Noise up to 5 MHz**	
	Absolute (pA_{RMS})	Contribution of noise at 100 kHz bandwidth to total noise	Absolute (pA_{RMS})	Contribution of noise at 100 kHz bandwidth to total noise	Absolute (pA_{RMS})	Contribution of noise at 100 kHz bandwidth to total noise
Open headstage	6.1	100%	47.8	12.76%	481	1.27%
Pore 1	14.9	100%	125.7	11.85%	1431	1.04%

Table S1. Contributions of low frequency noise to the integrated noise at different bandwidths.

6. Membrane thinning by highly-controlled scanning transmission electron microscope (STEM) electron irradiation

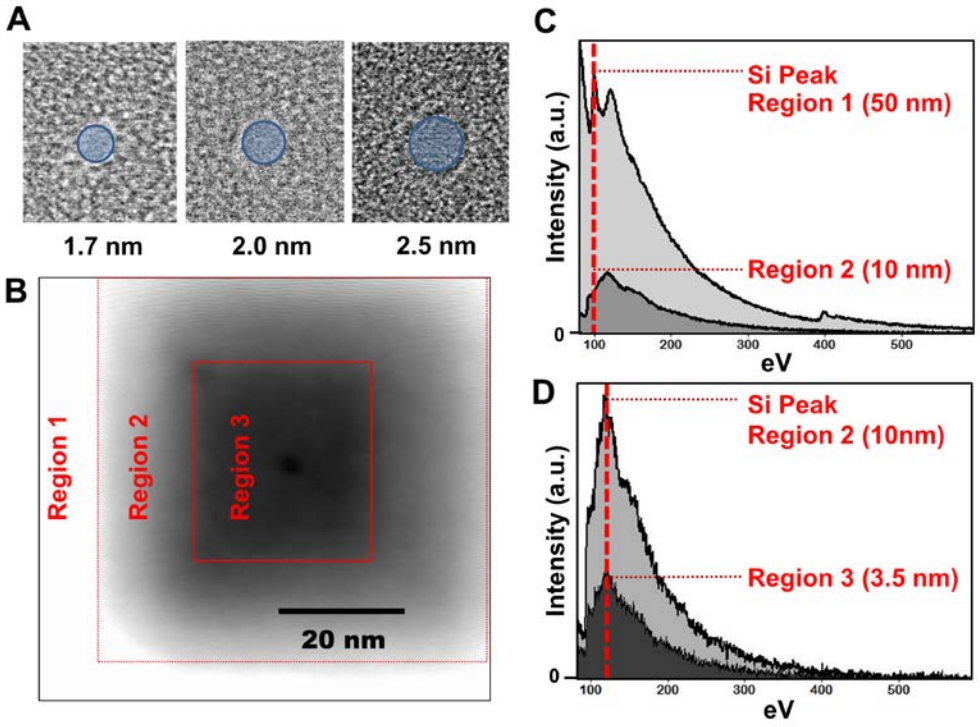

Figure S4. Characterization of nanopores and STEM-thinning in silicon nitride. (a) Bright-field TEM image of nanopores made in STEM-thinned membranes. Circles indicating diameters of 1.7 nm, 2.0 nm, and 2.6 nm are shown in overlay with corresponding nanopores. (b) High Annular Dark Field image of STEM-thinned regions of silicon nitride. Regions are labeled according to the steps in the STEM-thinning process, with Region 1 unthinned, Region 2 thinned to 10 nm, and Region 3 thinned to 3.5nm. (c) Electron-energy loss spectra (EELS) taken of silicon nitride before (Region 1) and after (Region 2) initial thinning. Red markers indicate the Si peak, which drops to 20% of its original value; this corresponds to a thinning from 50 nm to 10 nm. (d) Electron Energy Loss Spectra (EELS) taken of silicon nitride before (Region 2) and after (Region 3) the second thinning process. Red markers indicate the Si peak, which drops to 35%, corresponding to a thinning from 10 nm to 3.5nm. All images were taken using a JEOL 2010F STEM instrument.

Thinning was accomplished by removing silicon and nitrogen from our sample by irradiating with an electron probe of the JEOL 2010F S/TEM in STEM mode. Electron-energy loss spectroscopy (EELS) allows for monitoring this ablation of silicon and nitrogen from the sample, as described previously.[29]

As electrons hit the sample, they are scattered by the atoms in a way that is governed by the energy levels of the atoms. The scattering corresponding to silicon atoms occurs at the energy

level of ~100 eV. The intensity of the number of electrons scattered is proportional to the number of atoms in the sample, which is proportional to the thickness of the sample. Therefore, a ratio of the EELS scattering peak of silicon atoms before and after thinning gives the ratio of the thickness of the sample before and after thinning. The thickness of the sample is related only to the Si peak and N can be removed without changing the thickness.[29]

The membrane thickness was monitored by observing the silicon scattering peak intensity (Si-peak) with EELS. This is done in two steps, the first at a high electron probe current while rastering over an area 100 nm × 100 nm (Fig. S4b, Region 2). The original thickness was grown to 50 nm with low-pressure chemical vapor deposition (LPCVD). This thickness was confirmed by ellipsometry. Thinning was continued until the Si-peak reached 20% of the original value. Therefore, this first step brings the membrane thickness to 10 nm (Fig. S4c). The second thinning step the electron probe current was reduced and rastered over an area of 25 nm × 25 nm (Fig. S4b, Region 3), which allowed for finer control. The thinning continued until the Si peak reduced to 30-40% the intensity of the first thinning step, for a final thickness of 3-4 nm (Fig. S4d).

The nanopore was made at this thickness by stopping the rastering of the electron probe and letting the Si-peak drop to zero background intensity.

After proper alignment of the TEM, including the EELS detector and camera and focusing, it takes approximately 40 minutes to make one good pore when starting with 50 nm thick SiN_x. The first thinning process, to 10 nm thick, takes approximately 20-25 minutes. The second thinning process from 10 nm to 3 nm takes an additional 15 minutes. Maintaining excellent focus on the membrane is key to even thinning. With the gradual thinning at a rate of 5 A per minute, this allows good reproducibility without the danger of overthinning. Pores less than 2 nm thickness are in danger of spontaneously breaking. Pore formation takes less than 5 seconds. The nanopore diameter depends on how long the beam is kept on the sample and accurate focus. Typical nanopores open to a diameter between 1 and 2 nm (probe size is 1 nm). Smaller pores can be enlarged by partially condensing the beam while imaging in bright field TEM such that the diameter can be selected precisely.

7. Two-level translocation current waveforms

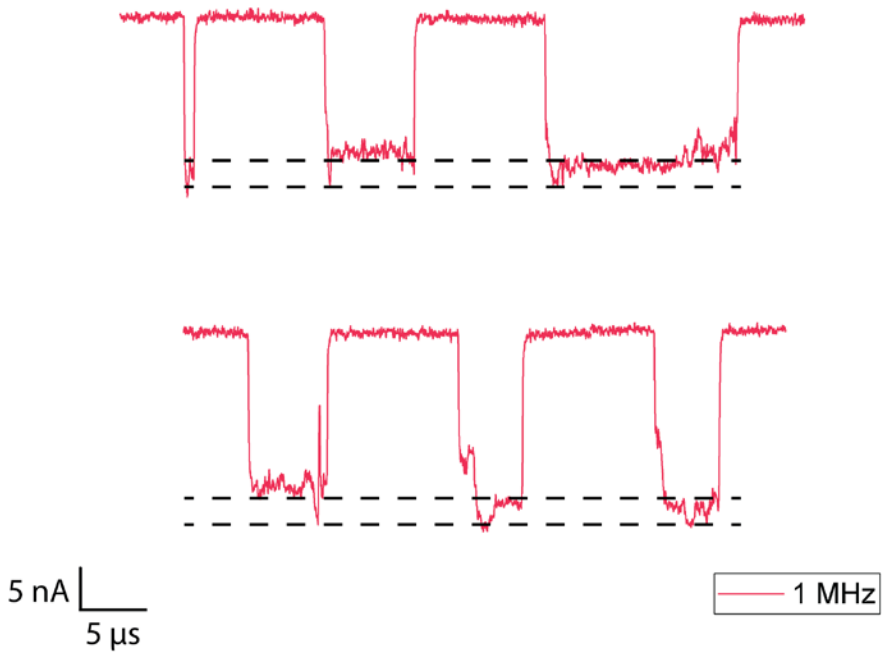

Figure S5. Representative translocation events for 100-nt ssDNA translocating through Pore 3 at 900 mV bias. The upper three events exhibit a deep level followed by a shallow level while the lower three events exhibit a deep level flanked by shallow level dwells before a return to baseline. All events are padded with points from the baseline for reference.

The presence of a shallow and deep level in DNA translocation waveforms has been attributed to a molecule being trapped at the pore's entrance (shallow level) before it translocates through (deep level).[7] However, we observed instances of 100-nt ssDNA translocation events where the deep level was either at the start or in the middle of the event (Fig. S5), which is in agreement with results from other studies.[29]

A collision followed by translocation model does not explain these features. Recent work has proposed that the shallow level may be due to modulation of the access resistance of the pore by the presence of the molecule.[33] This is more likely to explain the event signatures that we observed with the ssDNA molecule getting trapped during its entry or exit from the pore.

8. Comparison with other works

Table S2 compares our work with previous works in the area of high bandwidth single molecule recordings from solid-state nanopores.

	This work	Rosenstein et al.[7]	Balan et al.[21]	Larkin et al.[S1]
Analyte	100-nt ssDNA	25-bp dsDNA	15-kbp dsDNA	13.7-kDa RNase
Max. bandwidth	5 MHz	500 kHz	1 MHz	250 kHz
SNR at max bandwidth	> 10	> 5	> 20	> 10
Min. pore diameter	1.3 nm	3.5 nm	5 nm	4.8 nm
Min. effective thickness	1.2 nm	10 – 15 nm	< 10 nm	6.2 nm
Max. ΔI	30 nA	1.3 nA	4 nA	1 nA
v_n	3.15 nV/√Hz	5 nV/√Hz	1 nV/√Hz	1 nV/√Hz
C_{amp}	< 4 pF *	< 2.15 pF	20 pF	20 pF
C_{pore}	10 pF	6 pF	< 1 pF	< 100 pF

*C_{amp} is composed of $C_I = 1$ pF, $C_F = 0.9$ pF and $C_W \approx 2$ pF. Increase in C_F for bandwidth considerations and C_W due to the larger chip size compared to Rosenstein et al.[7] are responsible for slightly larger C_{amp}.

Table S2. Comparison of high-bandwidth single molecule measurements.

SUPPLEMENTARY REFERENCES

(S1) Larkin, J.; Henley, R. Y.; Muthukumar, M.; Rosenstein, J. K.; Wanunu, M. *Biophys. J.* **2014**, *106* (3), 696–704.