SUBJECT AREAS:

MATERIAL SCIENCE

APPLIED PHYSICS

ELECTRONIC DEVICES

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High performance organic transistor active-matrix driver developed on paper substrate

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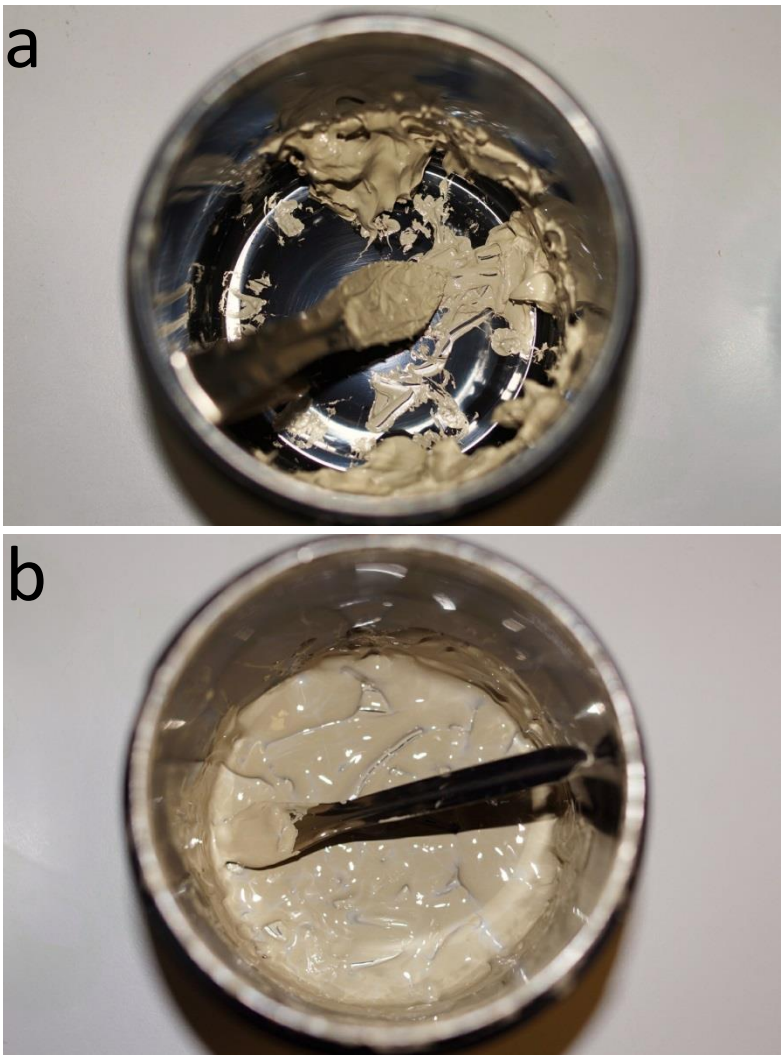

FigureS1| Optical images of screen-printing silver paste. (**a**) Fresh as-received silver paste for electrode patterning. (**b**) Silver paste diluted by solvent (cyclohexanone) in order to improve yield in the through-paper via-hole printing process.

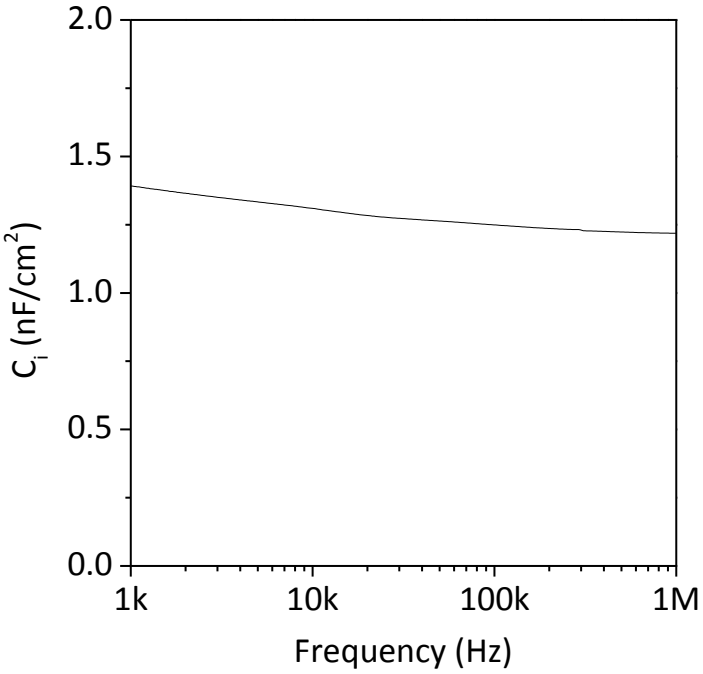

Figure S2| Capacitance-frequency measurement of 2-μm-thick parylene-C. The evaluated dielectric constant of the parylene-C is 3.16 at 1kHz.

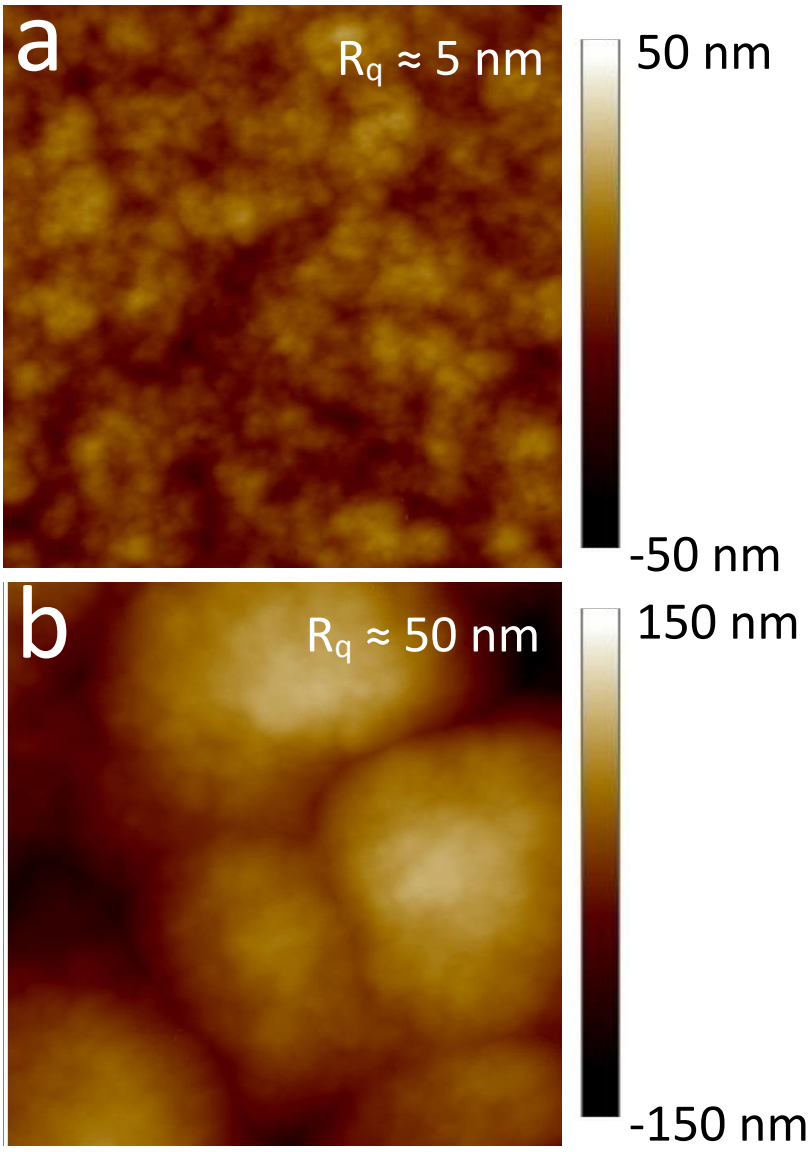

Figure S3| Parylene-C surface morphology measurement. (**a**) Surface AFM image of 2-µm-thick parylene-C on ITO glass. (**b**) Surface AFM image of 2-µm-thick parylene-C on screen-printed silver electrode on printer paper.

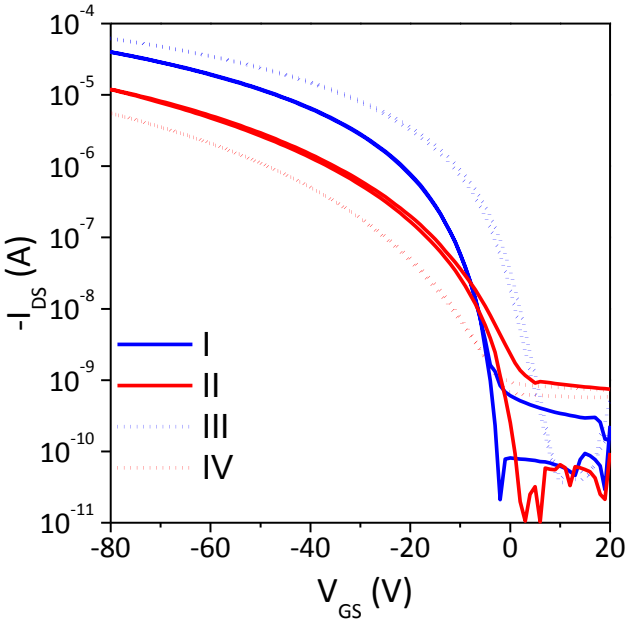

Figure S4| Transfer curves of Structures I-IV. V_{DS} = -80 V, W = 4 mm, L = 100 µm. Labels and measurements correspond to Table 1. DNTT on both substrates exhibits higher mobility and better subthreshold swing than pentacene.

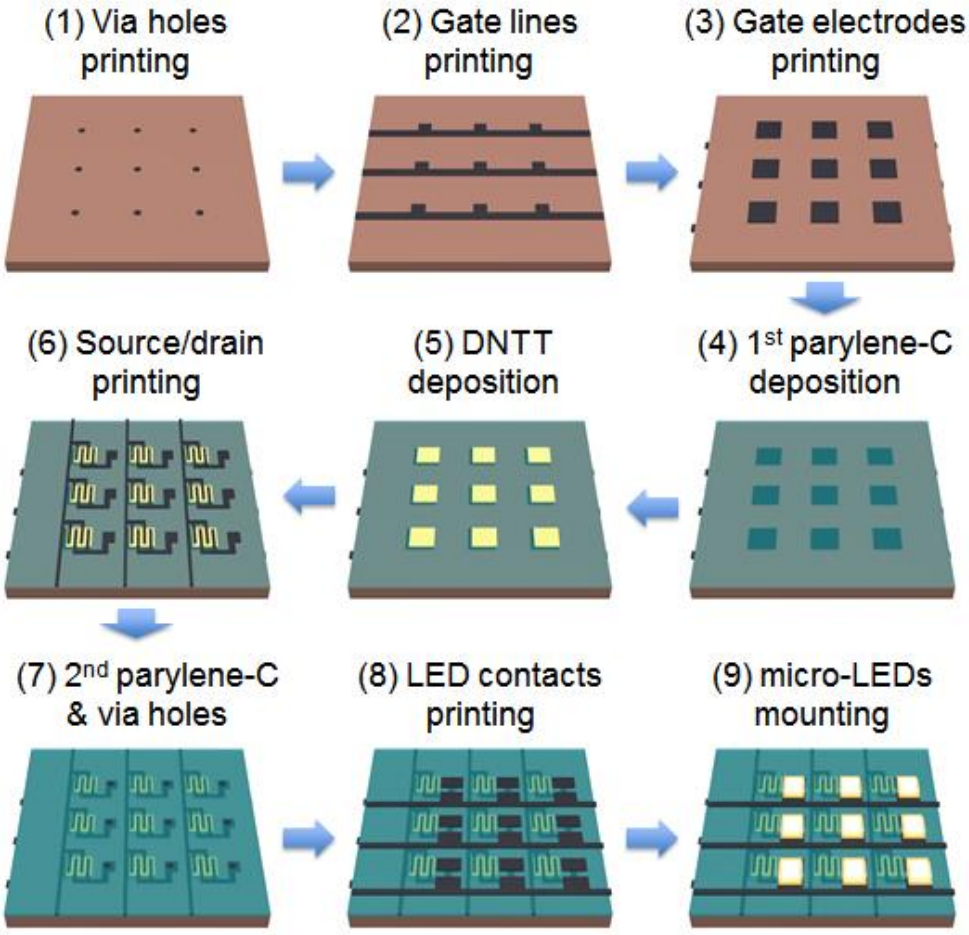

Figure S5| Fabrication process of AM array and LED driver. Steps (1-6) are for AM transistor array and steps (7-9) are for LED integration. Step (1), drill via-holes by CO_2 laser and fill in the via-holes with dilute silver paste. Step (2), screen-print gate lines on the back side of the paper. Step (3), screen-print gate electrodes on the front side of the paper. Step (4), deposit 2-μm-thick parylene-C layer as the gate dielectric. Step (5), deposit 50-nm-thick DNTT as the active layer. Step (6), screen-print silver source electrodes, drain electrodes and drain lines together. Step (7), deposit 5-μm-thick parylene-C layer for insulation between drain lines and source lines. Next, drill via-holes by CO_2 laser to expose source lines. Step (8), screen-print source contact pads (electrically connected to source electrodes through the via-holes in Step (8)) and source lines. Step (9), mount micro-LEDs before the paste dries under an optical microscope. Allow the device to dry 2 hours at room temperature prior to testing.

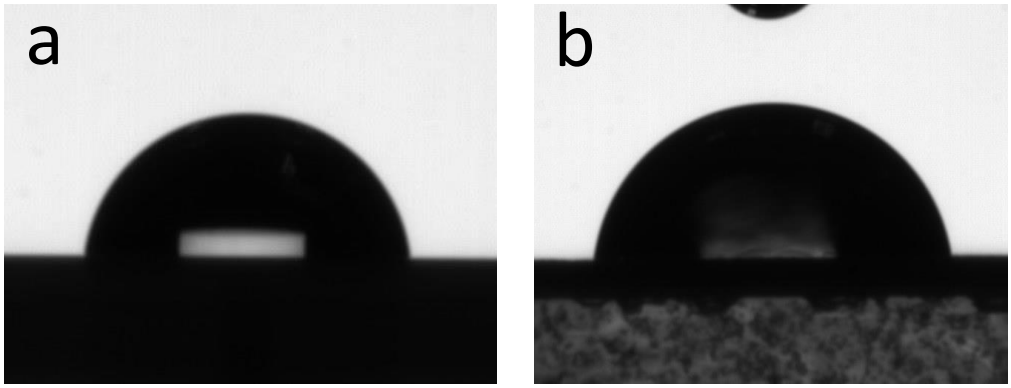

Figure S6| Parylene-C surface energy. (**a**) Parylene-C (2 μm thick) deposited on ITO glass. Water contact angle is 87.3°. (**b**) Parylene-C (2 μm thick) deposited on screen-printed silver electrode on printer paper. Water contact angle is 82.1°.

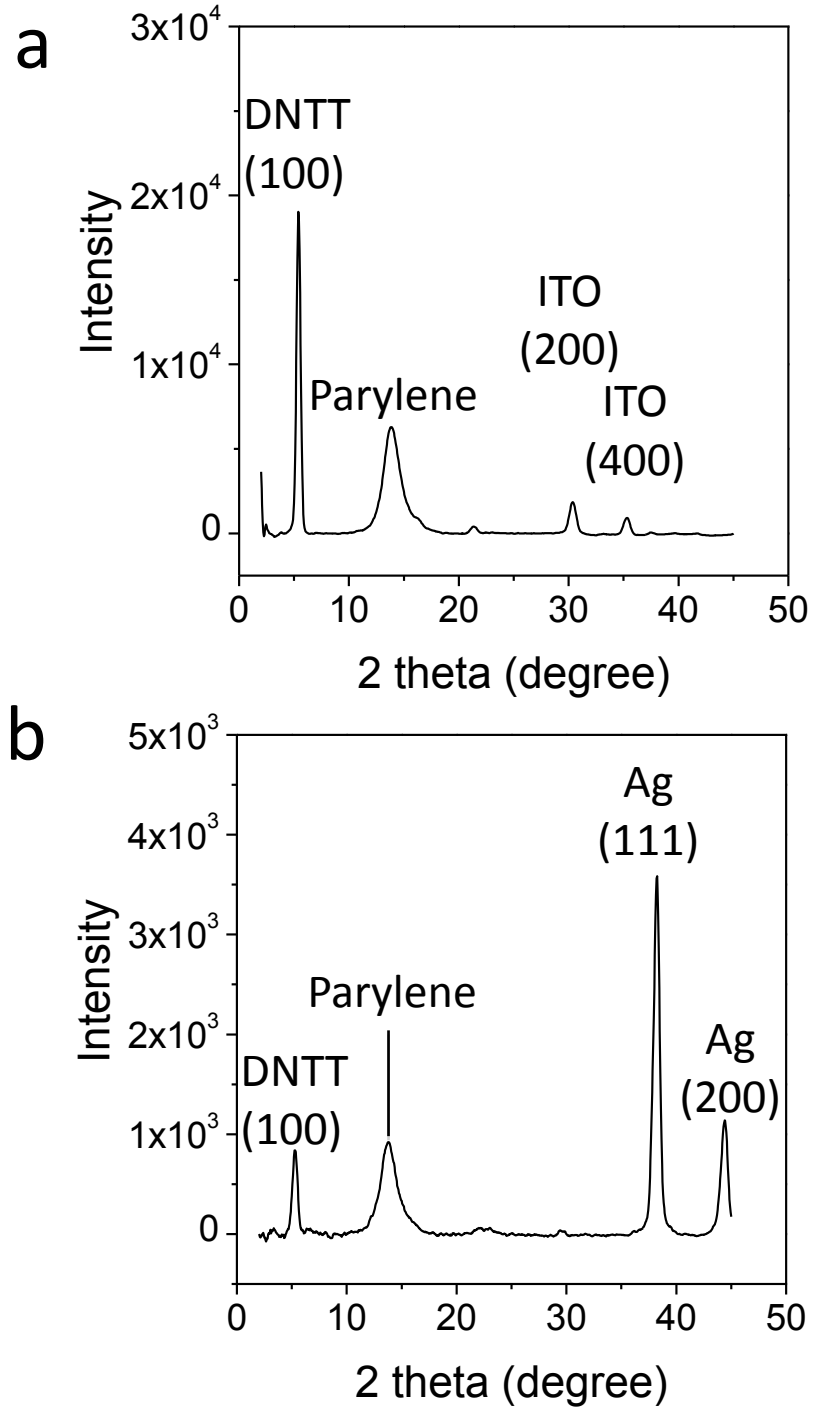

Figure S7| Out of plane XRD of DNTT transistor on glass and paper. (**a**) XRD of structure **I** (ITO glass). (**b**) XRD of structure of structure **III** (paper). Due to the paper substrate roughness, the peak intensity of DNTT is much lower than that of DNTT on ITO glass substrate.

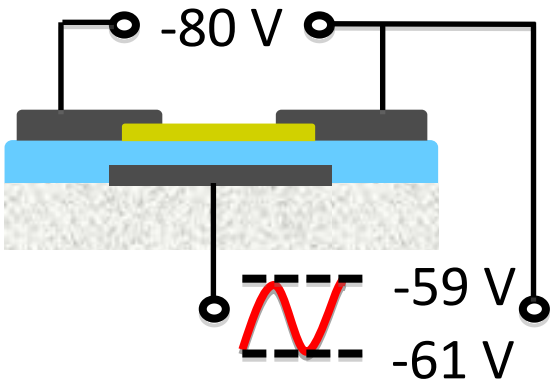

Figure S8| Schematic circuit of cut-off frequency test. AC voltage is applied between the gate and source, and a DC voltage is applied between the drain and source. $I_{GS,\ pk\text{-}pk}$ and $I_{DS,\ pk\text{-}pk}$ are acquired by a resistor combined with a lock-in amplifier.