A fully integrated CMOS microsystem for electrochemical measurements on 32x32 working electrodes at 90 frames per second

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Supporting Information:

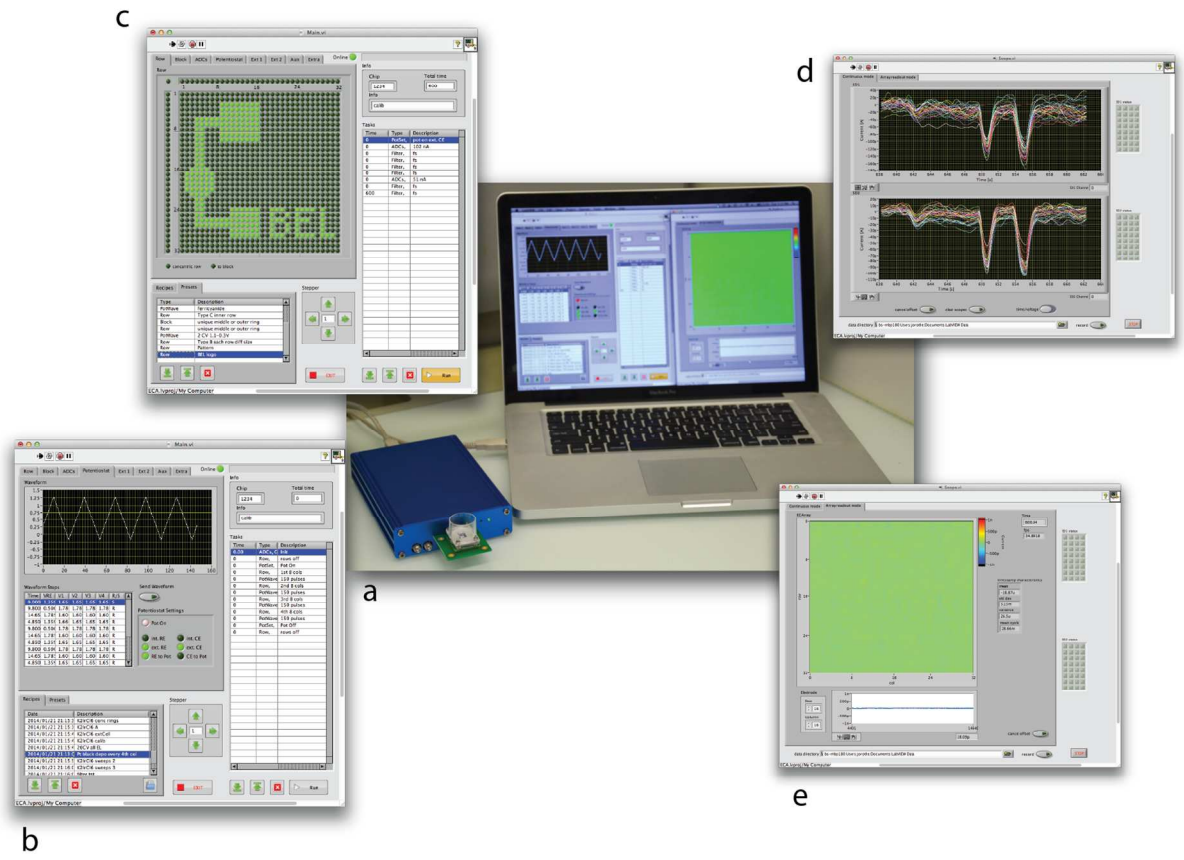

Figure S1. (a) Picture of the CMOS chip assembly, plugged into the measurement system with acquisition laptop. (b-e) Screenshots of the software suite: (b) controlling the potentiostat for cyclic voltammetry, (c) configuring the connectivity, (d) 64 ADC channels in continuous mode and (e) image of whole array to visualize the measurement data.

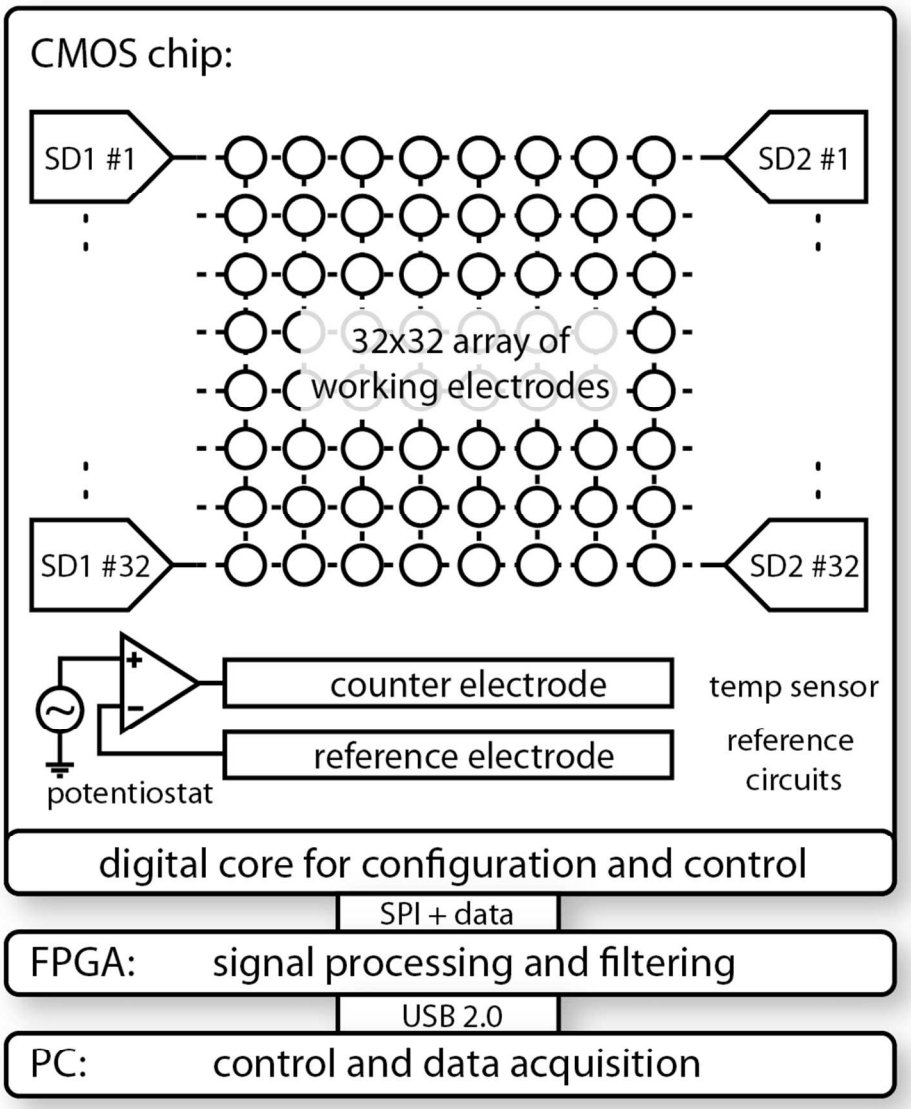

Figure S2. Block scheme showing an overview of the measurement system, the 3 different blocks involved and the digital communication. The CMOS chip with the main features integrated on chip, including the array of electrodes, the sigma-delta current ADCs (SD1 and SD2), the master potentiostat, and auxiliary circuits. The FPGA (Xilinx Spartan 6) includes a microcontroller soft core and custom peripheral cores for filtering of the bit streams from the sigma-delta converters, a real time engine for performing automated tasks, such as running cyclic voltammograms (CVs), and a data framing core to transmit measurement data in packets to the

computer via USB. The real-time engine also controls the fast acquisition of measurements from the whole electrode array: initialization of the ADCs to start the conversion, definition of the connections in the array and filtering of the acquired data. The filters consist of a cascaded integrator-comb (CIC) filter and a moving-average filter in series for each channel. Both filters are variable in order and filter characteristics, to adapt to the bandwidth and resolution needed in the respective experiments. For multiplexed fast scanning of the whole array, 32 third-order CIC filters with a fixed decimation ratio of 64 are implemented.

The experiments are controlled via PC with a graphical user interface programmed in LabVIEW (National Instruments) see also Figure SI-1. The recorded data sets are analyzed in MATLAB (MathWorks).

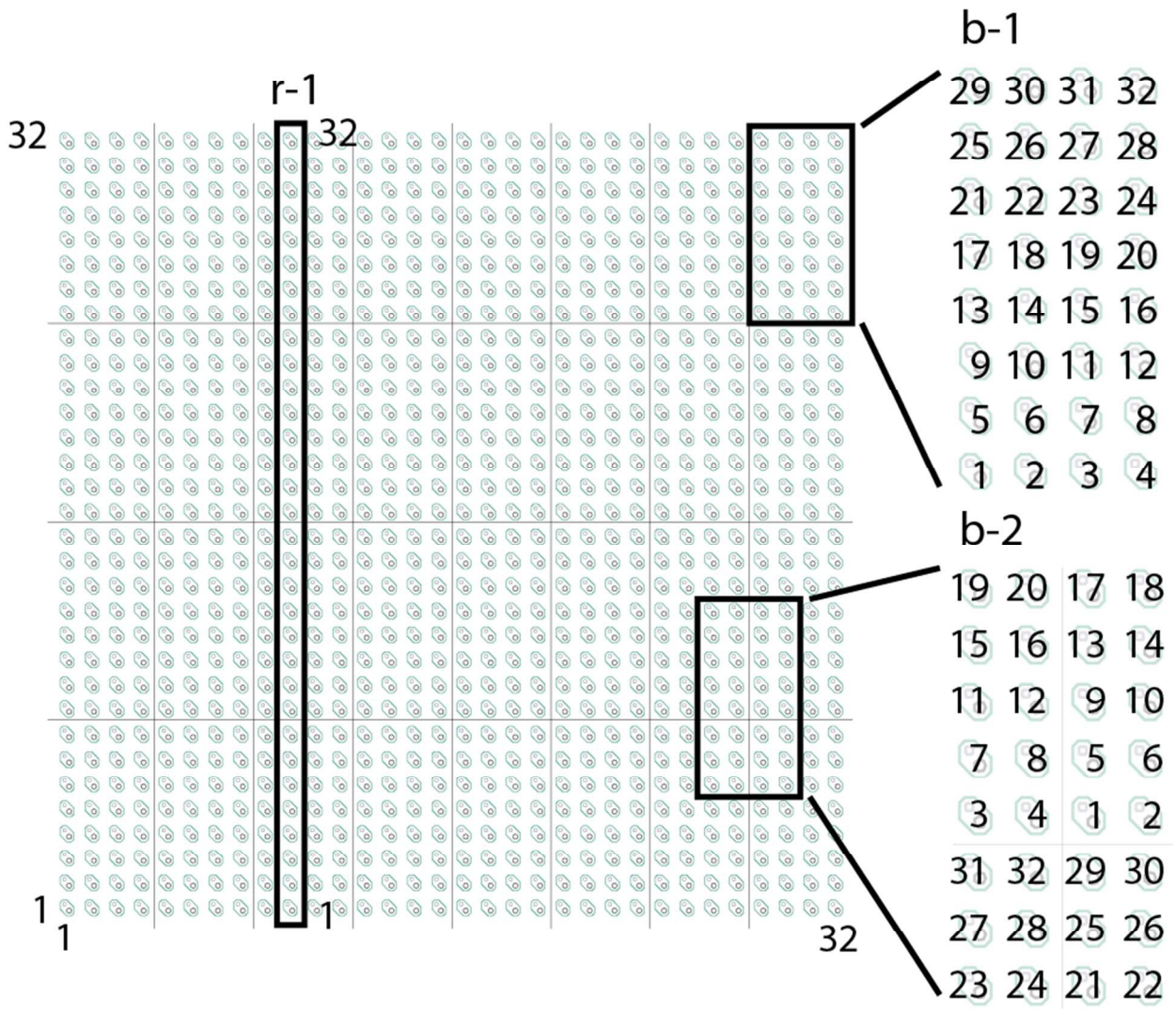

Figure S3. Different connection schemes. In the row scheme (r-1) arbitrary electrodes in one row can be connected to one readout channel. In the block scheme (b-1 and b-2) a subarray of 4x8 electrodes can be connected to the readout channels for obtaining a high-density patch.

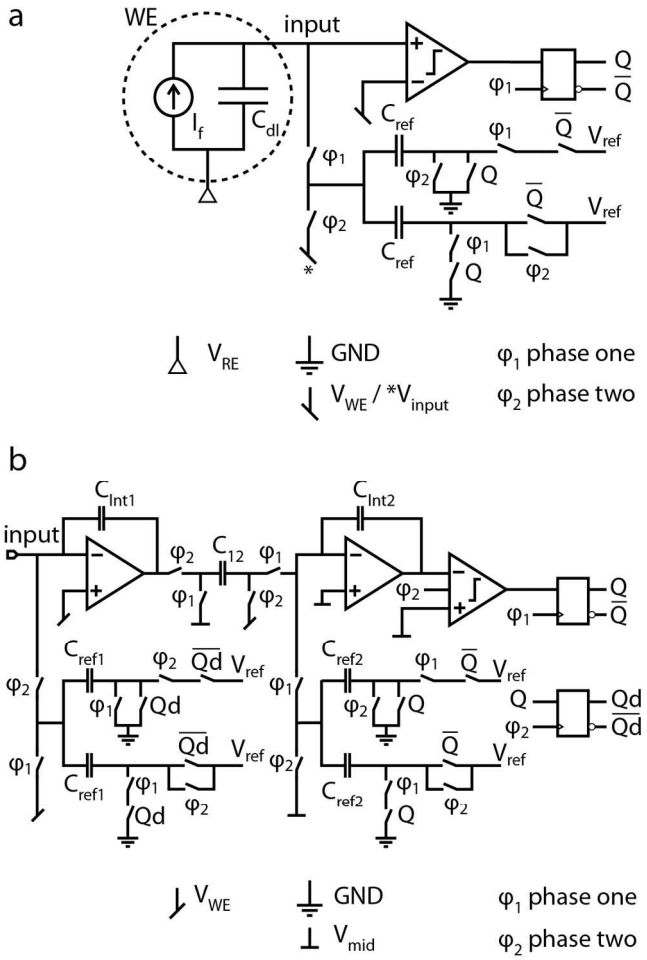

Figure S4. (a) Schematic view of the 1st-order sigma-delta converter. The double-layer capacitance (C_{dl}) of the electrode/electrolyte interface (shown in the dashed circle) is used as a circuit element. Using the electrode-electrolyte double layer as an integration capacitor is not ideal, mostly because the charge of the reference capacitors (C_{ref}) is not completely delivered to the electrode. Linearity can be improved by connecting the reference capacitors to the input voltage in phase two (* V_{input}) instead of the desired working electrode voltage (V_{WE}). (b) Schematic view of the 2nd-order sigma-delta converter. The first-stage amplifier keeps the voltage at the working electrode continuously at V_{WE}. In order to obtain a large voltage range,

the amplifier has a rail-to-rail input stage. Due to the sigma-delta loop, the average output of the first integrator is kept around the voltage of the input node, so that the output stage range needs to be also rail-to-rail. The coefficients of the sigma-delta converter are scaled to limit the signal swing to around 100 mV. The output of the first integrator is shifted to mid-supply by the subsequent capacitor, to reduce the requirement on the input range of the amplifier of the second stage. The clock distribution circuits produce a slow and shifted clock so that each converter operates on each channel at a different time-point in order to avoid simultaneous switching and large peak currents. The internal clock signals for the two sigma-delta converter implementations are provided by two non-overlapping clock phases (φ_1 and φ_2). (a+b) C_{ref} and V_{ref} are the respective reference capacitors and voltages. Q, $\overline{Q}$, Q_d, $\overline{Q_d}$ denote the digital bit stream of the ADCs, the inverse, and the delayed versions of it.

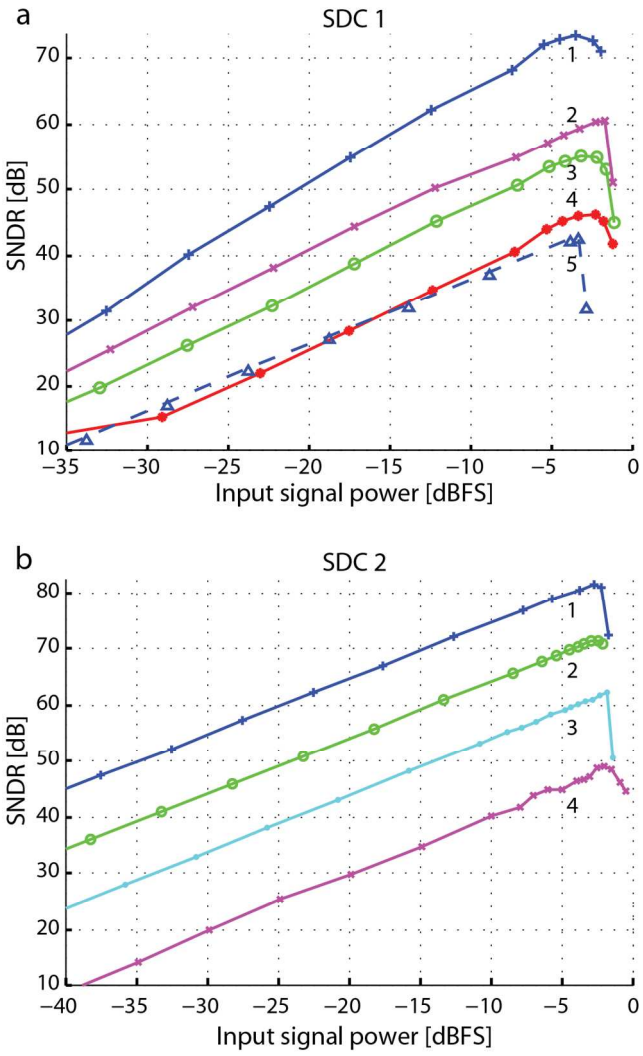

Figure S5. Electric characterization: (a) input signal power in dB of the full scale vs. signal-to-noise-and-distortion ratio (SNDR) of the 1st-order sigma-delta converter for ±1 μA (1), ±400 nA (2, 3, 4) and ±10 nA (5) full-scale range under different conditions. The effect of the compensation circuit can be assessed through comparison of the results of a single electrode (curve 4), of a single electrode with the compensation circuit turned on (curve 3), and of the results of 32 electrodes connected in parallel (curve 2). The larger the ratio of the double-layer capacitance to the reference capacitor value, the better is the performance. When 32 electrodes are connected in parallel, the SNDR increases by 15.3 dB compared to the case when only one

electrode is connected. In the latter case the SNDR can be increased by 9 dB upon turning on the compensation circuit. (b) SNDR of 2^{nd}-order SDC for ±1 μA (1), ±100 nA (2), ±10 nA (3), ±1 nA (4) full-scale range.

Figure S6. Video (in external file SI-6.avi) of amperometric measurement at 0.5 V vs. an external Ag/AgCl reference electrode showing the distribution of an aliquot of H_2O_2 injected in the center of the liquid phase on top of the array, taken at a frame rate of 89 fps. Electrodes were modified by depositing Pt black. The image size corresponds to an area of 3.2 by 3.2 mm^2. Video is the interpolated data from figure 7 and shown in half of real time for better visibility.

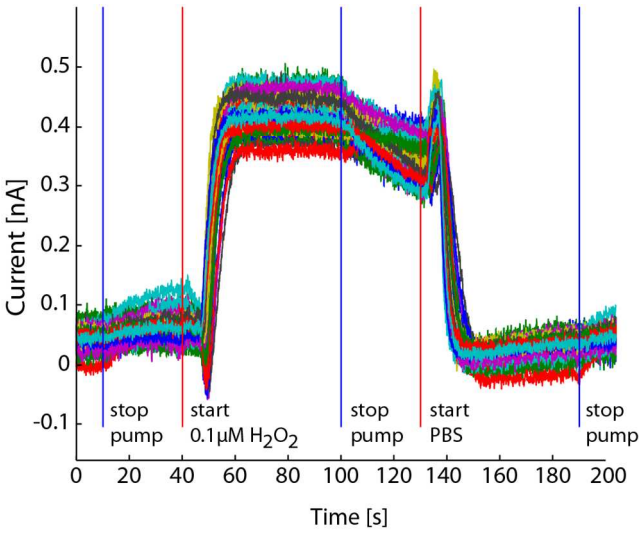

Figure S7. Raw data of amperometric H_2O_2 calibration experiments, measured with 32 individual electrodes of 25 µm diameter. A simple fluidic PDMS chamber was mounted atop the array. A syringe pump was used to pump different concentrations of H_2O_2 in PBS at a flow rate of 10 µl/s over the array. The on-chip counter and pseudo-reference electrodes were used, with the working electrodes being set to 700 mV vs. Pt. The sensitivity is 4.5 nA/µM, the theoretical limit of detection is 13 nM (3 times the background noise).

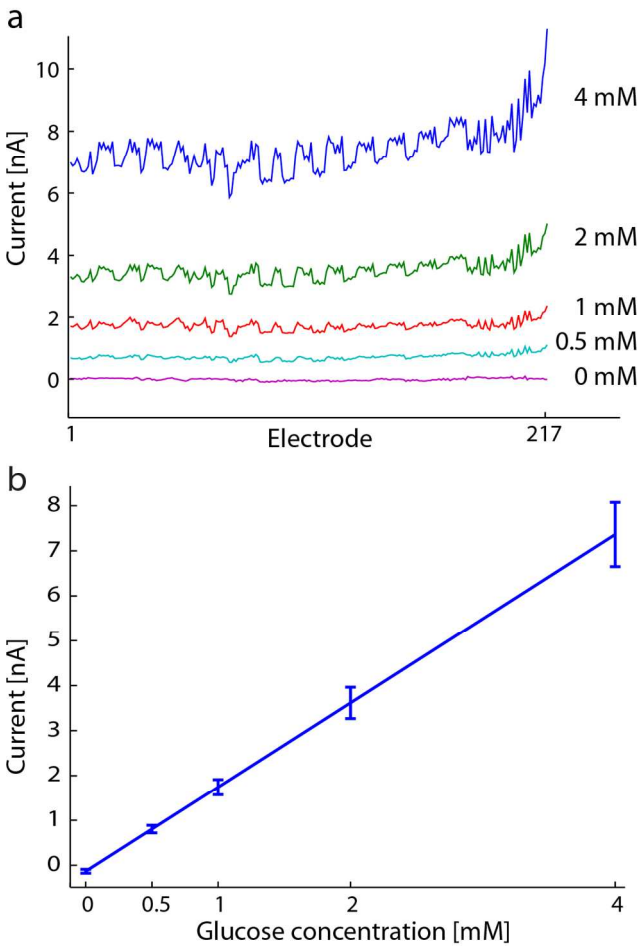

Figure S8. Calibration curve of the glucose biosensor (see manuscript Figure 7). a.) response of all 217 functionalized electrodes to additions of 0.5 mM, 0.5 mM, 1 mM, 2mM of glucose. b.) Mean response of the glucose sensors. Error bars denote the standard deviation. Sensitivity is 1.87 nA/mM ±180 pA/mM (mean, ± standard deviation).

SI-9. Protocols for layer deposition:

Pt black layer: Hexachloroplatinic acid (17.5 mM) with lead acetate (0.03 mM) was used for deposition by using voltage pulses. An external Ag/AgCl reference electrode and the on-chip platinum counter electrode were used. Pulses of 500 ms at 0.6 V followed by 250 ms at 0 V vs. Ag/AgCl were applied and repeated over 150 cycles.

Glucose oxidase/poly(o-phenylenediamine) layer: Glucose oxidase (15 kU/ml) in 500 µl de-aerated PBS was mixed with *o*-phenylenediamine (100mM) in 500 ul de-aerated PBS. An external Ag/AgCl reference electrode and an external platinum wire as counter electrode were used. The deposition was achieved by applying cyclic voltage signals in the range of 0 - 0.9 V vs. Ag/AgCl at 50 mV/s over 15 cycles.