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Supplementary Materials for

Stable organic thin-film transistors

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Supplementary Materials

section S1. Electrical properties of μc-OTFTs with different thicknesses of NL

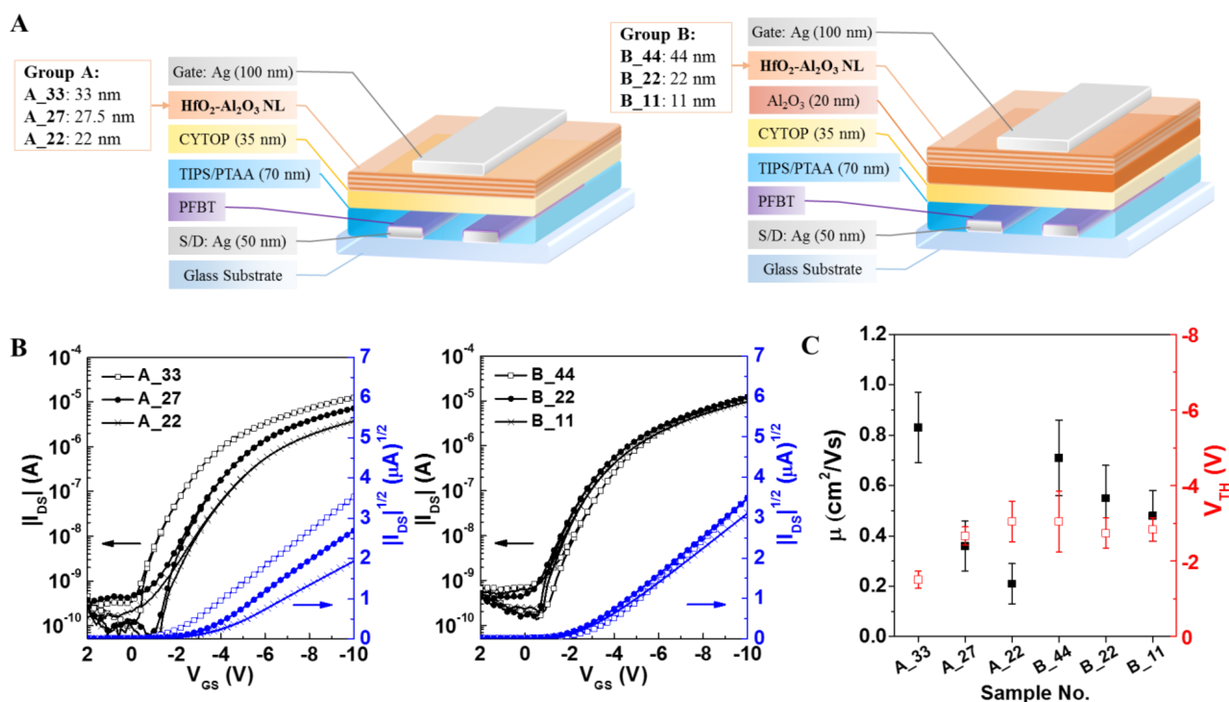

fig. S1. General electrical properties of μc-OTFTs with different configurations of gate dielectric layers. (**A**) The structures of top-gate bottom-contact TIPS-pentacene/PTAA *μc*-OFETs with gate dielectric layers of Group A: CYTOP/ALD Al_2O_3:HfO_2 NL (left) and Group B: CYTOP/ALD Al_2O_3/ALD Al_2O_3:HfO_2 NL (right). (**B**) Pristine transfer characteristics of Group A devices (left) and Group B devices (right). (**C**) Statistic values of mobility μ (black) and threshold voltage V_{TH} (red) of *μc*-OFETs for A_33, A_27, A_22, B_44, B_22, and B_11.

In order to investigate the influence of the NL thickness on the electrical properties and stability of devices, TIPS-pentacene/PTAA *μc*-OTFTs using two types of gate dielectric geometries with different NL thicknesses were fabricated. An illustration of the devices geometries is shown in fig. S1A. The samples with different dielectric layers were studied as two groups, referred to as Group A (sample A_33, A_27, and A_22) and Group B (sample B_44, B_22, and B_11). For Group A, the gate dielectric layer consists of CYTOP (35 nm) and ALD Al_2O_3: HfO_2 NL (varied thicknesses). For Group B, the gate dielectric layer of *μc*-OTFTs consists of CYTOP (35 nm) with metal oxide layers, which are Al_2O_3 (20 nm) and ALD Al_2O_3: HfO_2 NL (varied thicknesses). The thicknesses of dielectric layers for each sample are indicated in fig. S1A.

Figure S1B shows the pristine transfer characteristics of the champion devices (W/L = 2550 μm/180 μm) in Group A and B. All devices were measured in N_2 and exhibited hysteresis-free electrical characteristics. Table S1 shows a summary of the performance parameters measured on pristine *μc*-OTFTs of each type. The field-effect mobility (μ), the threshold voltage (V_{TH}), and the absolute value of (reciprocal) sub-threshold slope ($|S|$) were extracted from transfer curves. The maximum semiconductor-dielectric interfacial trap density was estimated using measured values of $|S|$ (*33*). All *μc*-OTFTs in Group A and B have similar maximum interfacial trap densities around 3.2×10^{12} cm^{-2}, which is consistent with the fact that CYTOP was coated on semiconductor layer as the first dielectric layer for all devices.

table S1. Summary of the device properties and pristine electrical performance.

Sample No.	Dielectric (nm)			C_{ox} (nF cm^{-2})	μ (cm^2 V^{-1} s^{-1})	V_{TH} (V)	|S| (V decade^{-1})	Est. Max. Trap Density (cm^{-2})	# Devices
	CYTOP	Al_2O_3	NL						
A_33	35	0	33	40.8	0.8 ± 0.1	-1.9 ± 0.2	0.70 ± 0.04	2.7×10^{12}	23
A_27	35	0	27.5	42.5	0.4 ± 0.1	-2.6 ± 0.2	0.77 ± 0.03	3.2×10^{12}	17
A_22	35	0	22	43.1	0.2 ± 0.1	-3.0 ± 0.5	0.93 ± 0.03	3.9×10^{12}	11
B_44	35	20	44	36.2	0.7 ± 0.1	-3.0 ± 0.8	0.75 ± 0.03	2.6×10^{12}	9
B_22	35	20	22	40.7	0.6 ± 0.1	-2.7 ± 0.4	0.79 ± 0.02	3.1×10^{12}	12
B_11	35	20	11	42.2	0.5 ± 0.1	-2.8 ± 0.3	0.80 ± 0.02	3.3×10^{12}	5

Figure S1C shows statistic values of μ and V_{TH}. The trends displayed by μ and V_{TH} can be attributed to differences in the gate-dielectric geometry and thickness; since the semiconductor-dielectric interfacial trap densities were the same. As the gate dielectric thickness is decreased, μ decreased from 0.8 cm^2 V^{-1} s^{-1} to 0.2 cm^2 V^{-1} s^{-1} for Group A, and from 0.7 cm^2 V^{-1} s^{-1} to 0.5 cm^2 V^{-1} s^{-1} for Group B. Thicker dielectric layers lead to smaller leakage currents from channel to gate, therefore, higher channel current between source and drain will be measured which results in higher calculated values of μ. By adjusting the thickness of the dielectric layer, we found that A_33 with 33-nm NL showed relatively small V_{TH} and high μ. This result also indicates that the layer-by-layer nanolaminate structure might have a denser configuration that leads to much lower leakage than a single Al_2O_3 layer for the same thickness. To investigate this hypothesis, we measured the leakage current density-electric field characteristics for each type of dielectric layer. As shown in fig. S2, thicker dielectric layers lead to reduced leakage current densities, the leakage current densities of A_33, which is smaller than 5×10^{-8} A cm^{-2} at applied fields up to 3 MV cm^{-1}, are low as those of B_44 and B_22.

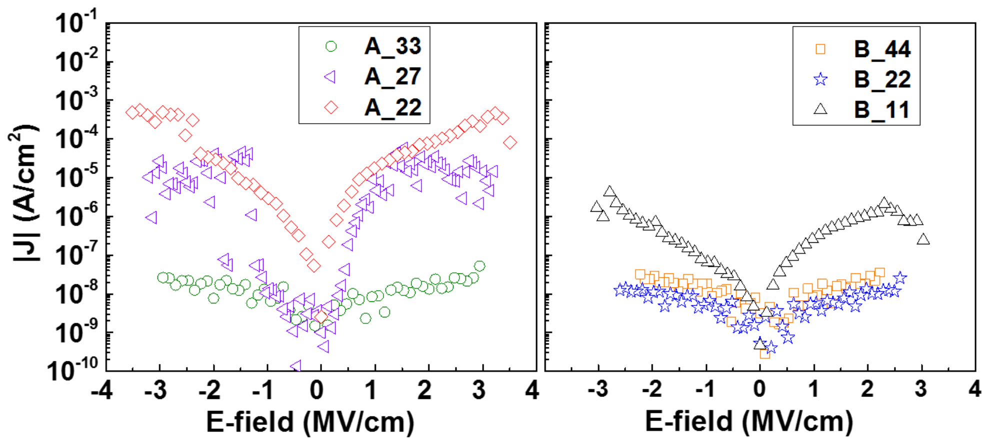

fig. S2. Current density–electric field (*J-E*) characteristics of dielectric layers.

section S2. Environmental stability

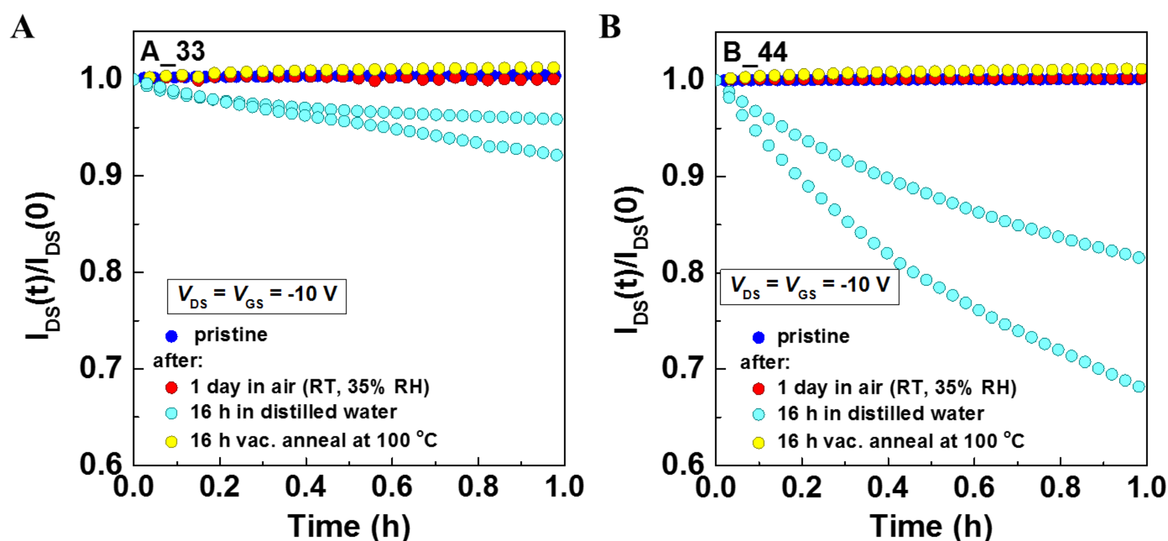

fig. S3. Environmental stability of μc-OTFTs with different configurations of gate dielectric layers. Environmental stability of (**A**) A_33 devices and (**B**) B_44 devices under continuous dc-bias stress for *μc*-OTFTs in different ambient conditions.

Here we compared the environmental stability of A_33 and B_44-type *μc*-OTFTs, which displayed the best characteristics in Group A and B, respectively. To this end, we evaluated the temporal changes in the source-to-drain current I_{DS} during on-state gate bias stress experiments for 1 h (i.e. while *μc*-OTFTs were subjected to a constant gate bias in the saturation regime), before and after exposing all devices to the following environmental conditions: (1) air with relative humidity (RH) of 35% for 1 day; (2) immersion in distilled water for 16 h; (3) vacuum annealing at 100 ºC for 16 h. The samples were briefly transferred into a N_2-filled glove box for testing at each interval. Fig. S3 shows the temporal evolution of the normalized I_{DS} of A_33 and B_44 *μc*-OTFTs for all different environmental conditions. After air exposure, I_{DS} changes of less than 1% were observed in both A_33 and B_44 *μc*-OTFTs, while prolonged immersion in water resulted in larger changes of I_{DS} in B_44 devices than in A_33 devices. The performance of both types of devices recovered after the samples annealed. These general trends are fully consistent with our previous reports on the environmental stability of top-gate *μc*-OTFTs, and in particular, on the detrimental effect that prolonged immersion in water produces on the I_{DS} stability. Remarkably, after 1 h of on-bias stress, A_33 devices display significantly reduced changes of I_{DS}, in the range 4 % to 8 %, compared to those observed on B_44 devices, in the range of 20 % to 35 %. These results provide evidence of the improved environmental stability displayed by A_33 devices.

section S3. One-hour operational stability

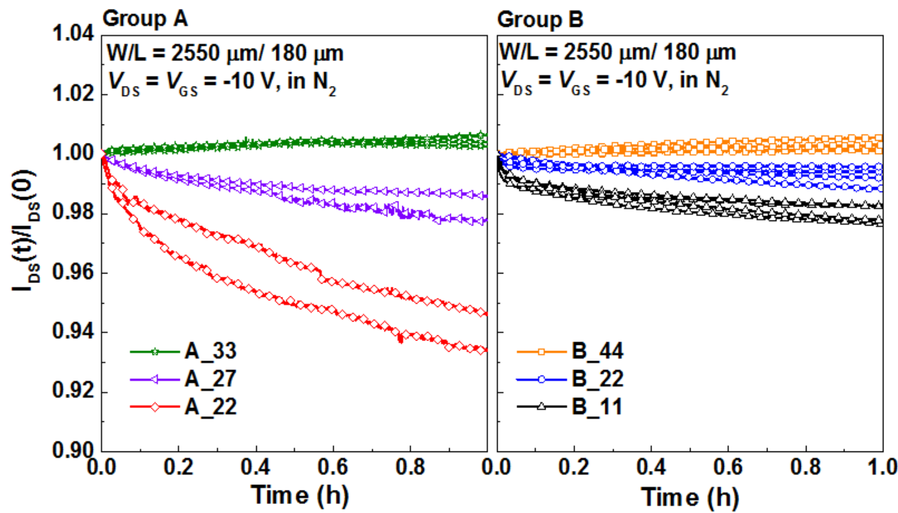

fig. S4. One-hour operational stability of μc-OTFTs. Operational stability in N_2 during 1 h continuous dc-bias stress at $V_{DS} = V_{GS}$ = -10 V for *μc*-OFETs of Group A and Group B.

Figure S4 shows the temporal evolution of the normalized $I_{DS}(t)$ measured during the on-state dc-bias stress test for 1 h on Group A and Group B devices; data are plotted from four devices for A_33, B_44, B_22, and B_11, and two for A_27 and A_22 *μc*-OTFTs, respectively. A_27 and A_22 were found to display a lower yield and larger device-to-device variation, presumably due to their high and unstable gate leakage current. After 1 h continuous dc-bias stress, the normalized I_{DS} of A_33 slightly increased to 1.008, while that of A_27 and A_22 dropped down to around 0.979 and 0.941, respectively. In Group B, B_44 devices displayed normalized I_{DS} increases of 1.002. During the same interval, the normalized I_{DS} dropped to 0.994 in B_22 and 0.981 in B_11 *μc*-OTFTs. In addition, A_33 *μc*-OTFTs exhibited higher operational stability than that of B_22 and B_11, which had similar or even thicker dielectric layers. These results demonstrate that the operational stability during bias stress tests can be controlled systematically by changing the thickness of the oxide gate dielectric layer (*20*).

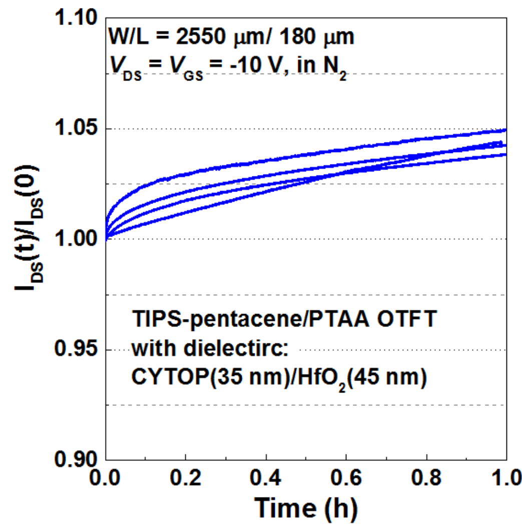

fig. S5. One-hour operational stability of μc-OTFTs using a CYTOP/HfO$_2$ dielectric. Operational stability in N_2 during 1 h continuous dc-bias stress at $V_{DS} = V_{GS}$ = -10 V for TIPS-pentacene/PTAA μc-OFETs using CYTOP(35 nm)/HfO$_2$(45 nm) as gate dielectric.

section S4. Long-term operational stability

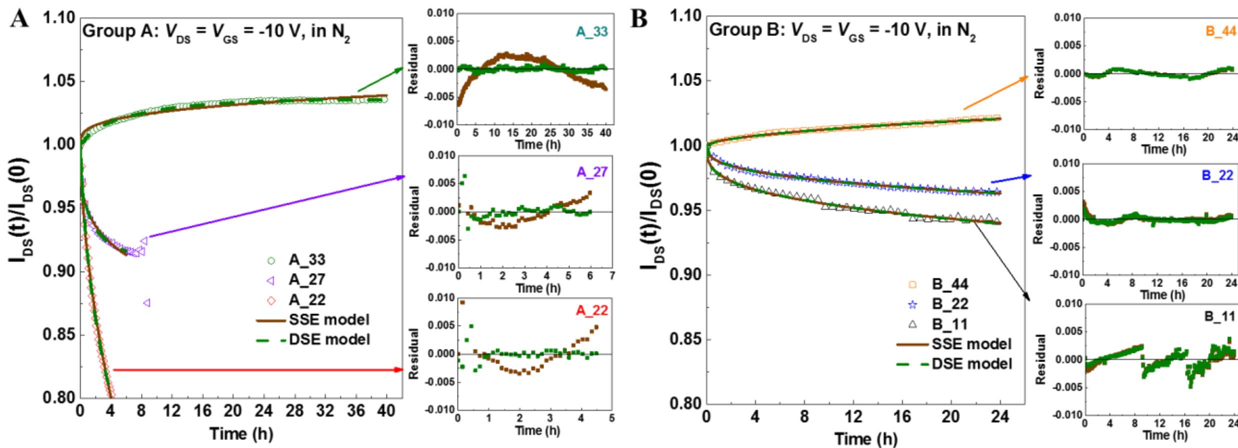

fig. S6. Long-term operational stability of μc-OTFTs. Long-term operational stability in N_2 during continuous dc-bias stress at $V_{DS} = V_{GS}$ = -10 V for μc-OTFTs of **(A)** Group A and (**B**) Group B, with the fitted curves fitted using single stretched-exponential (SSE) model and double stretched-exponential (DSE) model. The fitting residuals using two models are shown next to the main figures.

Figure S6 shows the long-term temporal evolution of the normalized $I_{DS}(t)$ for TIPS/PTAA μc-OTFTs in Group A and Group B. As discussed in the main text, A_33 displayed remarkable I_{DS} stability after 40 h bias stress. On the contrary, A_27 and A_22 showed poor long-term stability. On A_27 μc-OTFTs, the normalized I_{DS} dropped to 0.92 before the device failed after 8 h of continuous bias stress. On A_22 μc-OTFTs, the normalized I_{DS} dropped below 0.8 in 4 h prior to

failing. In contrast, fig. S6B displays the changes of normalized I_{DS} after 24 h for Group B devices (-2.2%, -3.6%, and -5.9 % for B_44, B_22, and B_11 μc-OTFTs, respectively), which were not found to fail. These results correlate to some extent with the quality of the dielectric layer as determined by leakage current measurements, furthermore, prove that the operational stability of devices can be engineered by controlling the thicknesses of gate dielectric layers.

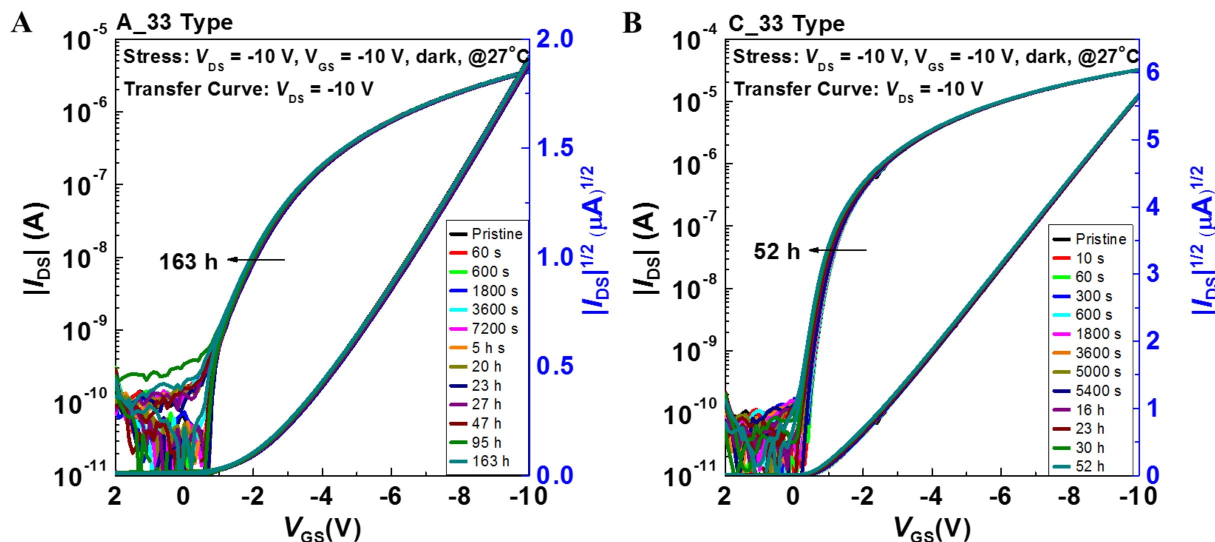

fig. S7. Transfer characteristics of μc-OTFTs during long-term operational stability tests. Transfer characteristics of **(A)** A_33 type μc-OTFTs and (**B**) C_33 type μc-OTFTs upon dc-bias stress at $V_{DS} = V_{GS} = -10$ V.

table S2. Summary of the device electrical parameters before and after stress tests.*

Sample No.	μ (cm² V⁻¹ s⁻¹)		V_{TH} (V)		|S| (V decade⁻¹)		Current on/off ratio	
	pristine	after stress**	pristine	after stress**	pristine	after stress**	pristine	after stress**
A_33	0.26	0.26	-2.69	-2.73	0.71	0.70	5.9×10^4	8.2×10^4
C_33	1.41	1.37	-1.12	-1.01	0.30	0.31	7.3×10^5	4.9×10^5

* The parameters are calculated from transfer curves in fig. S7.
** The stress time is 163 h for A_33 and 52 h for C_33.

In addition, we carried out independent long-term on-bias stress tests ($V_{DS} = V_{GS} = -10$ V) at room temperature (ca. 27 °C) on pristine A_33 and C_33 μc-OTFTs. Fig. S7 shows the transfer characteristics measured during these tests and reveals only very small changes. Table S2 provides a comparison of the electrical parameters (i.e. μ, V_{TH}, $|S|$, and current on/off ratio) which were derived from these transfer characteristics in fig. S7 before and after stress tests. After stress, the values of μ, V_{TH}, and $|S|$ are changed by less than 3 %.

section S5. Analytic models of bias stress effects

Bias stress effects on TFTs typically describes the V_{TH} shifts under dc-bias stress test due to diffusion-mediated charge trapping, which is modeled by a stretched-exponential formula (*9, 28, 29*)

$$\Delta V_{TH,1}(t) = \Delta V_{TH,1\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_1}\right)^{\beta_1}\right]\right\} \quad \text{(S1)}$$

where τ_1 is a characteristic decay time, and β_1 is the dispersion parameter ($0<\beta_1<1$) and $\Delta V_{TH,1\infty} = [V_{TH,1}(\infty) - V_{TH}(0)]$. We refer to this model as the single-stretched exponential (SSE) model.

As discussed in the main text, for μc-OTFTs with a bilayer dielectric, we need to account for two opposite bias stress effects, which are attributed to the simultaneous occurrence of charge trapping at dielectric-semiconductor interfaces (described by eq. S1) and a second attributed to the reorientation of dipoles present in the gate dielectric or to the injection of charge carriers at the gate, which can be modeled with the following expression (*28, 34*)

$$\Delta V_{TH,2}(t) = \Delta V_{TH,2\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_2}\right)^{\beta_2}\right]\right\} \quad \text{(S2)}$$

where τ_2 is characteristic decay time, and β_2 is the dispersion parameter ($0<\beta_2<1$) and $\Delta V_{TH,2\infty} = [V_{TH,2}(\infty) - V_{TH}(0)]$. We assume that $m = \Delta V_{TH,1\infty}/\Delta V_{TH,2\infty}$. Consequently, bias stress effects in μc-OTFTs in this work are expected to exhibit the following functional form

$$\Delta V_{TH}(t) = \Delta V_{TH,1\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_1}\right)^{\beta_1}\right]\right\} + \Delta V_{TH,2\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_2}\right)^{\beta_2}\right]\right\} \quad \text{(S3)}$$

This model will be referred to as the double stretched-exponential model (DSE) model.

Assuming μ and C_{ox} are constant and using the standard square-law transistor equations, the I_{DS} changes of SSE model and DSE model could be derived from eqs. S1 and S3, respectively, using the equations

$$\frac{I_{DS}(t)}{I_{DS}(0)} = 1 - \frac{\Delta V_{TH}(t)}{V_{GS} - V_{TH}(0)}, \text{ if } |V_G| \gg |V_D|, \text{ linear regime} \quad \text{(S4)}$$

$$\frac{I_{DS}(t)}{I_{DS}(0)} = \left[1 - \frac{\Delta V_{TH}(t)}{V_{GS} - V_{TH}(0)}\right]^2, \text{ saturation regime} \quad \text{(S5)}$$

In this work, eqs. S1 and S5 were adopted to fit the experimental data as shown in Fig. 2A and fig. S6, and eqs. S1 and S4 were used to fit the data in Fig. 2B for the long-term dc-bias stress study. However, we note that for A_33 and B_44 μc-OTFTs displaying an increasing trend of I_{DS} over time, the data of A_33 and B_44 was fitted using eq. S1 but without the negative sign in the exponential function. The values of τ_1 and β_1 derived from best fits of the SSE model to the experimental data are listed in table S3 and compared with several typical transistors in literature.

To compare the SSE and DSE models, the experimental data showing in Fig. 2A and fig. S6 were fitted with eqs. S3 and S5, while the data in Fig. 2B were fitted with eqs. S3 and S4. The parameters of the models derived from these fits are shown in table S4. Fig. S8 shows the V_{TH} shifts of Group A and Group B devices modeled using the DSE model (eq. S3) with the lifetime

parameters in table S4, which were obtained by fitting the data of $I_{DS}(t)/I_{DS}(0)$ under bias stress. The corresponding $\Delta V_{TH,1}(t)$ and $\Delta V_{TH,2}(t)$ from two opposite mechanisms for each sample are calculated using eqs. S1 and S2, respectively.

For the devices with TIPS/PTAA-CYTOP interfaces (e.g. devices in Group A and Group B, and the TIPS/PTAA μc-OTFTs with CYTOP single dielectric (*20*)), the influence of charge trapping effect at the semiconductor-dielectric interface should be similar. Therefore, using DSE model, the A_33, A_27, B_44, B_22, and B_11 devices show similar values of $\boldsymbol{\tau_1}$ and $\boldsymbol{\beta_1}$ (see table S4), which are comparable to $\boldsymbol{\tau_1}$ and $\boldsymbol{\beta_1}$ fitted from experimental data of TIPS/PTAA μc-OTFTs with CYTOP single gate dielectric using SSE model (table S3). In table S4, devices in Group A and Group B under bias stress in saturation regime also display comparable values of $\boldsymbol{\tau_2}$ and $\boldsymbol{\beta_2}$. In addition, devices with thicker dielectric had larger values of m in Group A and Group B, respectively, which supports the hypothesis that thicker metal-oxide layers lead to the stronger influence of the second effects described by the second term in eq. S3. In addition, the experimental data of ΔV_{TH} showing in Figs. 2C and D and Fig. 3A were fitted with eq. S3 and the fitted parameters are shown in tables S4 and S5, respectively.

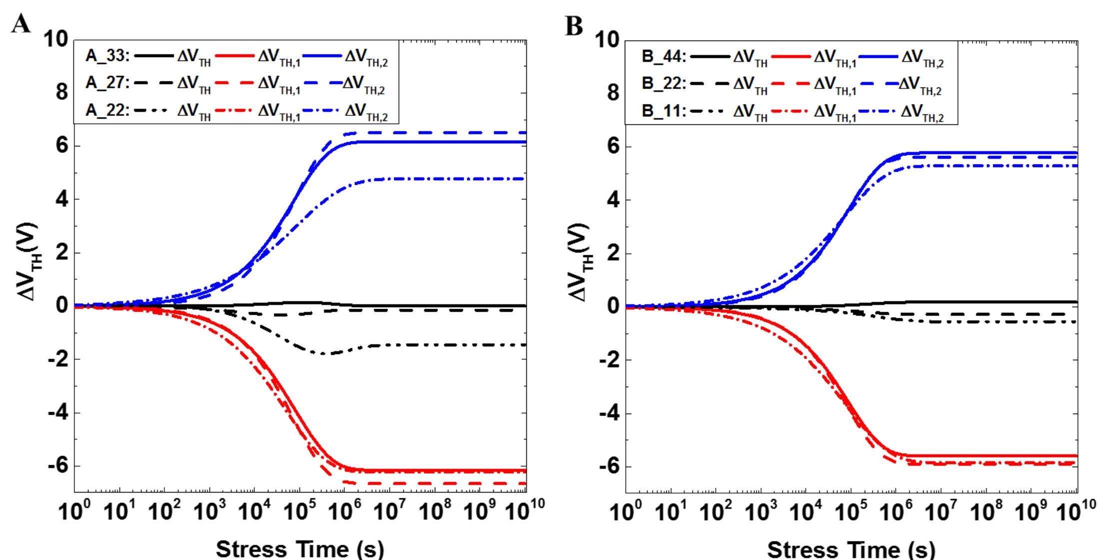

fig. S8. Simulation of ΔV_{TH} and the corresponding two opposite contributions of $\Delta V_{TH,1}$ and $\Delta V_{TH,2}$ of µc-OTFTs during dc-bias stress using the DSE model. The simulated ΔV_{TH} and the corresponding $\Delta V_{TH,1}$ and $\Delta V_{TH,2}$ using the DSE model and the lifetime parameters in table S4 for (**A**) A_33, A_27, and A_22 devices and (**B**) B_44, B_22, and B_11 devices under on-state bias stress ($V_{DS} = V_{GS} = -10$ V).

table S3. Summary of lifetime parameters of TFTs using the SSE model. The lifetime parameters of various types of TFTs obtained by fitting data shown in Figs. 2A and B and fig. S6 with eqs. S1, S4, and S5, and from the literature.

Semiconductor	Gate dielectric	Regime	$V_{GS}-V_{TH}(0)$ (V)	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1
TIPS/PTAA (this work)	A_33: CYTOP/NL (35/33 nm)	Saturation	-8.0	-11.84	2.50×10^{11}	0.302
		Linear	-8.0	-8.40	1.66×10^{10}	0.299
	A_27: CYTOP/NL (35/27.5 nm)	Saturation	-7.4	-3.92	7.76×10^{7}	0.296
	A_22: CYTOP/NL (35/22 nm)	Saturation	-7.0	-6.20	3.92×10^{5}	0.626
	B_44: CYTOP/Al_2O_3/NL (35/20/44 nm)	Saturation	-7.0	-2.24	4.62×10^{7}	0.548
	B_22: CYTOP/Al_2O_3/NL (35/20/22 nm)	Saturation	-7.2	-4.90	2.44×10^{9}	0.350
	B_11: CYTOP/Al_2O_3/NL (35/20/11 nm)	Saturation	-7.3	-7.52	4.77×10^{9}	0.322
TIPS/PTAA (*20*)	CYTOP	Saturation	-25	-5.25	6.07×10^{4}	0.527
PDIF-CN_2 (single-crystal) (*14*)	CYTOP/SiO_2	Linear	80	80	4.7×10^{9}	0.38
a-Si (*8*)	SiN_x	Linear	30	30	3.2×10^{6}	0.39

table S4. Summary of lifetime parameters of μc-OTFTs using the DSE model. The lifetime parameters obtained by fitting data shown in Figs. 2A and B and fig. S6 with eqs. S3, S4, and S5.

Sample No.	Regime	$V_{GS}-V_{TH}(0)$ (V)	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1	$\Delta V_{TH,2\infty}$ (V)	m	τ_2 (s)	β_2	Chi-Sqr.
A_33	Saturation	-8.0	-6.16	7.92×10^{4}	0.532	6.17	1.002	7.12×10^{4}	0.541	1.09×10^{-7}
	Linear	-8.0	-4.85	10.53×10^{4}	0.575	5.04	1.039	9.32×10^{5}	0.598	3.43×10^{-6}
A_27	Saturation	-7.4	-6.66	7.20×10^{4}	0.582	6.51	0.977	8.42×10^{4}	0.617	2.48×10^{-6}
A_22	Saturation	-7.0	-6.23	5.13×10^{4}	0.484	4.78	0.767	8.75×10^{4}	0.402	2.09×10^{-6}
B_44	Saturation	-7.0	-5.60	8.50×10^{4}	0.562	5.78	1.032	8.86×10^{4}	0.561	2.73×10^{-7}
B_22	Saturation	-7.2	-5.90	8.28×10^{4}	0.592	5.62	0.953	8.05×10^{4}	0.600	1.80×10^{-7}
B_11	Saturation	-7.3	-5.85	7.92×10^{4}	0.447	5.30	0.906	6.84×10^{4}	0.457	1.90×10^{-6}

table S5. Summary of μc-OTFTs lifetime parameters at different temperatures using the DSE model. The parameters are obtained by fitting data shown in Fig. 2C for on-state and off-state temperature stress to eq. S3.

DC-bias	Temperature	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1	$\Delta V_{TH,2\infty}$ (V)	m	τ_2 (s)	β_2	Chi-Sqr.
On-state	27 °C	-6.50	1.98×10^{4}	0.537	6.38	0.982	1.92×10^{4}	0.543	5.96×10^{-5}
	55 °C	-6.50	6.43×10^{4}	0.463	6.33	0.974	6.38×10^{4}	0.469	1.57×10^{-4}
	75 °C	-7.95	7.53×10^{2}	0.496	7.75	0.975	6.87×10^{2}	0.507	7.30×10^{-4}
Off-state	27 °C	-6.27	1.99×10^{3}	0.718	6.18	0.986	1.95×10^{3}	0.723	1.63×10^{-5}
	55 °C	-6.46	5.78×10^{2}	0.751	6.35	0.983	5.69×10^{2}	0.761	9.19×10^{-6}
	75 °C	-6.28	5.37×10^{2}	0.619	6.05	0.963	5.00×10^{2}	0.630	3.21×10^{-4}

table S6. Summary of lifetime parameters of μc-OTFTs extracted from V_{TH} shifts using the DSE model. The lifetime parameters obtained by fitting data shown in Fig. 3 with eq. S3.

Sample No.	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1	$\Delta V_{TH,2\infty}$ (V)	m	τ_2 (s)	β_2	Chi-Sqr.
A_33	-6.51	4.71×10^{4}	0.582	6.50	0.998	5.00×10^{4}	0.579	3.03×10^{-4}
C_33	-6.06	5.50×10^{4}	0.513	6.29	1.038	5.92×10^{4}	0.517	9.56×10^{-5}

section S6. Operational stability of short-channel devices

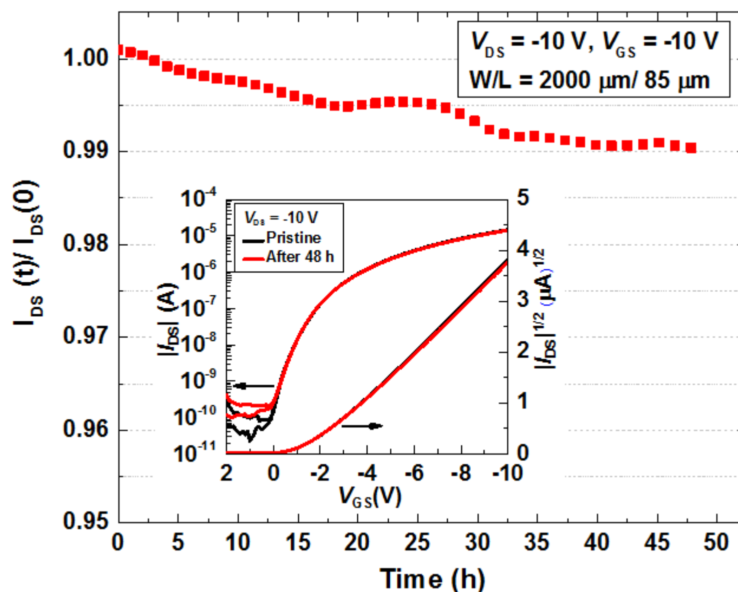

fig. S9. dc-bias stress test of short-channel μc-OTFTs. Operational stability in N_2 during 48 h continuous dc-bias stress at $V_{DS} = V_{GS}$ = -10 V for *μc*-OFETs of type A_33. The inset shows the transfer curves tested before and after dc-bias stress.

In an effort to explore the stability of devices with shorter channel lengths we fabricated OTFTs with channel lengths of 85 µm. In reducing the channel length, the contact resistance becomes increasingly relevant. Consequently, instead of using PFBT, we used a 10 nm MoO_x layer on the source and drain electrodes to reduce the contact resistance for these shorter channel OTFTs. It should be noted that in addition to different electrodes, the mask geometry (gate, source and drain electrodes areas) used for these devices is also different than the one used for devices with larger channel lengths.

Figure S9 shows I_{DS} changes monitored for 48 h of continuous dc-bias stress at $V_{GS} = V_{DS}$ = -10 V. This figure shows that shorter-channel devices exhibited less than 1 % change of $/I_{DS}/$, smaller than changes observed in larger channel devices. It should be noted that both, variations of the overall device geometry can be reasonably expected to affect the sign, magnitude and overall balance between compensating processes. However, as we have shown in fig. S4, variations of the nanolaminate layer thickness provides a knob to tune I_{DS} changes over time.

section S7. Temperature stability

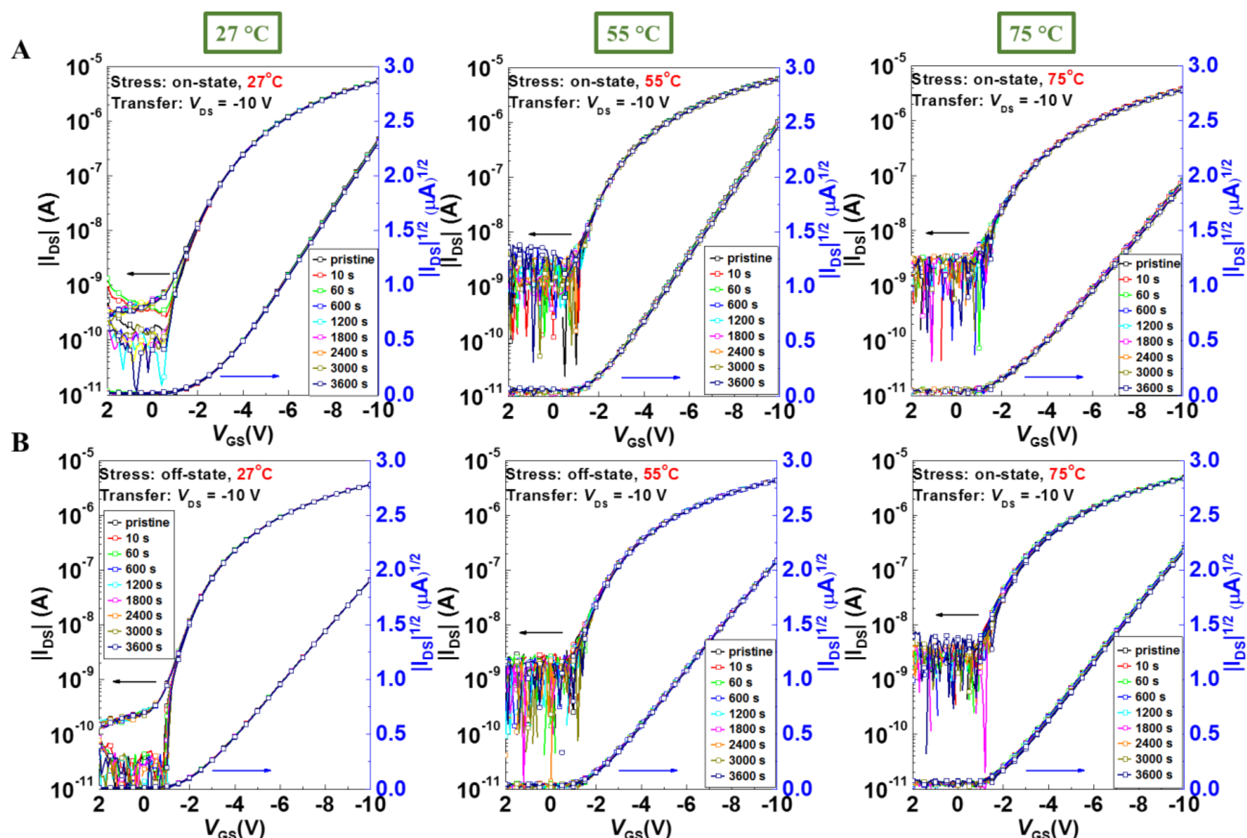

fig. S10. Transfer curves of μc-OTFTs during dc-bias stress at different temperatures. The transfer curves of as-fabricated A_33 devices after 1 h bias stress at (**A**) on-state ($V_{DS} = V_{GS} = -10$ V) and (**B**) off-state ($V_{DS} = 0$V, $V_{GS} = 10$ V) under different temperatures in dark.

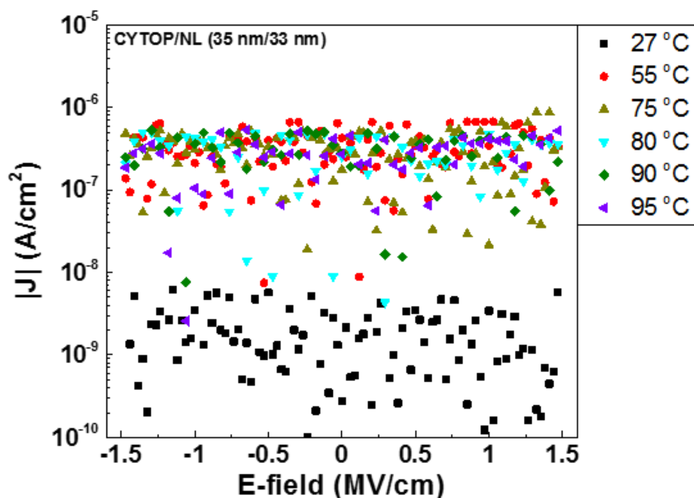

fig. S11. Current density–electric field (*J-E*) characteristics of dielectric layers for A_33 at different temperatures.

Figure S10 shows the transfer curves of as-fabricated A_33 devices under bias stress tests at different temperatures. The shifts of V_{TH} of each condition in Figs. 2C and D were calculated from these transfer curves. All of the devices display high operational stability at elevated temperatures. At high temperatures, the increase of the off current is attributed to an increase of gate leakage current, as shown in as shown in fig. S11.

section S8. Bias stress effects with different experimental procedures and device bias stress history

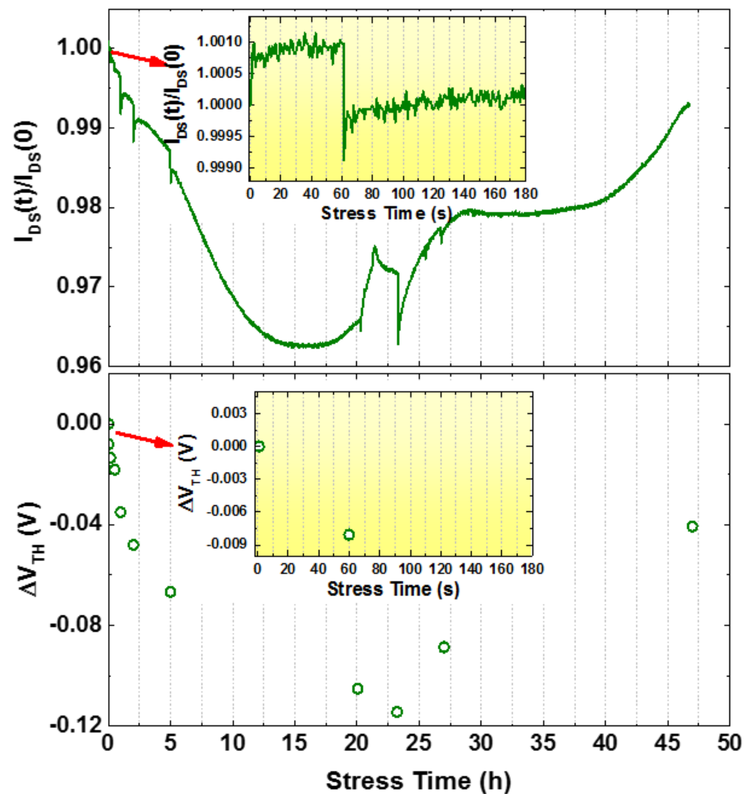

fig. S12. Temporal dynamic of I_{DS}, including interruptions to measure the transfer characteristics, during 47-hour dc-bias stress at $V_{DS} = V_{GS} = -10$ V at RT. (Top panel) The normalized $I_{DS}(t)$ for dc bias stress showing multiple interruptions to measure the transfer characteristics. (Bottom panel) The ΔV_{TH} values derived from the transfer characteristic measured after different stress times. The insets show the normalized $I_{DS}(t)$ for the first 180 s dc-bias stress including one interruption to measure the transfer characteristics at 60 s and the corresponding ΔV_{TH}.

Figure S12 illustrates the bias stress effects study on ΔV_{TH} under dc-bias stress tests at room temperature of pristine A_33 devices. The insets show the first 180 s dc-bias stress with one time interrupt for transfer characteristic measurement at 60 s. The $I_{DS}(t)$ showed increasing trend before and after the interrupt, respectively, except a small drop at the interrupt resulting in an overall decrease tendency. We believe that the transfer characteristic measurement at the interrupt of the continuous bias stress leads to different the temporal dynamic of $I_{DS}(t)$ from those measured during constant bias stress.

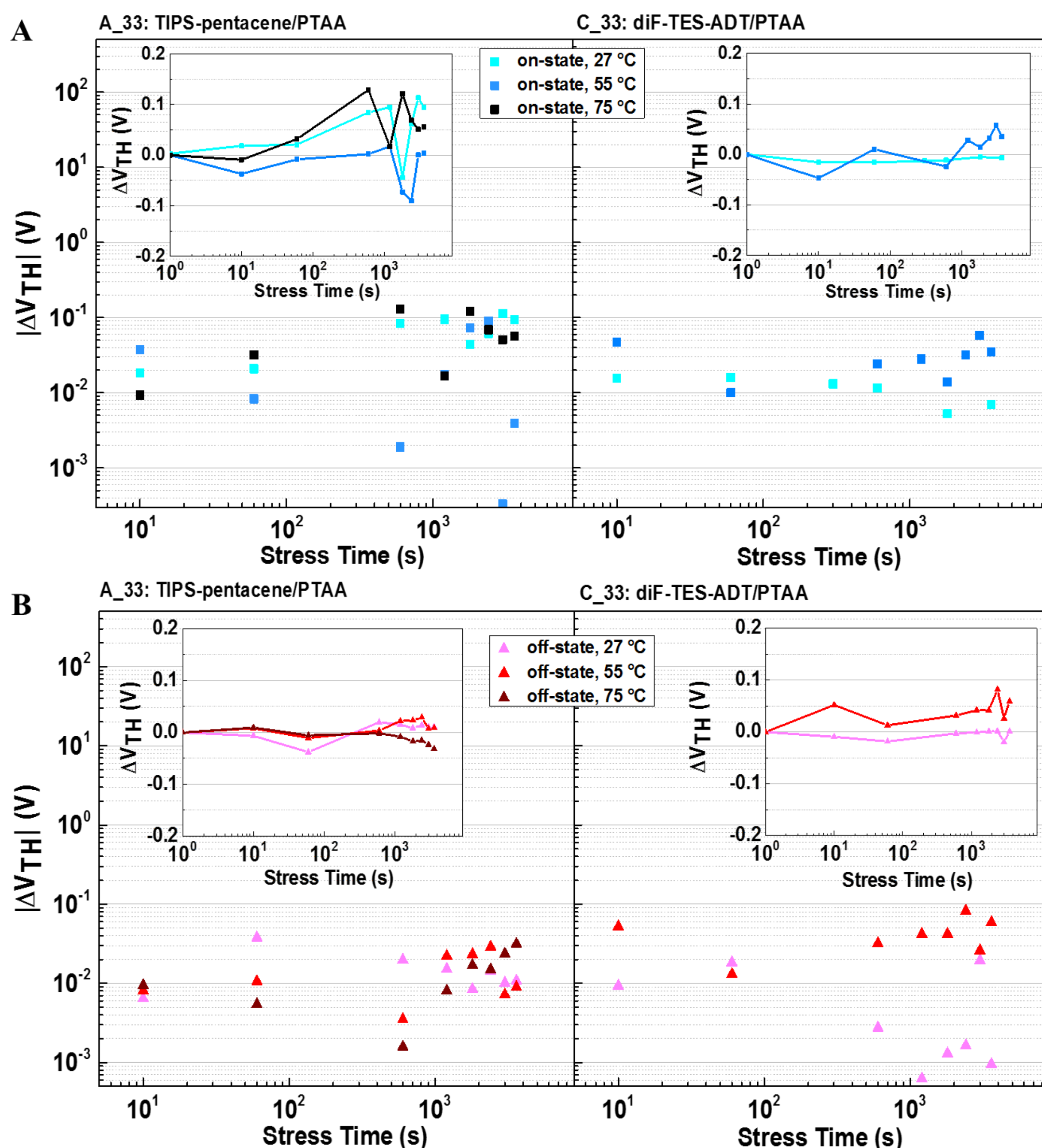

fig. S13. V_{TH} shifts of A_33 and C_33 devices that were tested after long-term operational and environmental stability tests. The $|\Delta V_{TH}|$ values after dc-bias stress of stressed A_33 and C_33 devices (**A**) at on-state and (**B**) at off-state bias stress tests under different temperatures in dark. The insets show the corresponding ΔV_{TH} values for each condition.

Figure S13 shows the $|\Delta V_{TH}|$ and ΔV_{TH} under on-state and off-state bias stress tests at different temperature in dark of A_33 and C_33 devices, which had been stressed for long-term operational and environmental stability tests. The trends of $|\Delta V_{TH}|$ on these devices are not as obvious as those on pristine devices shown in Figs. 2C and D in the main text. However, the overall V_{TH} shifts are still very small although with no clear functional dependence with respect to the temperature.