Supporting Information

Lithography-based fabrication of nanopore arrays in freestanding SiN and graphene membranes

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1. Fabrication of SiN membrane supports with a 1x1um square

The silicon-nitride chips are fabricated using similar protocol as published in Janssen et al[1] to obtain 20 nm thick freestanding SiN membranes of 40 by 40 µm wide. The top layers on the substrate are removed to create a flat SiN surface extending over the chip. Subsequently squares are etched in the SiN membrane which defined the area of freestanding graphene, in a similar procedure to making the nanopore arrays in SiN (see SI section 2). For this, the chips are spincoated with a 100 nm thick layer of poly(methyl methacrylate) (PMMA, 495K) electron sensitive resist (MicroChem Corp). Then, the layer is patterned by exposing the resist with a 100 keV electron bundle from the electron-beam pattern generator (EBPG5200, Raith). Depending on the experiment, either a single square or an array of squares is patterned. For the dose test, we patterned an array of squares (1 by 1 µm). After exposure, the PMMA is developed in a 1:3 mixture of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) for 1 min. The pattern is transferred into the SiN by reactive ion etching (1 min 40 sec, 50 W, 50 sccm CHF3 and 2.5 sccm O2, 8.5 µbar, Leybold). The remaining resist is stripped using hot acetone (50°C) for 20 mins. For the nanopore experiments, a single 100 by 100 nm wide square is etched to define the freestanding graphene area.

2. TEM images of graphene nanopore arrays

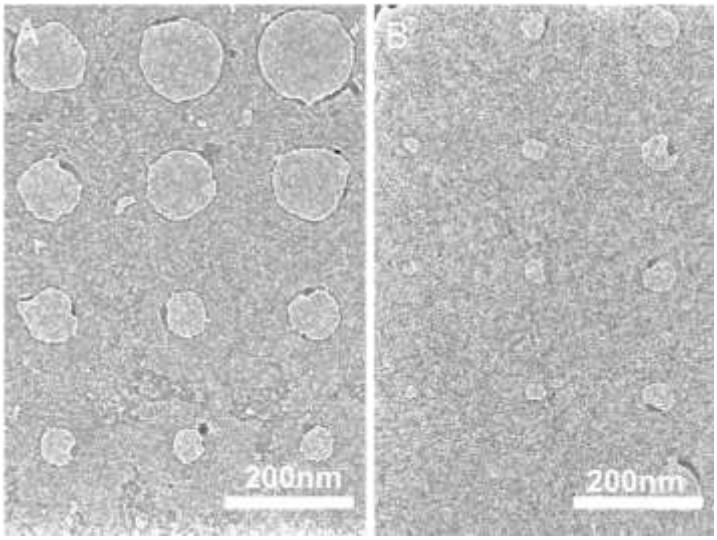

Figure S1. Example TEM images of a nanopore arrays fabricated using RIE on graphene. The electron dose was varied to produce different sized holes. A) Graphene nanopore array with diameters ranging from 140 nm to 67 nm. B) Graphene nanopore array with diameters ranging from 62 nm to 17 nm.

3. TEM images of SiN nanopore arrays

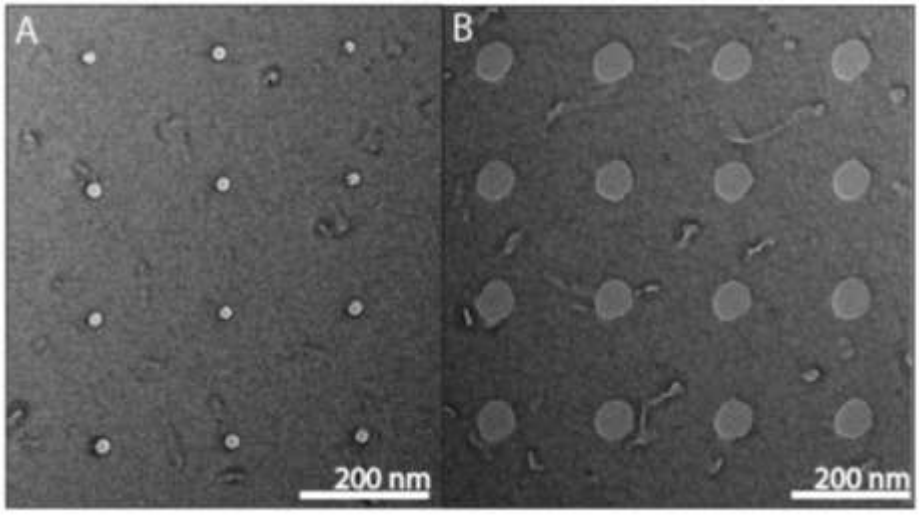

Figure S2. Example TEM images of a nanopore arrays fabricated using RIE in SiN. (A) Nanopore array with an average diameter of 16±2 nm. (B) Nanopore array with an average diameter of 62±2 nm

4. Noise spectrum of RIE fabricated graphene nanopore

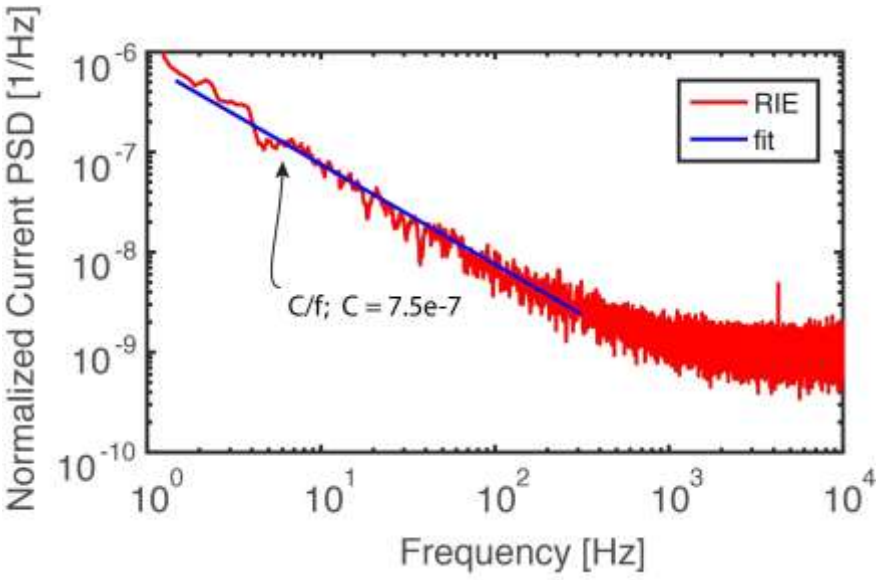

Figure S3. Normalized current power spectral density (PSD) (S_I/I^2) of a 18 nm graphene nanopore fabricated using RIE using a dose of 88fC and a fit to flicker noise contribution ($S_I/I^2 = \mathrm{C/f},$), where f is the frequency and C is low-frequency noise amplitude. The fit shows a value for the low-frequency noise amplitude of $7.5 * 10^{-7}$, which is similar to values obtained from graphene nanopores drilled with the TEM $(\sim 10^{-6})^2$. The PSDs are smoothened using a 20 point moving average.

5. Noise spectrum of RIE fabricated SiN nanopore

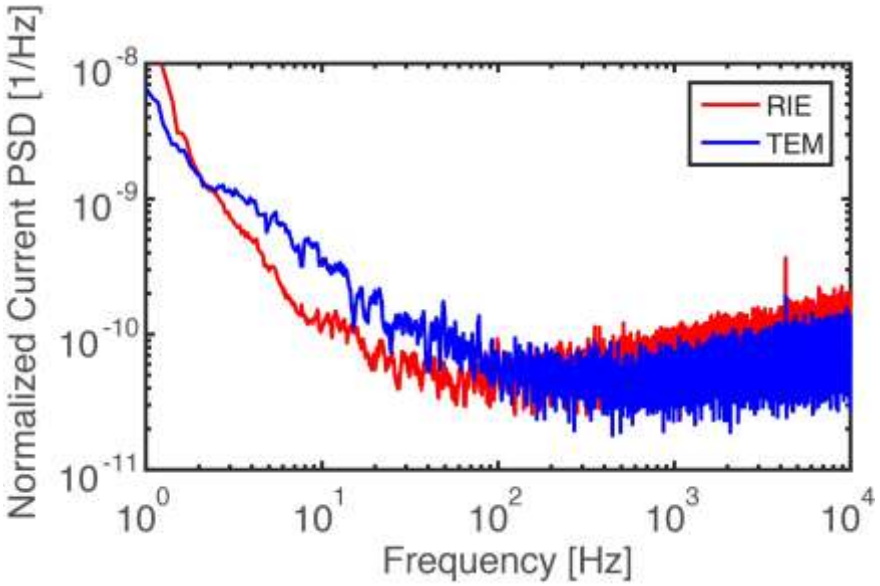

Figure S4. Normalized current power spectral density (PSD) (S_I/I^2) of a 25 nm SiN nanopore fabricated using RIE with a dose of 15fC and a 20 nm nanopore created using TEM drilling. The low frequency component of the noise (< 1kHz) is comparable between TEM drilled and RIE fabricated nanopores. The PSDs are smoothened using a 20-point moving average.

References

1. Janssen, X. J.; Jonsson, M. P.; Plesa, C.; Soni, G. V.; Dekker, C.; Dekker, N. H. *Nanotechnology* **2012,** 23, (47), 475302.
2. Heerema, S. J.; Schneider, G. F.; Rozemuller, M.; Vicarelli, L.; Zandbergen, H. W.; Dekker, C. *Nanotechnology* **2015,** 26, (7), 074001.