Conductively Coupled Flexible Silicon Electronic Systems for Chronic Neural Electrophysiology

Jinghua Li[a,b,1], Enming Song[a,c,1], Chia-Han Chiang[d], Ki Jun Yu[e], Jahyun Koo[a,b], Haina Du[a], Yishan Zhong[a], Mackenna Hill[d], Charles Wang[d], Jize Zhang[a], Yisong Chen[a], Limei Tian[f], Yiding Zhong[a], Guanhua Fang[a], Jonathan Viventi[d], John A. Rogers[a,b,c,g,h,i,j,k,l,m,2]

[a] Department of Materials Science and Engineering, Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana–Champaign, Illinois 61801, United States

[b] Departments of Materials Science and Engineering, Northwestern University, Evanston, IL 60208, United States

[c] Center for Bio-Integrated Electronics, Northwestern University, Evanston, IL 60208, United States

[d] Department of Biomedical Engineering, Duke University, Durham, North Carolina 27708, United States

[e] Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, Republic of Korea

[f] Beckman Institute for Advanced Science and Technology, University of Illinois at Urbana–Champaign, Urbana, Illinois 61801, United States

[g] Department of Biomedical Engineering, Northwestern University, Evanston, IL 60208, United States

[h] Department of Chemistry, Northwestern University, Evanston, IL 60208, United States

[i] Department of Mechanical Engineering, Northwestern University, Evanston, IL 60208, United States

[j] Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL 60208, United States

[k] Simpson Querrey Institute, Northwestern University, Evanston, IL 60208, United States

[l] Feinberg School of Medicine, Northwestern University, Evanston, IL 60208, United States

[m] Department of Neurological Surgery, Northwestern University, Evanston, IL 60208, United States

[1] These authors contributed equally to this work.

[2] Corresponding author. E-mail: jrogers@northwestern.edu (J.A.R)

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Supplementary Information

Supplementary Note 1

Supplementary Figure Legends

Supplementary Figure S1-S19

Supplementary Note 1: Step-by-step process flow to fabricate sealed and conductive coupled flexible active arrays.

Wafer back grinding

1. Start with SOI wafer (200 nm device Si, 1 μm BOX layer, 500 μm handle wafer, Soitec);
2. Grind handle wafer to 200 μm by Syagrus Systems;
3. Cut the wafer into chips of device size;

P-doping

4. RCA cleaning of SOI wafers;
5. Dry thermal oxidation to form 200 nm SiO_2 at 1150 °C;
6. Photolithography to define sensing pad doping area using photoresist (PR) (AZ 5214E);
7. RIE to dry etch SiO_2, (a) 50 mTorr of CF_4/O_2 (40/1.2 sccm), with RF power of 100 W for 5min, (b) gentle O_2 plasma, 50 mTorr, 20 sccm of O_2, with RF power of 100 W for 20 s;
8. BOE (10:1) wet etch SiO_2 for 5 min;
9. PR strip by acetone, isopropanol and blow dry;
10. RCA cleaning;
11. Dope sensing pad area with diffusive boron source at 1000 °C for 15 min;

12. Wet etch SiO_2 doping mask using 49% HF for 20 s; and DI rinse;
13. RCA cleaning;

N-doping

14. Deposit 400 nm PECVD SiO_2 as diffusion mask;
15. Photolithography to define S/D doping area using photoresist (PR) (AZ 5214E);
16. RIE to dry etch SiO_2, (a) 50 mTorr of CF_4/O_2 (40/1.2 sccm), with RF power of 100 W for 15 min, (b) gentle O_2 plasma, 50 mTorr, 20 sccm of O_2, with RF power of 100 W for 20 s;
17. BOE (10:1) wet etch SiO_2 for 5 min;
18. PR strip by acetone, isopropanol and blow dry;
19. RCA cleaning;
20. Dope S/D area with diffusive phosphorus source at 1000 °C for 7 min;
21. Wet etch SiO_2 doping mask using 49% HF for 20 s; and DI rinse;
22. RCA cleaning;

Si isolation

23. Photolithography to define Si isolation area using PR (AZ 5214E);
24. RIE to dry etch Si (50 mTorr, 40 sccm of SF_6, with RF power of 100 W for 1 min);
25. PR stripe by acetone, IPA and blow dry;

Gate stack deposition

26. RCA cleaning;
27. Dry thermal oxidation to form 50 nm SiO_2 at 1150 °C for 15 min;
28. Deposit 13 nm (130 cycles) Al_2O_3 at 80 °C using an Atomic Layer Deposition (ALD) system;

Via 0

29. Photolithography to define S/D and sensing pad opening via using PR (AZ 5214E);
30. Gentle O2 plasma using RIE (50 mTorr, 20 sccm of O_2, with RF power of 100 W for 20 s);
31. BOE (6:1) to etch gate dielectric for 2 min;
32. PR stripe by acetone soaking, IPA and blow dry;

Metal 1

33. Deposit Cr/Au, 10/300 nm with an electron-beam evaporator;
34. Photolithography to define metal 1 using PR (AZ 5214E);
35. Au, Cr wet etching using Au, Cr etchant respectively;
36. PR stripe by acetone, IPA and blow dry;
37. Measure test transistors;

Interlayer PI 2545

38. Clean samples using acetone, IPA, DI, and blow dry;
39. Dehydration: bake samples at 110 °C for 5 min;
40. Spin coat PI adhesion promoter (VM 652) using 500 rpm 5s, hold 20s, 3000 rpm 30s; soft bake at 110 °C for 1 min;
41. PI coating: spin coat PI 2545 precursor at 4000 rpm for 30 s; soft bake at 110 °C for 2 min and 150 °C 5 min; cure at 250 °C for 70 min;

Via 1

42. Photolithography to define via 1 using PR (AZ P4620);

43. RIE to etch via 1 (200 mTorr, 20 sccm O_2, with RF power of 150 W for 900s);
44. Check microscope and resistance to make sure via is open;
45. PR stripe by acetone, IPA, and blow dry;

Metal 2

46. Deposit Cr/Au, 10/500 nm with an e-beam evaporator;
47. Photolithography to define metal 2 using PR (AZ 5214E);
48. Au, Cr wet etching using Au, Cr etchant respectively
49. PR stripe by acetone, IPA and blow dry;
50. Measure test transistors;

PI substrate 2545

51. Clean samples using acetone, IPA, DI, and blow dry;
52. Dehydration: bake samples at 110 °C for 5 min;
53. Spin coat VM 652 using 500 rpm 5s, hold 20s, 3000 rpm 30s; soft bake at 110 °C for 1 min;
54. PI coating: spin coat PI 2545 precursor at 3000 rpm for 30 s; soft bake at 110 °C for 2 min and 150 °C for 6 min; cure at 250 °C for 70 min;

Pre-conditioning before bonding

55. Deposit 20 nm Al_2O_3 at 150 °C to the devices' PI side using ALD;
56. Deposit Ti/SiO_2 5/50 nm to the devices' PI side with an electron-beam evaporator;

Bonding

57. Bond devices to 13-μm kapton films (coated with Ti/SiO_2 5/20 nm) using an adhesive (Kwik-Sil, World Precision Instruments).

Si wafer removal

58. Scratch off back contamination until the contamination on the back is gone;
59. Si back RIE etching (50 mTorr of SF_6/O_2, 40/3 sccm, with RF power of 100 W. Do 6 runs of 30 min;
60. Deep RIE to continue etching back the devices, until all the back Si is etched;

Via 2

61. Photolithography to define small regions on t-SiO2 aligned to the p^{++}-Si islands using PR (AZ 5214E);
62. RIE to dry etch SiO_2, (a) 50 mTorr of CF_4/O_2 (40/1.2 sccm), with RF power 100 W for 15 min, (b) gentle O_2 plasma, 50 mTorr, 20 sccm of O_2, with RF power 100 W;
63. BOE (6:1) wet etch SiO_2 for 11 min;
64. PR strip by acetone, IPA and blow dry;

Metal 3

65. Deposit Cr/Au, 10/300 nm with a thermal evaporator;
66. Photolithography to define metal 3 using PR (AZ 5214E);
67. Au, Cr wet etching using Au, Cr etchant respectively
68. PR strip by acetone, IPA and blow dry;

Hand cutting

69. Razor blade cut to define the device outline profile;

70. Peel off devices gently from handling substrates;
71. Stick the stiffener onto the device ZIF side under microscope; devices are then ready to be tested with the DAQ.

Supplementary Figure Legends

Figure S1. Dopant concentration measured by secondary ion mass spectrometry (SIMS) for p^{++}-Si (A) and n^{++}-Si (B) as biofluid barriers.

Figure S2. A: Schematic illustration of the structure of an Mg-based passive device used in soak tests. B: Top view showing the exposed Si barrier layer.

Figure S3. A-B: Change in thickness of a nanomembrane of Si at different doping levels as a function of immersion time in PBS at 37 °C and 70 °C. C: Dissolution rate of p^{++}-Si (concentration: 10^{20} atoms/cm^3) as a function of 1/T.

Figure S4. Statistics of lifetimes of Mg test devices encapsulated by p^{++}-Si at 70 and 96 °C, p^{++}-Si (170 nm) coated with 5 nm Ti/ 200 nm Pt at 70 and 96 °C, and n^{++}-Si (170 nm) at 70 and 96 °C.

Figure S5. Soak tests of p^{++}-Si as a barrier layer for arrays of passive electrodes. A: Schematic illustration passive electrode arrays encapsulated with p^{++}-Si (170 nm). B: Display of lifetimes of 13 test devices.

Figure S6. Optical image, schematic illustration and photograph of an n-MOSFET (channel length: L_{eff} = 16 μm, width: 400 μm) with p^{++}-Si as an electrical interface (p^{++}-Si via) through the t-SiO_2, of the type used in soak tests.

Figure S7. Results from soak tests of an n-MOSFET with a p^{++}-Si via in PBS solution at 65 and 70°C.

Figure S8. Results from soak tests of an n-MOSFET with p^{++}-Si and Au (300 nm) on the side in contact with PBS at 60, 70 and 90°C.

Figure S9. Schematic illustration of the design of a 64 channel multiplexed device, showing the entire device (A) and a unit cell (B).

Figure S10. Procedures for fabricating flexible, sealed and conductively coupled active matrix systems.

Figure S11. Images of active multiplexed matrix devices after six key fabrication steps. A: Isolation of device Si (p^{++}-Si as encapsulation layer and sensing pad, and n^{++}-Si as backplane transistor) above the buried oxide, t-SiO_2. B. Metal 1 for source, drain and gate (connecting to p^{++}-Si), and row selects for multiplexing. C: Metal 2 for interconnection with source and drain, and column selects for signal output. D: Configuration after the removal of Si handle-wafer, with t-SiO_2 on the top. E: Via opening on t-SiO_2 to expose p^{++}-Si underneath. F: Metal 3 for sensing pads on the tissue-contacting side.

Figure S12. Schematic illustration of the cross-section of the sealed and conductively coupled active sensing matrix.

Figure S13. Statistics of on/off ratio and subthreshold swing of test transistors from 10 different samples.

Figure S14. Photographs of an active matrix system before (A) and after (B) the application of a Kapton stiffener, and after insertion into an adaptor PCB board through a ZIF connector (C-D).

Figure S15. Schematic illustration of the data acquisition system for in vitro assessment.

Figure S16. Cumulative leakage current of the 64-channel multiplexed arrays over time.

Figure S17. Photograph of Mg electrodes with sealed structure in flexible form for immersion test in PBS at 37 °C.

Figure S18. Photograph of a stimulation electrode system in flexible form with an opening of 3 × 3 mm^2 to p^{++}-Si through t-SiO_2.

Figure S19. Sequential images of a Au thin film electrode during simulation with a voltage of 2V showing that failure occurs after 6 h.

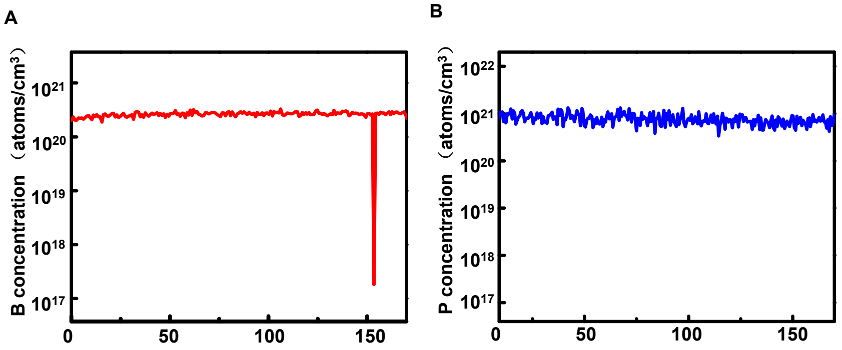

A
B concentration （atoms/cm^3）
10^{21}
10^{20}
10^{19}
10^{18}
10^{17}
0
50
100
150
B
P concentration （atoms/cm^3）
10^{22}
10^{21}
10^{20}
10^{19}
10^{18}
10^{17}
0
50
100
150

Figure S1

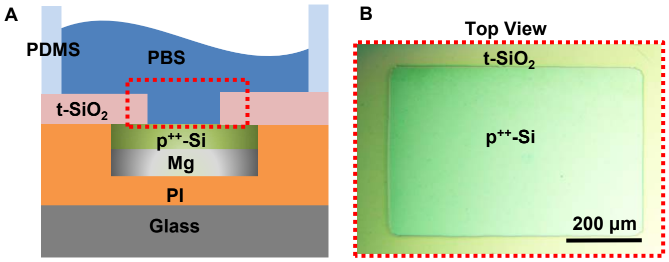


Figure S2

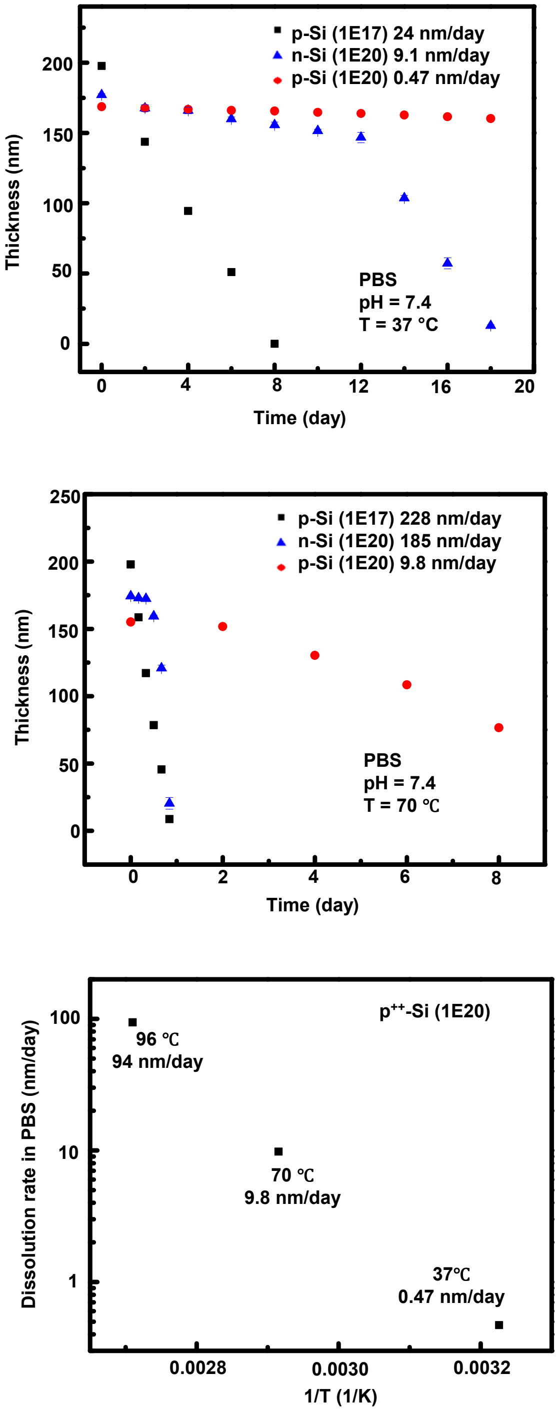

p-Si (1E17) 24 nm/day
n-Si (1E20) 9.1 nm/day
p-Si (1E20) 0.47 nm/day
Thickness (nm)
200
150
100
50
0
PBS
pH = 7.4
T = 37 °C
0
4
8
12
16
20
Time (day)
250
p-Si (1E17) 228 nm/day
n-Si (1E20) 185 nm/day
p-Si (1E20) 9.8 nm/day
Thickness (nm)
200
150
100
50
0
PBS
pH = 7.4
T = 70 ℃
0
2
4
6
8
Time (day)
p++-Si (1E20)
Dissolution rate in PBS (nm/day)
100
10
1
96 ℃
94 nm/day
70 ℃
9.8 nm/day
37℃
0.47 nm/day
0.0028
0.0030
0.0032
1/T (1/K)

Figure S3

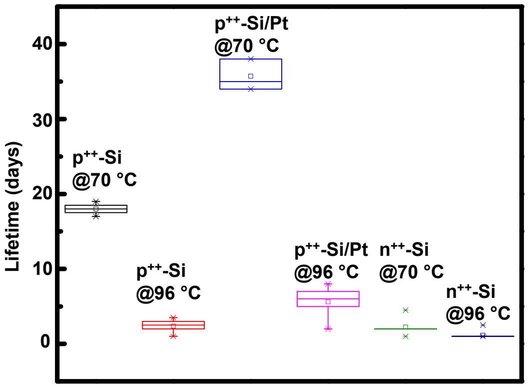

Lifetime (days)
0
10
20
30
40
p++-Si/Pt
@70 °C
p++-Si
@70 °C
p++-Si
@96 °C
p++-Si/Pt
@96 °C
n++-Si
@70 °C
n++-Si
@96 °C

Figure S4

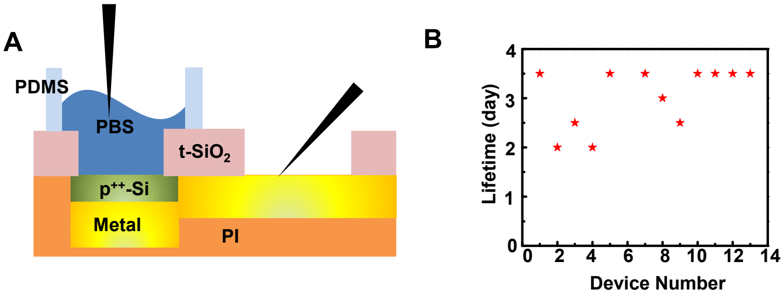

A
PDMS
PBS
t-SiO$_2$
p^{++}-Si
Metal
PI
B
Lifetime (day)
0
1
2
3
4
0
2
4
6
8
10
12
14
Device Number

Figure S5

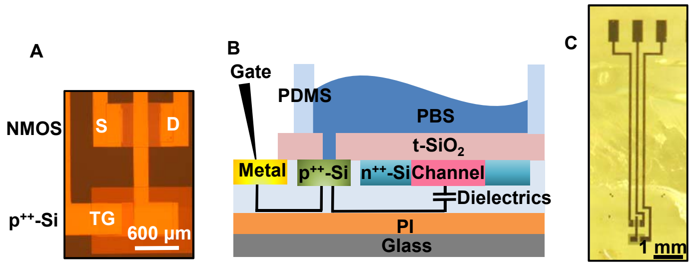
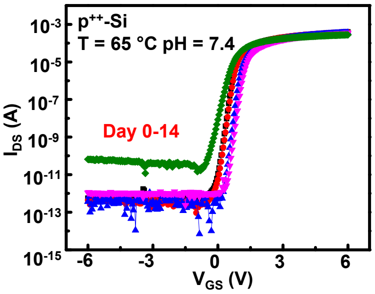

A
NMOS
S
D
p++-Si
TG
600 µm
B
Gate
PDMS
PBS
t-SiO2
Metal
p++-Si
n++-Si
Channel
Dielectrics
PI
Glass
C
1 mm

Figure S6


p++-Si
T = 65 °C pH = 7.4
Day 0-14
10-3
10-5
10-7
10-9
10-11
10-13
10-15
IDS (A)
-6
-3
0
3
6
VGS (V)

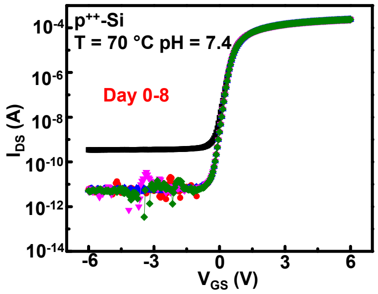

p++-Si
T = 70 °C pH = 7.4
Day 0-8
10-4
10-6
10-8
10-10
10-12
10-14
IDS (A)
-6
-3
0
3
6
VGS (V)

Figure S7

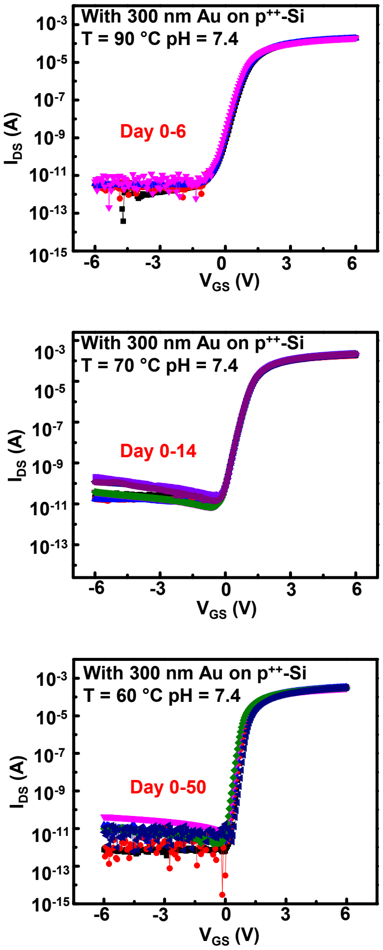

With 300 nm Au on p++-Si
T = 90 °C pH = 7.4
Day 0-6
I_DS (A)
10^-3
10^-5
10^-7
10^-9
10^-11
10^-13
10^-15
-6
-3
0
3
6
V_GS (V)
With 300 nm Au on p++-Si
T = 70 °C pH = 7.4
Day 0-14
I_DS (A)
10^-3
10^-5
10^-7
10^-9
10^-11
10^-13
-6
-3
0
3
6
V_GS (V)
With 300 nm Au on p++-Si
T = 60 °C pH = 7.4
Day 0-50
I_DS (A)
10^-3
10^-5
10^-7
10^-9
10^-11
10^-13
10^-15
-6
-3
0
3
6
V_GS (V)

Figure S8

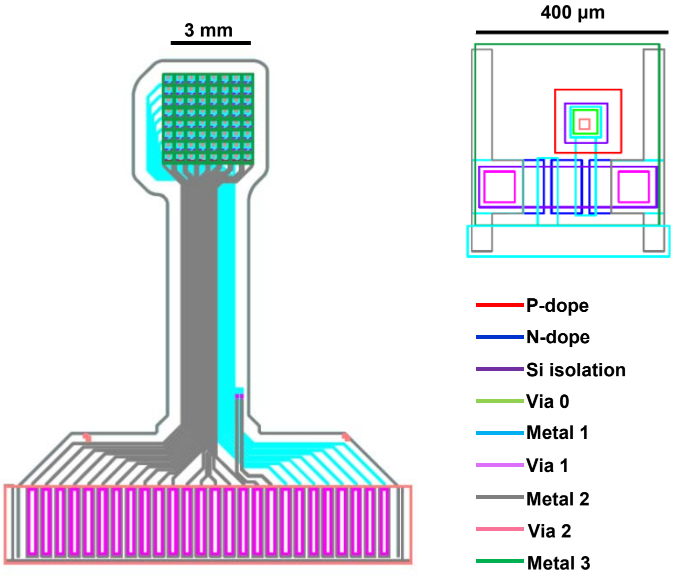
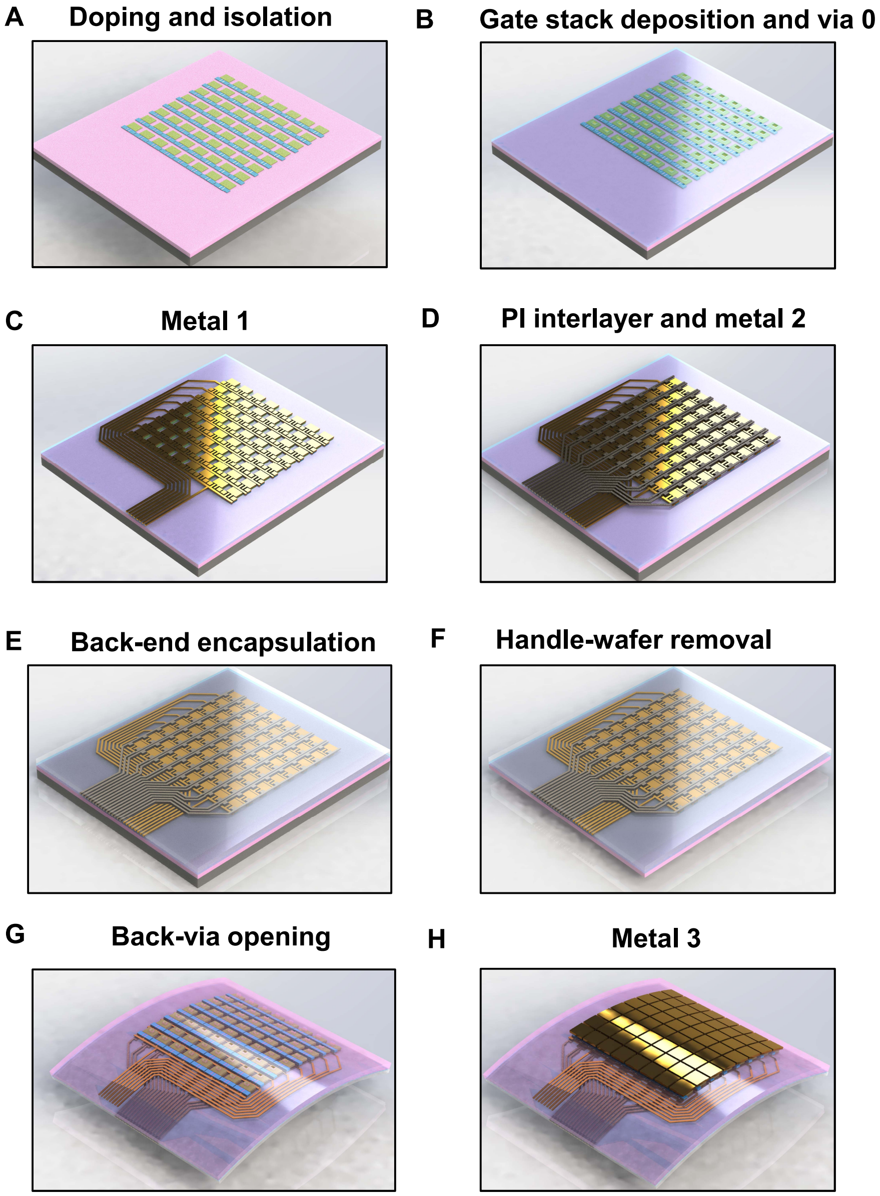

3 mm
400 µm
P-dope
N-dope
Si isolation
Via 0
Metal 1
Via 1
Metal 2
Via 2
Metal 3

Figure S9



A Doping and isolation

B Gate stack deposition and via 0

C Metal 1

D PI interlayer and metal 2

E Back-end encapsulation

F Handle-wafer removal

G Back-via opening

H Metal 3

Figure S10

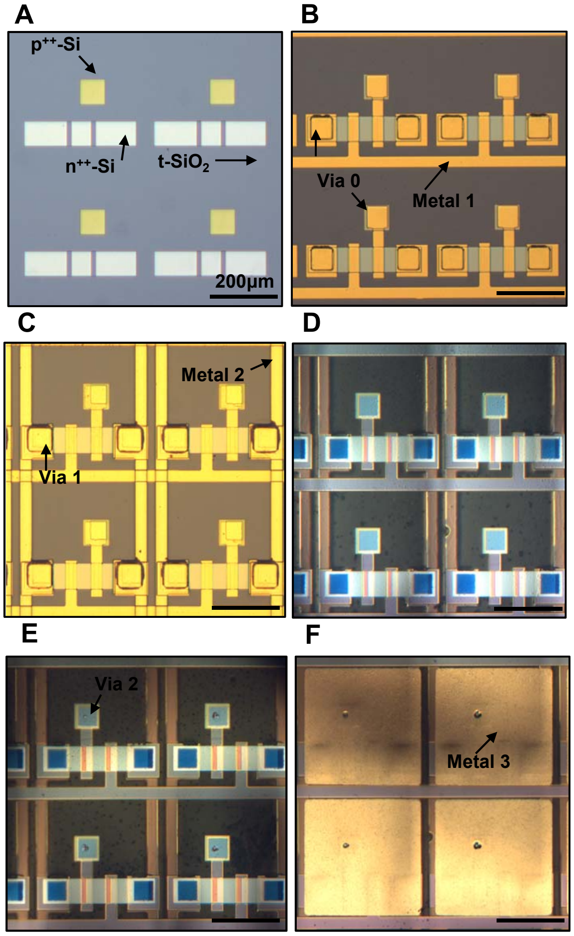

A
p++-Si
n++-Si
t-SiO2
200μm
B
Via 0
Metal 1
C
Metal 2
Via 1
D
E
Via 2
F
Metal 3

Figure S11


Metal 3 (300 nm)
Via 2
T-SiO$_2$ (1 μm)
Si (60 nm)
T-SiO$_2$ (50 nm)
Al$_2$O$_3$ (13 nm)
Via 0
Metal 1 (300 nm)
Via 1
PI (1.6 μm)
Metal 2 (500 nm)
PI (2 μm)
Al$_2$O$_3$ (20 nm)
Kwik Sil (20 μm)
Al$_2$O$_3$ (20 nm)
Kapton film (13 μm)

Figure S12

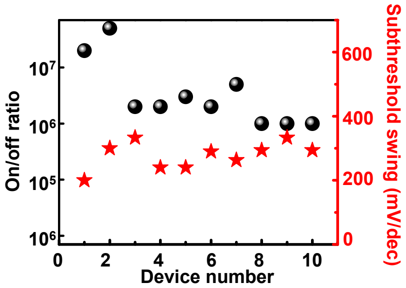

10^7
10^6
10^5
10^6
On/off ratio
0
2
4
6
8
10
Device number
600
400
200
0
Subthreshold swing (mV/dec)

Figure S13

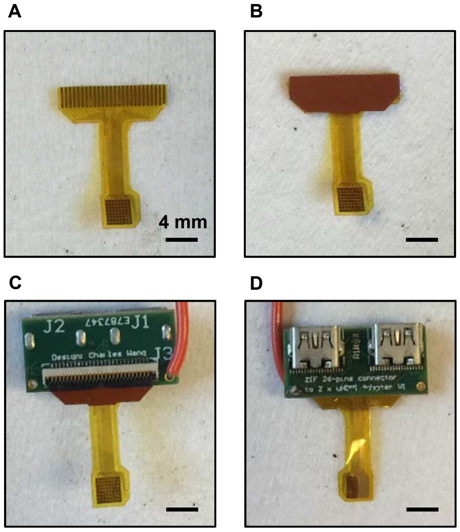

A
B
4 mm
C
J2
E787347
J1
Design: Charles Wang
J3
D
ZIF 26-pins connector

Figure S14

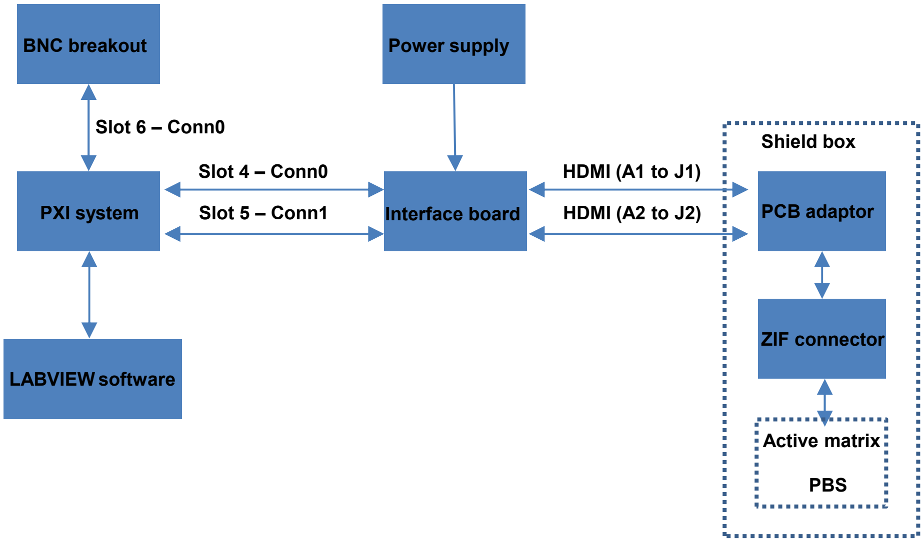

BNC breakout
Power supply
Slot 6 – Conn0
Shield box
Slot 4 – Conn0
HDMI (A1 to J1)
PXI system
Slot 5 – Conn1
Interface board
HDMI (A2 to J2)
PCB adaptor
ZIF connector
LABVIEW software
Active matrix
PBS

Figure S15

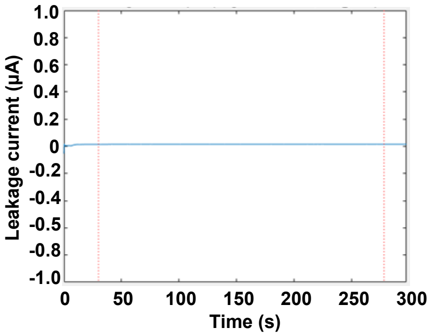

1.0
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.5
-0.8
-1.0
Leakage current (µA)
0
50
100
150
200
250
300
Time (s)

Figure S16

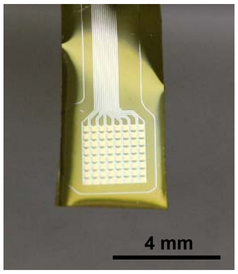


Figure S17

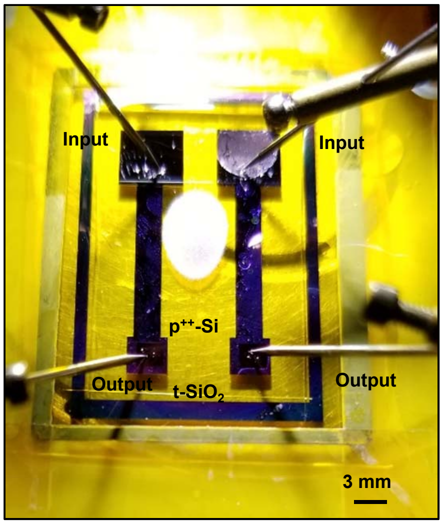
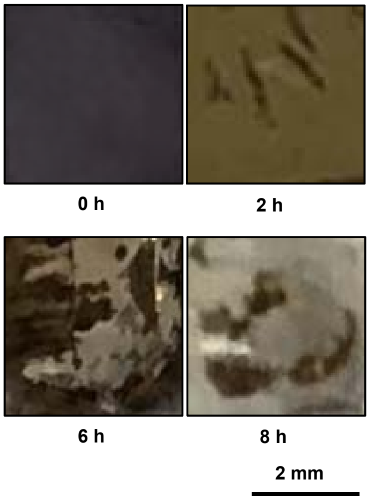


Figure S18


0 h

2 h

6 h

8 h

Figure S19