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Supplementary Materials for

Compliant and stretchable thermoelectric coils for energy harvesting in miniature flexible devices

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Note S1. Step-by-step fabrication procedures for 3D compliant and stretchable thermoelectric coils

Preparing Si wafer for doping

1. Dice SOI wafer (Si device layer = 200 nm, BOX layer = 1 μm, handling Si = 500 μm) into device size.
2. Clean SOI with acetone, IPA, DI water, then blow dry.
3. Pattern align markers on SOI using photoresist (PR; AZ 5214).
4. Dry etch Si by RIE (50 mTorr, 40 sccm SF_6, RF power of 100 W for 30 s).
5. Remove PR by acetone, then blow dry.

Patterned p- and n-doping

6. Clean SOI with RCA.
7. Deposit 500 nm SiO_2 at 350 °C by plasma enhanced vapor deposition.
8. Pattern p-type opening on SiO_2 using PR (AZ 5214).
9. Etch SiO2 by RIE (50 mTorr, 40 sccm CF_4, 1.2 sccm O_2, RF power of 200 W for 4 min), and then BOE (10:1, 4.5 min).
10. Remove PR by acetone, then blow dry.
11. Clean SOI with RCA.
12. Dope p-type regions with solid boron source at 1000 °C for 14.5 min.
13. Dip in 49 % HF for 20 s to remove SiO_2.
14. Repeat steps 6 to 13 for n-type regions, and use solid phosphorus source at 1000 °C for 5.5 min in step 12.

Preparing PI/PMMA substrates

15. Start with single-side polished, test-grade Si wafer.
16. Clean Si wafer with acetone, IPA, DI water, then blow dry.
17. Expose Si wafer to UV lamp for 5 min.
18. Spin coat PMMA (950PMMA A4) at 2000 rpm for 30 s, then bake at 180 °C for 3.5 min.
19. Spin coat PI (PI 2545) at 1000 rpm for 60 s. Soft bake at 110 °C for 2 min, then at 150 °C for 3 min.
20. Cure in vacuum oven at 220 °C for ≈ 80 min.

Transfer printing Si

21. On SOI: pattern via holes (diameter 3 μm, pitch 50 μm) using thin PR (S1805).
22. Dry etch Si by RIE (50 mTorr, 40 sccm SF_6, RF power of 100 W for 30 s).
23. Etch in 49 % HF for 30 min, then rinse with DI water for at least 1 min.
24. Slowly press down a flat slab of PDMS on SOI, then remove quickly to transfer PR/Si onto PDMS.
25. On PI/PMMA: spin coat PI diluted in NMP (volume ratio 1:3) at 4000 rpm for 60 s, then soft bake at 110 °C for 20 s.
26. Laminate PDMS with PR/Si facing down onto PI/PMMA and apply gentle pressure for 30 s.
27. Place the sample on hot plate at 110 °C, then gently remove PDMS at ≈ 90 s. Soft bake the sample at 150 °C for 1 min.
28. Remove PR by acetone, then blow dry.
29. Cure in vacuum oven at 220 °C for ≈ 80 min.

Isolating Si

30. Pattern Si serpentine layouts using PR (AZ 5214).
31. Dry etch Si by RIE (50 mTorr, 40 sccm SF_6, RF power of 100 W for 30 s).
32. Strip PR by PR stripper (AZ 400T), rinse with DI water, then blow dry.

Metalizing Si

33. Clean the sample by RIE (190 mTorr, 19 sccm O_2, RF power of 100 W for 2 min).
34. Deposit Ti/Au, 60/60 nm by electron beam evaporation.
35. Pattern electrical interconnects and electrodes using PR (AZ 5214).
36. Wet etch Au with gold etchant (gold etchant TFA, 20 s), then Ti with BOE (10:1, 20 s).
37. Strip PR by PR stripper (AZ 400T), rinse with DI water, then blow dry.

Encapsulating Si

38. Spin coat PI (PI 2545) at 1000 rpm for 60 s. Soft bake at 110 °C for 2 min, then at 150 °C for 3 min.
39. Cure in vacuum oven at 220 °C for ≈ 80 min.
40. Pattern device layout using thick PR (AZ P4620).
41. Dry etch PI by RIE (300 mTorr, 20 sccm O_2, RF power of 200 W for ≈ 40 min).
42. Clean sample with DI water and cleanroom swab, then blow dry.

Releasing device from wafer

43. Clamp the sample between two glass slides covered with cleanroom wipe, then immerse in acetone bath overnight.
44. Carefully remove the glass slides, wait 10 s for acetone to evaporate, then laminate a piece of water-soluble tape on top of the device.
45. Slowly peel off the tape to transfer the device onto the tape.

Defining bonding sites

46. Attach a shadow mask (laser-milled Kapton film) onto the device under the microscope.
47. Clean the sample by RIE (190 mTorr, 19 sccm O_2, RF power of 100 W for 2 min).
48. Deposit Ti/SiO_2, 5/50 nm by electron beam evaporation.

Assembling into 3D

49. Stretch a piece of silicone substrate (Dragon Skin 10) to the prescribed strain level.
50. Expose both silicone and sample (still on water-soluble tape) to UV-induced ozone (Jelight UVO-Cleaner, Model 144X) for 5 min.
51. Laminate the tape onto the silicone and apply gentle pressure, then bake in oven at 70 °C for ≈ 8 min.
52. Dissolve water-soluble tape with warm water, then immerse the sample in cold water.
53. Slowly release the pre-strain in silicone substrate to buckle the device into 3D.
54. Evaporate the water under room conditions to complete the fabrications.

Note S2. Power optimization in thermoelectric harvesters

Power output from a thermoelectric harvester

Thermoelectric devices convert heat into electrical power with an efficiency η. The generated power P from a heat flow through a thermoelectric material $\dot{Q}_{\mathrm{TE}}$ is

$$P = \eta \dot{Q}_{\mathrm{TE}} \tag{S1}$$

The conversion efficiency is

$$\eta = \frac{\Delta T_{\mathrm{TE}}}{T_{\mathrm{H}}} \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+1+\frac{\Delta T_{\mathrm{TE}}}{T_{\mathrm{H}}}} \tag{S2}$$

Here, T_{H} is the temperature at the hot side of the thermoelectric material and ΔT_{TE} is the temperature drop across the thermoelectric material that drives $\dot{Q}_{\mathrm{TE}}$. Notice the Carnot efficiency $\eta_{\mathrm{c}} = \frac{\Delta T_{\mathrm{TE}}}{T_{\mathrm{H}}}$ appearing in the equation. ZT is the *device* figure-of-merit employed in device modeling, which is different than the *material* figure-of-merit zT. In the harvester, this distinction can be avoided by simplifying Eq.S2. The "harvesting limit" is characterized by $\Delta T_{\mathrm{TE}} \to 0$, in which we can replace ZT with zT. In addition, $\eta_{\mathrm{c}} \ll (1+\sqrt{1+zT})$ allows for further simplification. The conversion efficiency reduces to a much simpler form

$$\eta = \frac{\Delta T_{\mathrm{TE}}}{T_{\mathrm{H}}} \frac{\sqrt{1+zT}-1}{\sqrt{1+zT}+1} = \frac{\Delta T_{\mathrm{TE}}}{T_{\mathrm{H}}} \cdot \eta_0(zT) \tag{S3}$$

η_0 is an irreversibility factor that determines the conversion efficiency relative to η_{c}, and is a function of only zT in the harvesting limit. The harvested power can now be expressed as

$$P = \eta_0(zT) \cdot \frac{\dot{Q}_{\mathrm{TE}} \Delta T_{\mathrm{TE}}}{T_{\mathrm{H}}} \tag{S4}$$

It is seen that, for a given thermoelectric material, the harvested power is proportional to $\dot{Q}_{\mathrm{TE}}\Delta T_{\mathrm{TE}}/T_{\mathrm{H}}$, a factor that is determined by the heat exchange characteristics of the harvester. $\dot{Q}_{\mathrm{TE}}\Delta T_{\mathrm{TE}}/T_{\mathrm{H}}$ could be thought of as the maximum energy available for conversion.

The thermal impedance matching condition

The thermal impedance matching concept originates from the design situation where $\dot{Q}_{\mathrm{TE}}\Delta T_{\mathrm{TE}}$ (which determines power; Eq.S4) becomes maximum when the thermal impedance of the thermoelectric leg θ_{TE} is at an optimum value; increasing θ_{TE} increases ΔT_{TE} but decreases $\dot{Q}_{\mathrm{TE}}$, creating an optimum point.
In a conventional generator geometry, thermal impedance of the thermoelectric leg can be controlled independently from that of the heat exchangers (θ_{ex} combining both hot and cold sides). For a given temperature difference between the heat source and environment ΔT_{Envi}

$$\dot{Q}_{\mathrm{TE}} = \frac{\Delta T_{\mathrm{Envi}}}{\theta_{\mathrm{ex}} + \theta_{\mathrm{TE}}} \tag{S5}$$

and

$$\Delta T_{\mathrm{TE}} = \Delta T_{\mathrm{Envi}} \frac{\theta_{\mathrm{TE}}}{\theta_{\mathrm{ex}} + \theta_{\mathrm{TE}}} \tag{S6}$$

where zero parasitic heat was assumed. It is seen that $\dot{Q}_{TE}\Delta T_{TE}$ is maximized when $\theta_{ex} = \theta_{TE}$ (or, equivalently $\Delta T_{TE} = \frac{1}{2}\Delta T_{Envi}$). This condition is referred to as the thermal impedance matching condition for thermoelectrics. In practice, $\theta_{ex} \approx \theta_{TE}$ rather than an equality mostly because of the additional heat transport by Peltier currents.

Thermal impedance matching in coil harvesters

In the coil harvester, the impedance matching condition is more complex because θ_{ex} and θ_{TE} are not controllable independently. Scaling the leg length, which is the primary means of controlling θ_{TE}, also changes θ_{TE} because the occupied area of the coil changes (which enlarges the coil surface area). Therefore, one must consider areal power density. In Fig.2d, it is seen that $\Delta T_{TE} = \frac{1}{2}\Delta T_{Envi}$ is still a good criterion for maximizing aerial power density.

Note S3. Effect of PI width on the pop-up yield for 3D coils

To further increase the thermal property of the 3D coil structure, the polyimide (PI) is designed to have a surface area as large as possible near the cold side (top of the 3D coil) using a tapered geometry. A larger cold-to-hot side width ratio gives a better thermal property but will compromise the mechanical property by increasing the strain in the silicon layer (Fig. S4). Furthermore, we observed an increasing trend for the 3D coils to buckle downwards when the width ratio is changed from 2 to 3 during actual experiments. The pop-down coils need to be avoided because they do not contribute to thermoelectric energy harvesting, due to the nearly equal temperature at hot side and cold side in this configuration (*i.e.* $\Delta T \approx 0$).

To address this problem, we calculated the total strain energy for the 3D coil with a width ratio of 2 (Fig. S5a) and 3 (Fig. S5b), each in the two buckling modes (*i.e.* pop-up mode and pop-down mode), at a constant total PI thickness of 8 μm. For the width ratio of 2, the total strain energy of pop-down mode (0.862 μJ) is significantly higher than pop-up mode (0.424 μJ), indicating that the structure will likely to pop-up. Experimentally we observed a pop-up yield of > 95%. However, for the structure with a width ratio of 3, the total strain energy of pop-down mode (0.335 μJ) is only around 30% higher than pop-up mode (0.258 μJ). This leads to an increased pop-down probability, which agrees well with the experimental observations where around 40%to50% structures buckled downwards. The energy difference between pop-down and pop-up mode continues to drop as the width ratio keeps increasing, leading to larger mechanical instability.

Note S4. Mechanical compression test

In the compression test (Fig. 3d and Fig. S7a), the coils are compressed between two parallel glass plates (cover slip and microscope slide) with increasing out-of-plane strain from 10 % up to 40 % for 50 fatigue cycles each. In order to correlate the out-of-plane fatigue with performance, the electrical resistance of the device was measured after each fatigue test. Following 10 % and 20 % tests, the resistance remained at $< 20k\Omega$. After 30 %, the resistance increased slightly to $\approx 25k\Omega$. After 40 %, the circuit became open, indicating fatigue failure (Fig. 3e). The out-of-plane force-displacement response (Fig. S7b) shows limited hysteresis at strains which do not cause fatigue failure, but more apparent hysteresis at 40 % strain, which corresponds to the fatigue failure according to the electrical resistance measurements.

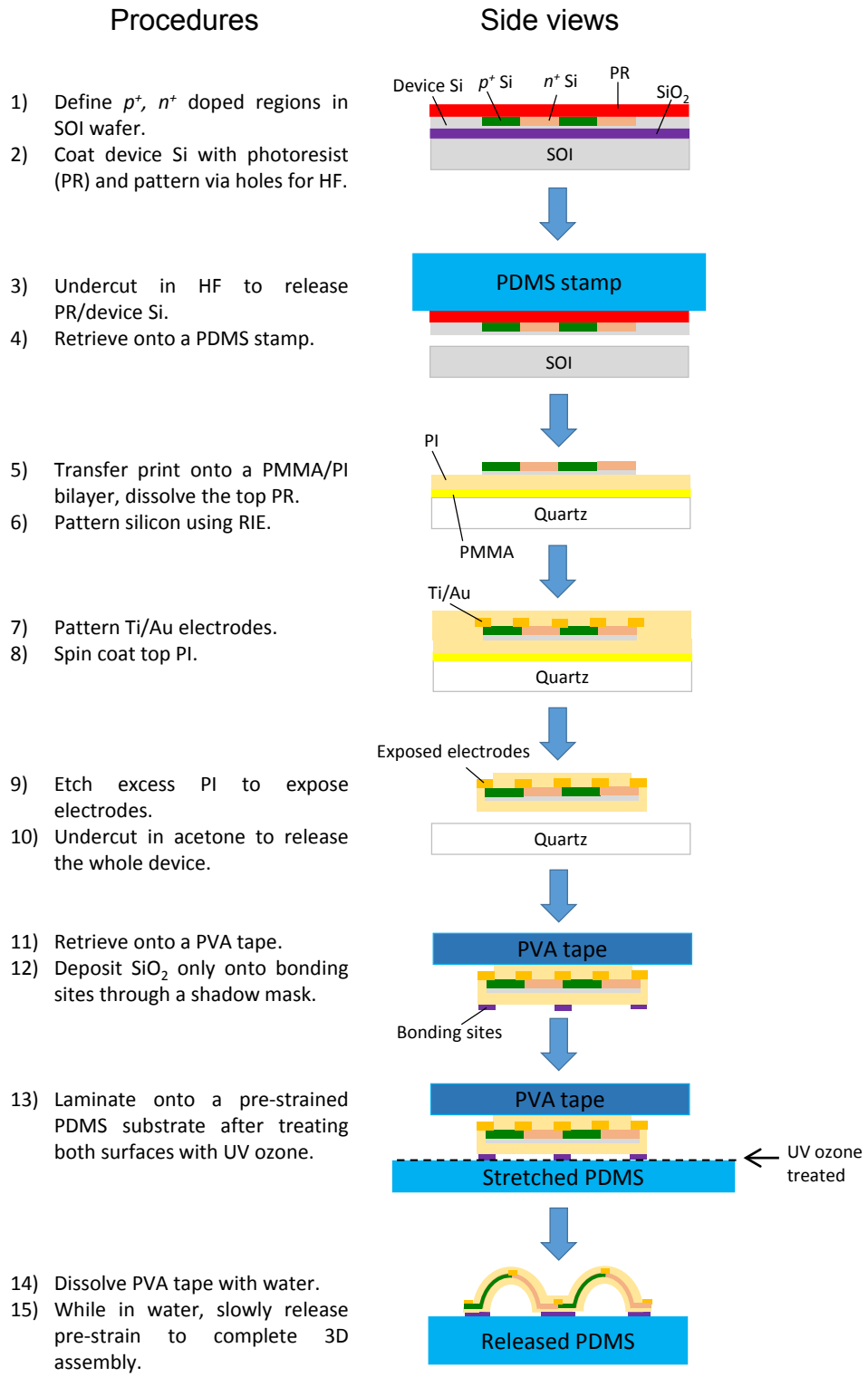

Fig. S1. Schematic step-by-step fabrication procedures for 3D compliant and stretchable thermoelectric coils.

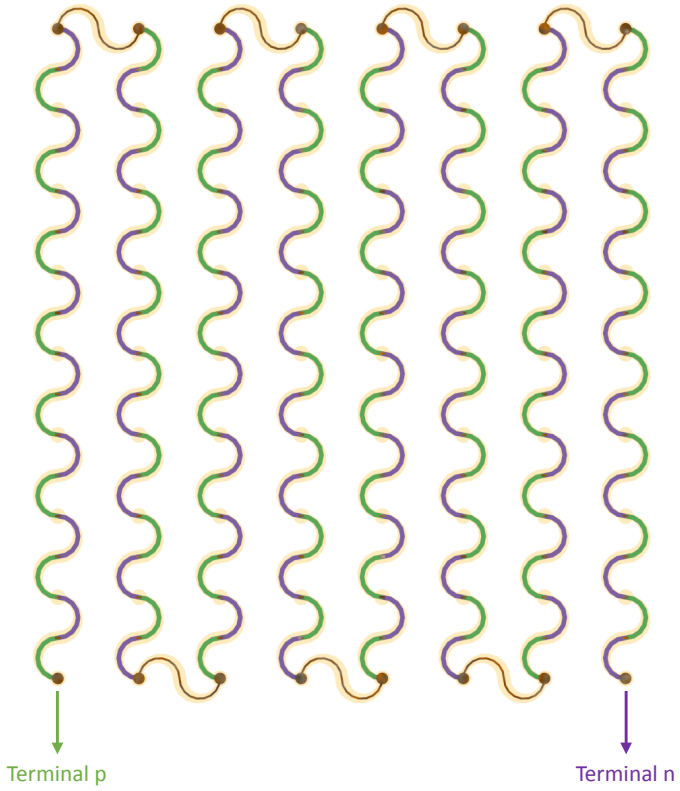

Fig. S2. Design of the 2D precursor for the 8×8 array. The colors in silicon represent p-type (green) and n-type (purple) respectively.

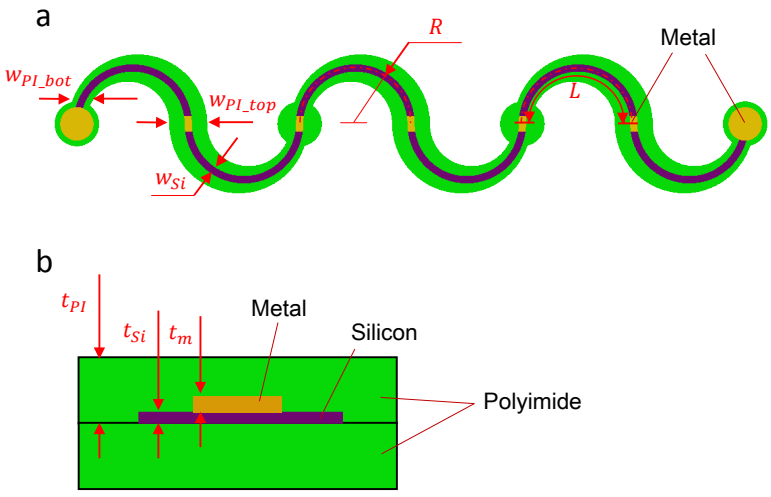

Fig. S3. Illustration of geometric parameters. (a) Definition of geometric parameters for the 2D precursor of spring coil: width of polyimide (PI) $w_{\mathrm{PI\_top}} = 0.34$ mm and $w_{\mathrm{PI\_bot}} = 0.17$ mm (a tapering width ratio of 2); width of silicon $w_{\mathrm{Si}} = 0.065$ mm; radius of leg $r = 0.5$ mm; length of leg $L = 1.57$ mm. **(b)** Schematic illustration of PI encapsulated composite layer (PI/metal/silicon/PI) with optimized thickness $t_{\mathrm{PI}} = 4\ \mu$m, $t_{\mathrm{metal}} = 0.2\ \mu$m, and $t_{\mathrm{Si}} = 0.2\ \mu$m.

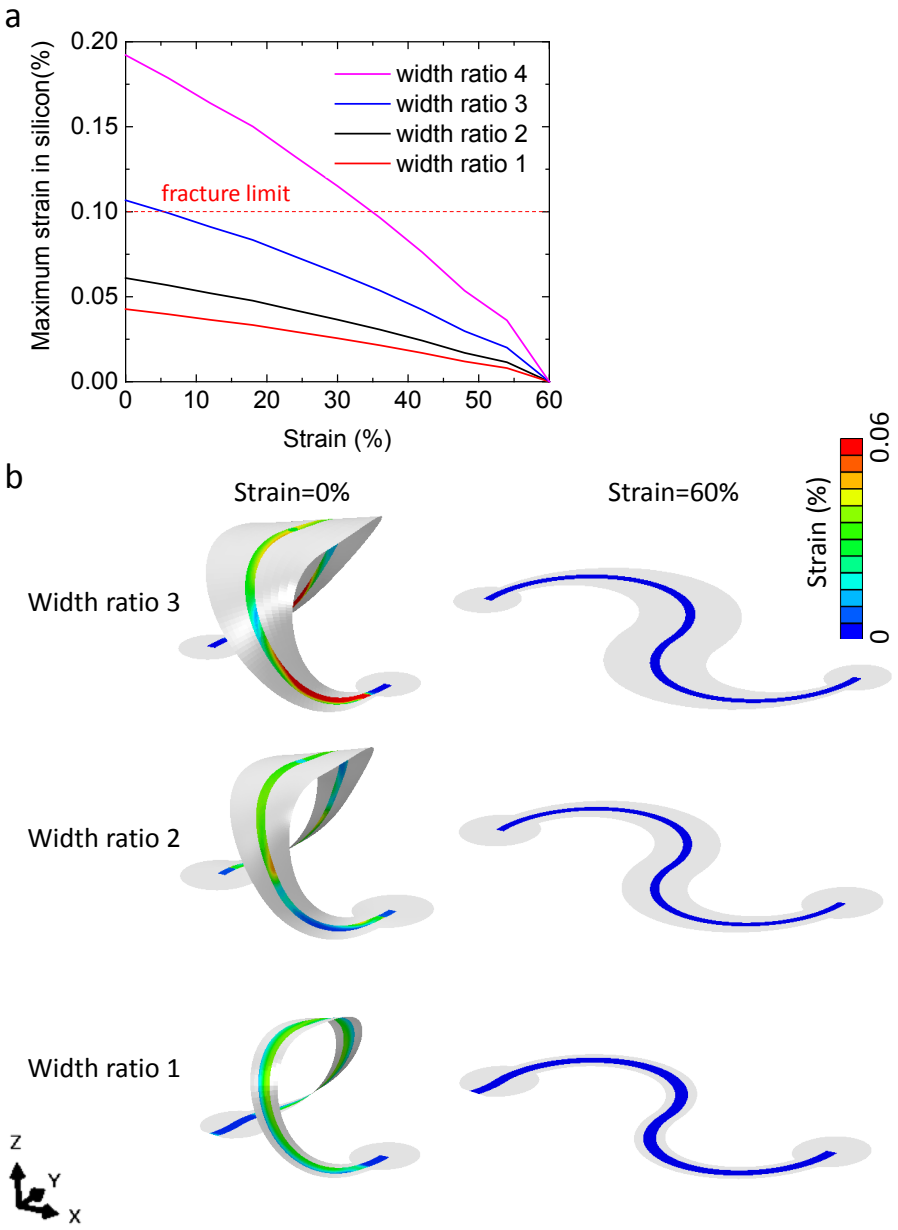

Fig. S4. Mechanics of the in-plane stretching process for the 3D spring coil. (a) Maximum strain in the silicon layer versus the in-plane stretching strain of the 3D spring coil for various designs with different PI widths. **(b)** Deformed configurations with the strain distribution in the silicon layer shown for different designs.

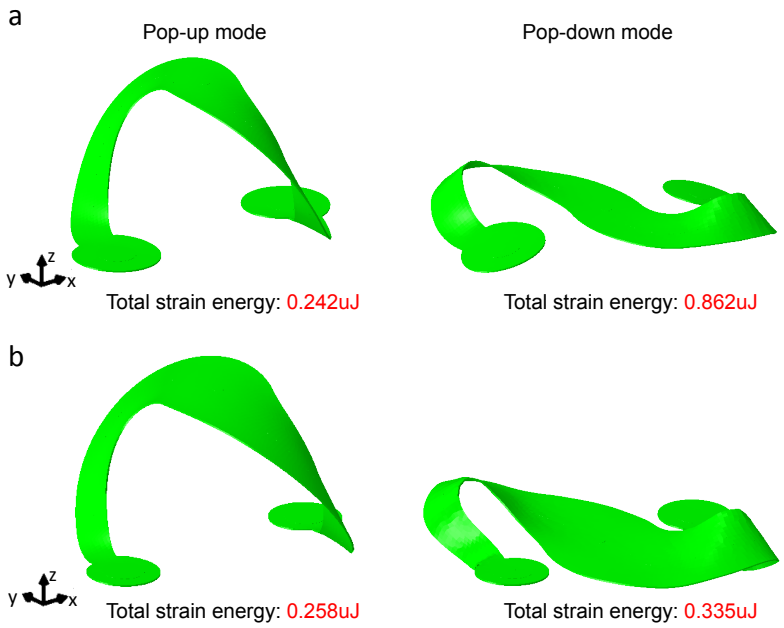

Fig. S5. Polyimide width effect on yield of buckle-up process. Deformed configuration of the pop-up and pop-down mode with total strain energy for cold-hot area width ratio of **(a)** 2 and **(b)** 3. The results indicate that the design with the width ratio of 3 will have a lower yield for the buckle-up process.

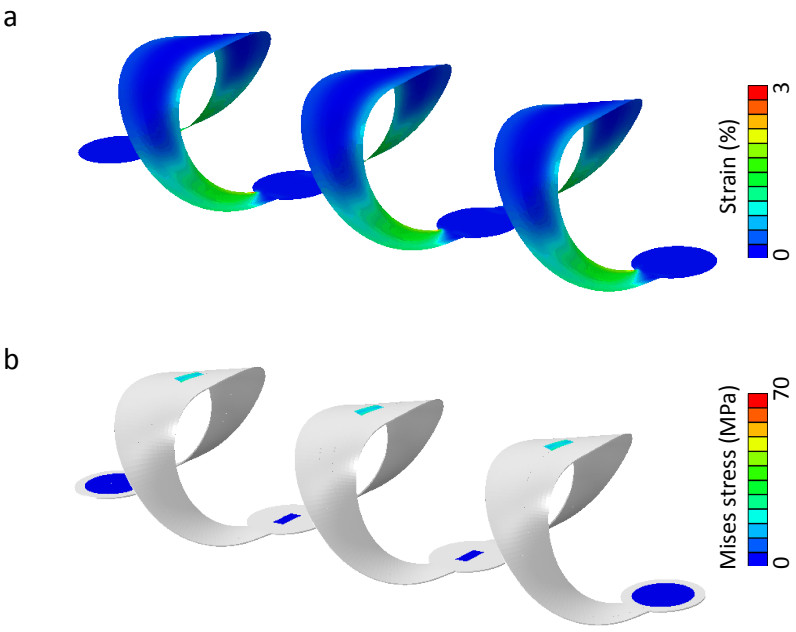

Fig. S6. Simulated strain/stress distribution in the encapsulation and metal layers. **(a)** Strain distribution in the PI encapsulation layer. **(b)** Mises stress distribution in the Ti/Au metal layer. Both are well below the yielding limits of the corresponding materials.

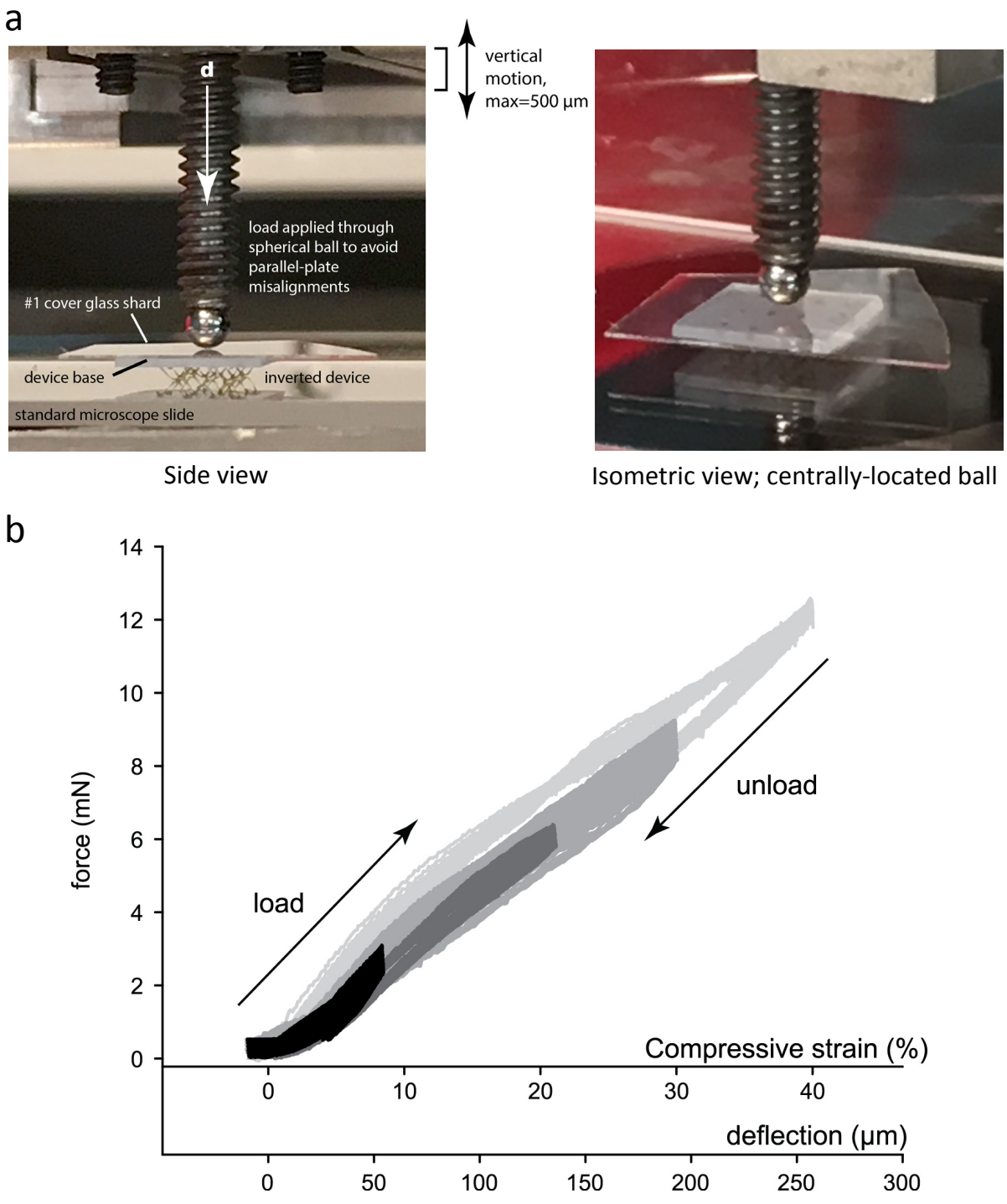

Fig. S7. Mechanical compression testing. (a) Side and isometric views of the test setup. **Photo credit: Xiwei Shan, UIUC Lab. (b)** The out-of-plane force-displacement response from external compression cycles upto 10, 20, 30, and 40 %.

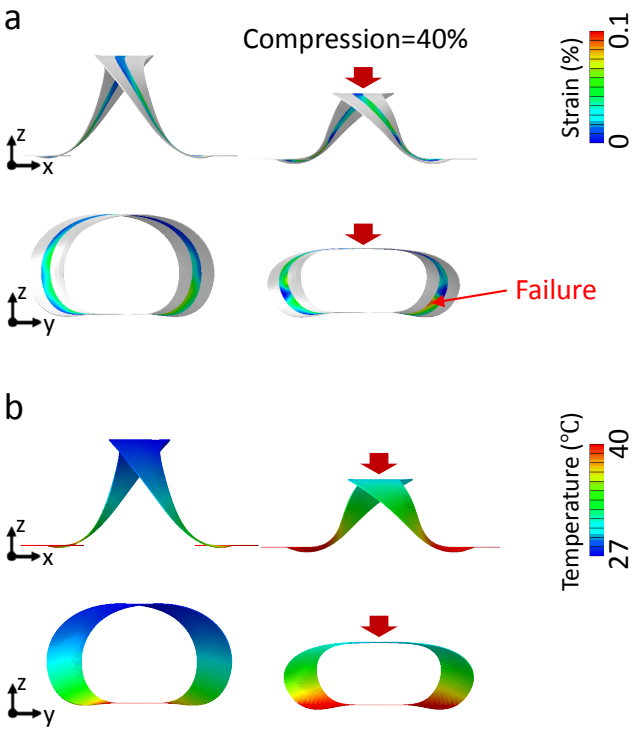

Fig. S8. Mechanics of the vertical compression process of the 3D spring coil. Deformed configuration under 0 (left column) and 40 % (right column) vertical external compression. **(a)** Strain distriubtion in the silicon layer. **(b)** Temperature distribution.

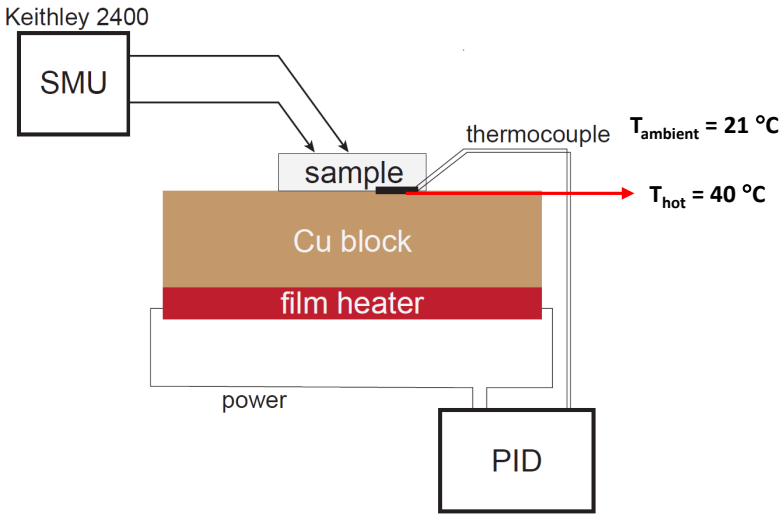

Fig. S9. Schematic illustration of the testing setup for measuring the thermoelectric response of the devices.

	Resistivity [mΩ-cm]	n_Hall [/cm³]	Hall mobility [cm²/Vs]	Seebeck [μV/K]
n-type	0.64	1.9e20	35	-67
p-type	0.86	2.1e20	50	62

Fig. S10. Thermoelectric properties for heavily doped n-type and p-type silicon thin films measured in the silicon-on-insulator wafer form before patterning.

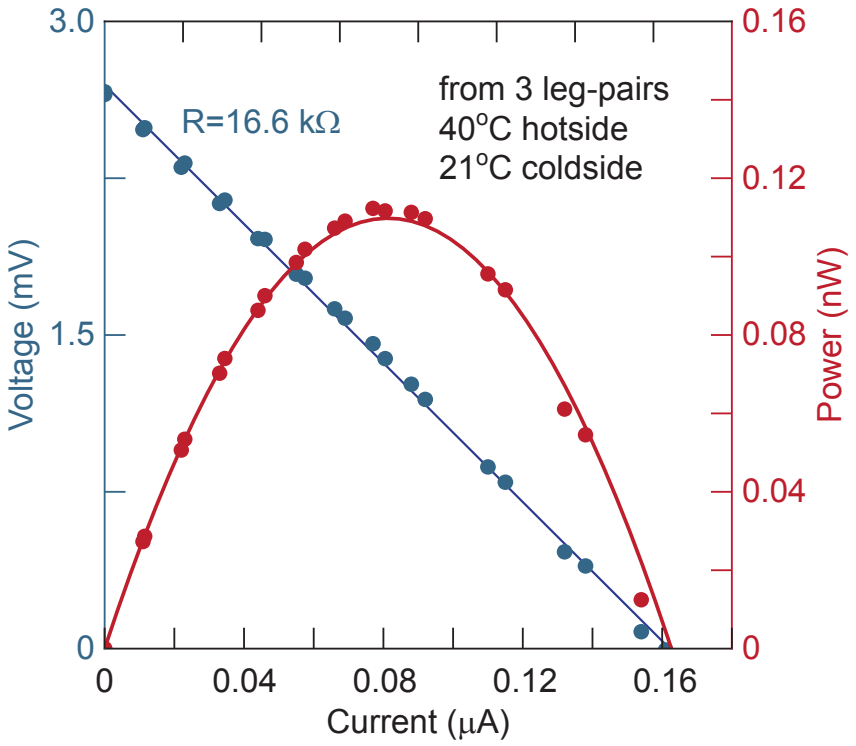

Fig. S11. Output characteristics of the 3×1 harvester shown in Fig. 1B. The open circuit voltage is 2.66 mV at $\Delta T_{\text{Envi}} = 19$ K, which gives an estimated temperature drop of 6.9 K across each individual leg using the Seebeck coefficient measured in Fig. S10.

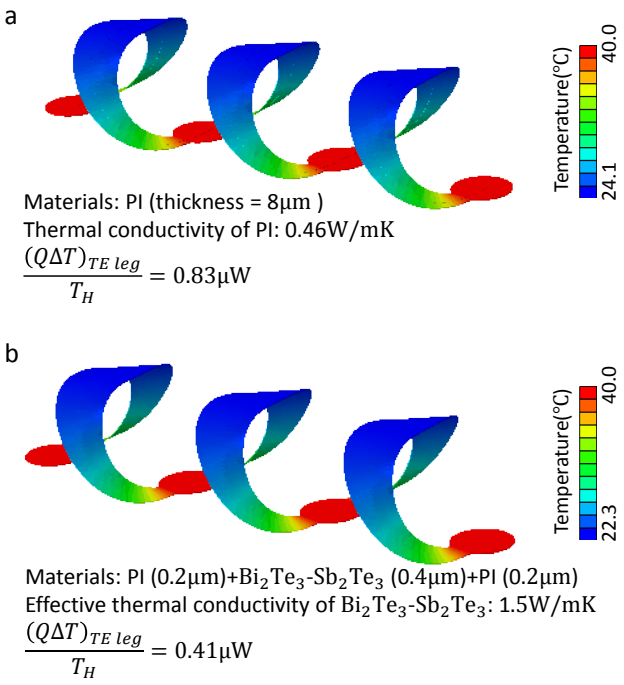

Fig. S12. Preliminary thermal modeling by replacing silicon with other thermoelectric materials. **(a)** In the case of organic thermoelectric materials, they are simply modeled as additional PI layers since they typically have similar mechanical properties and thermal conductivity (0.46 W/m·K is used in this simulation). **(b)** In the case of inorganic thermoelectric materials, Bi_2Te_3-Sb_2Te_3 is used as a reference for properties. The thermal conductivity is set to an effective value [37] of 1.5 W/m·K to account for Peltier heat transfer, which is non-negligible in high zT materials.

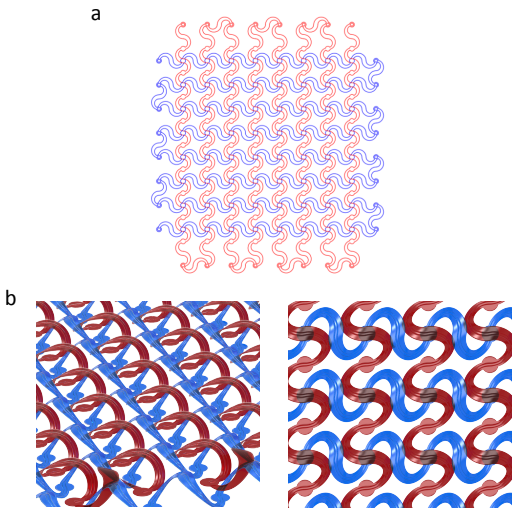

Fig. S13. The design that uses multilayer stacking to improve the power density. **(a)** Layout of the 2D precursor that stacks two 8 by 8 designs rotated by 90° with respect to each other (see Fig. S2 for the original 2D precursor). **(b)** Isometric and top views of the design made into 3D.