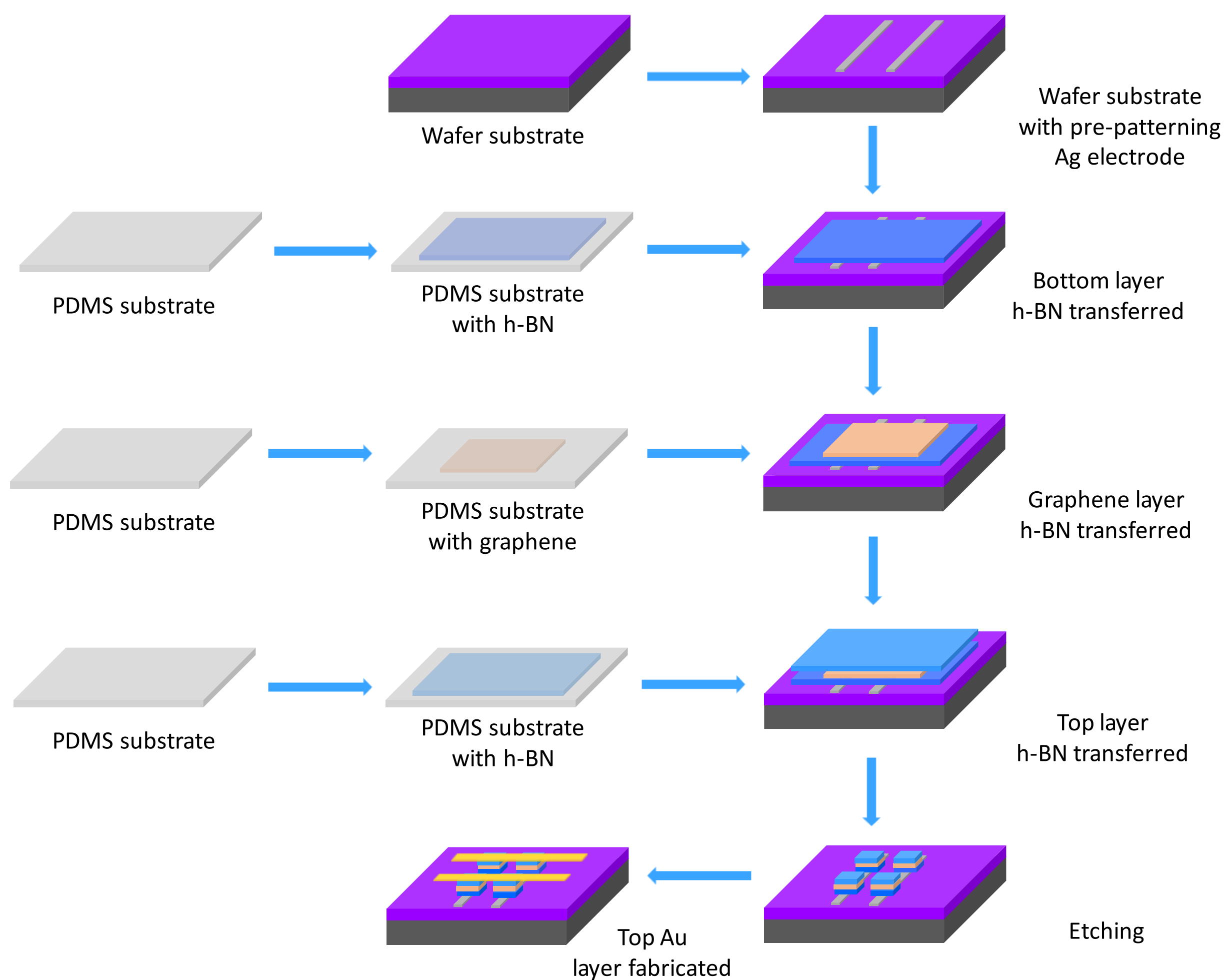
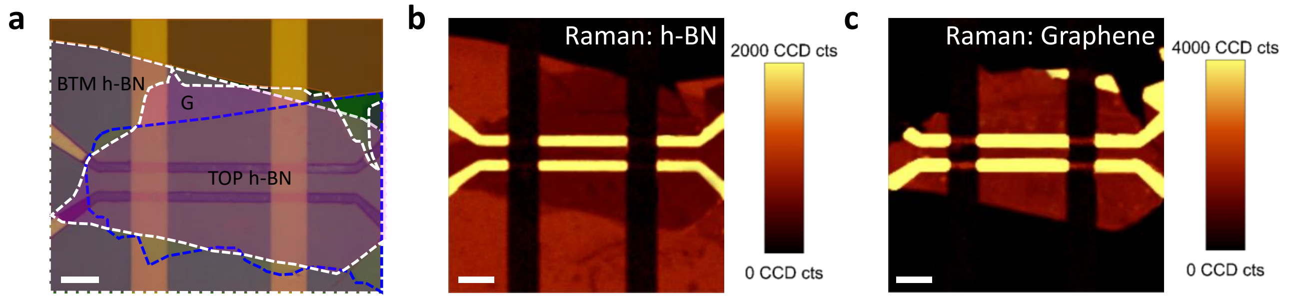
Supplementary Information

Self-selective van der Waals heterostructure for large scale memory array

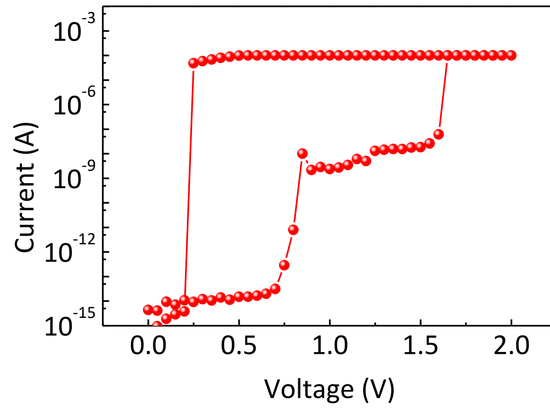
By Sun et al.



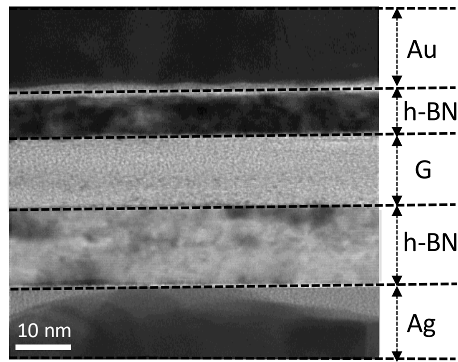
Supplementary Figure 1 Schematic illustration of device fabrication steps. (1) First, the Si/SiO_2 substrate is patterned with Ag as the bottom electrode for our self-selective memory cells by using e-beam lithography and lift-off processes (see details in Methods: Device fabrication). Then, we prepare a polydimethylsiloxane (PDMS) substrate with a pre-exfoliated h-BN layer on it and transfer the suitable h-BN layer on the pre-pattern Ag electrode, assisted by optical microscopy. (2) Using the same methods, another graphene layer is transferred onto the pre-transferred h-BN layer. The alignment during the transfer processes is assisted by optical microscopy. (3) Another h-BN layer with a small thickness is transferred on top of the structure discussed above. (4) Etching the area of the 2D layered materials without the Ag electrode support, as shown in the figure above. (5) Finally, the Au electrode is patterned, forming a cross bar shape relative to the bottom Ag electrode. This schematic is viable for only the memory cell array measurement. For the measurement of a single device, the etching step shown above was omitted (Figure 1 and Supplementary Figure 2).



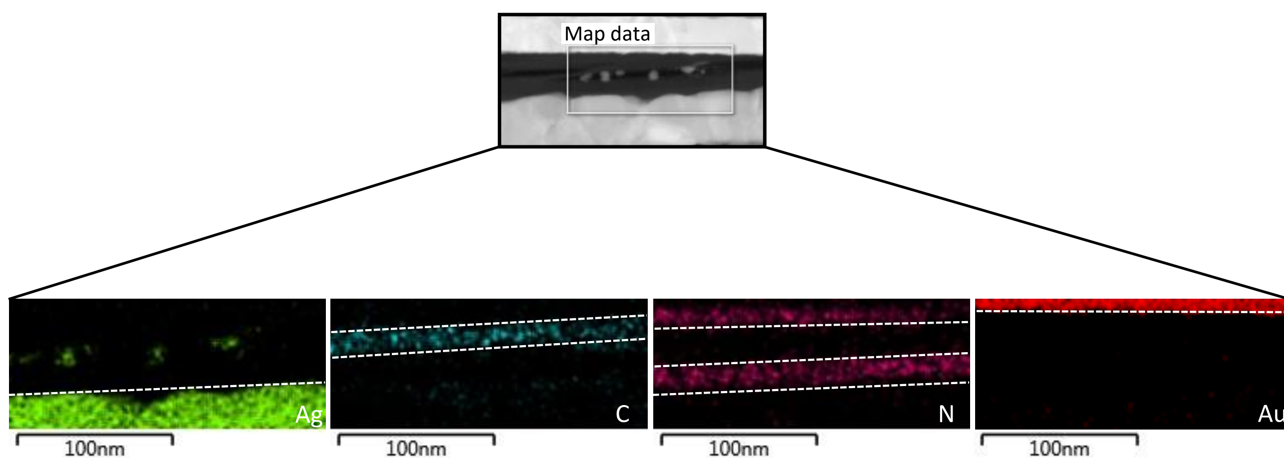
Supplementary Figure 2 Material characterization of van der Waals structures. **a,** Optical image of the fabricated 2×2 self-selective memory. We selected one of them as a single device to measure the I-V curve. In this image, the narrow electrode is Ag while the wide electrode is Au. The areas marked using yellow, white and blue dashed lines represent the bottom h-BN, graphene and top h-BN layers, respectively. The scale bar is 10 μm. **b** and **c** Raman mapping images integrated with the Raman peaks from G bands in h-BN and G band in graphene, respectively. The scale bar is 10 μm.



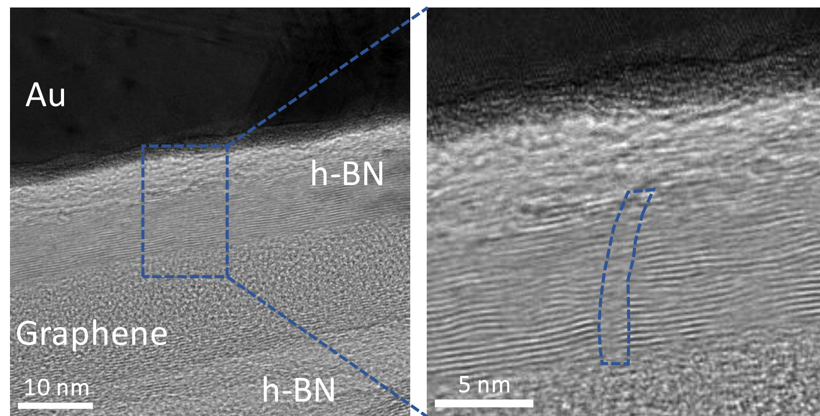
Supplementary Figure 3 Typical I-V curve using thin h-BN layer (~5nm), with a clearly decreased Vth.



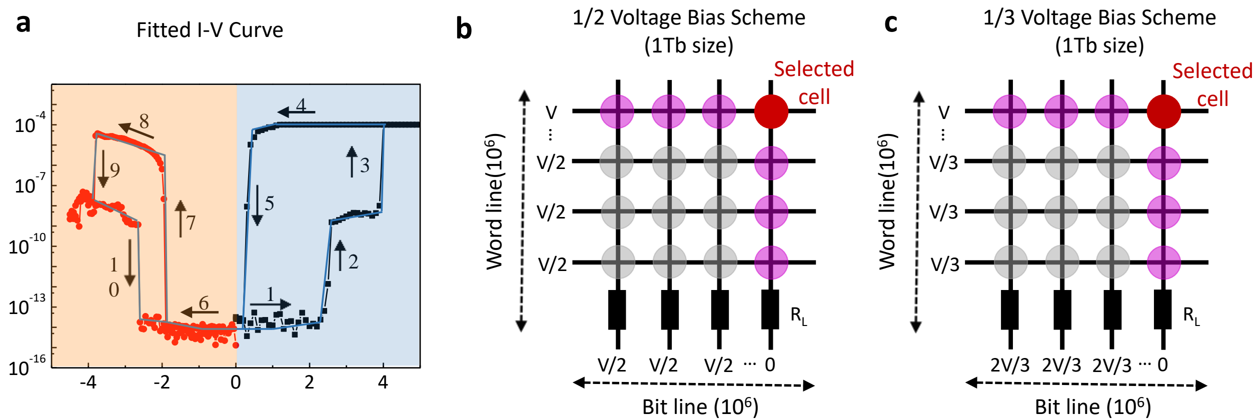
Supplementary Figure 4 Cross-sectional TEM image of our self-selective devices. From top to bottom, there are five layers: Au, thin h-BN, graphene, thick h-BN and Ag layers.



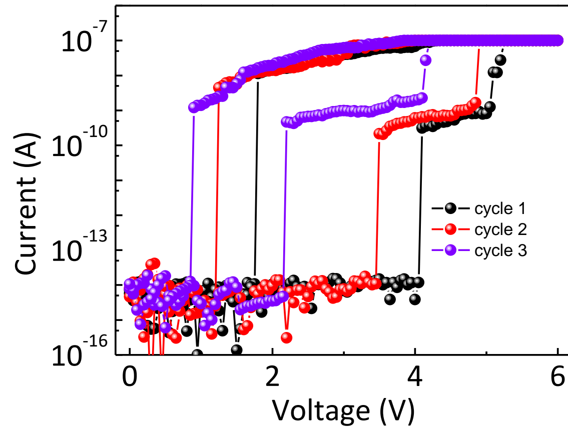
Supplementary Figure 5 The EDX mapping for all involved elements, including the van der Waals structures and electrodes. The clear silver particles are shown near the interface between graphene and bottom the h-BN layer, but there are no sliver particles observed between the Au and top h-BN layer, which is consistent with the discussion in the main text.



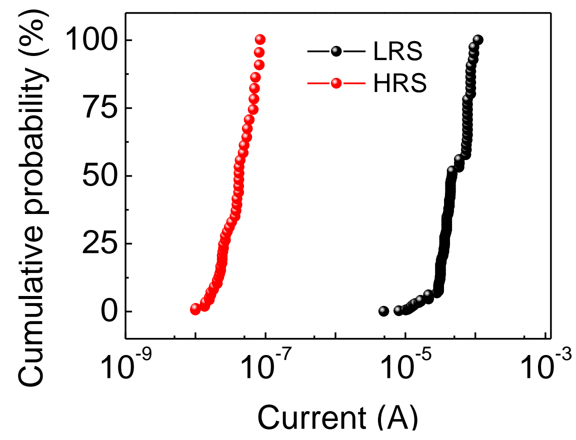
Supplementary Figure 6 The observed defective path in the h-BN layer stacked between the Au and graphene layers, which functions as NVM, as shown by the dashed line in the right zoomed-in figure.



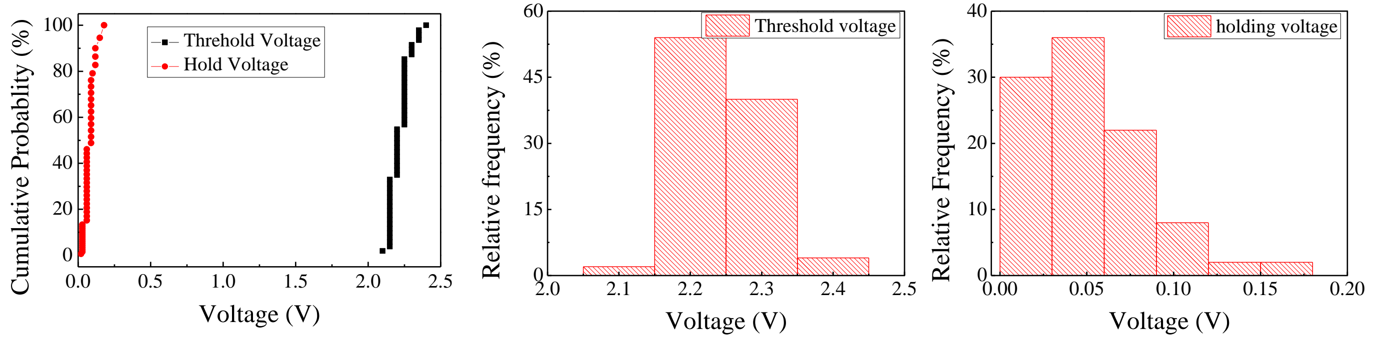
Supplementary Figure 7 The fitted curve for simulation and two bias voltage schemes used in this work. **a,** the simulated DC I-V curve (solid straight line) based on a single self-selective memory cell from the SPICE simulation. **b,** 1/2 voltage bias scheme; **c,** 1/3 voltage bias scheme. For a detailed description of the difference between these two kinds of bias scheme, please refer to the Methods.



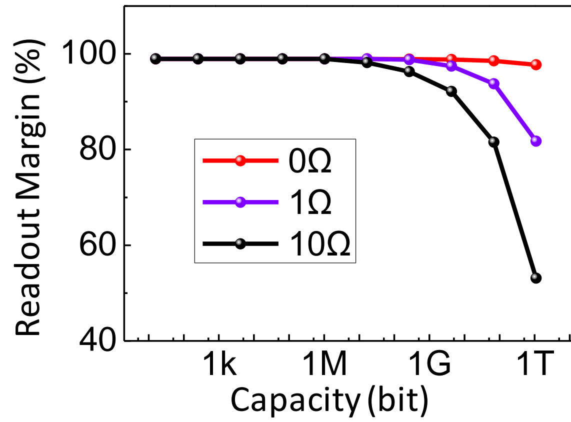
Supplementary Figure 8 The electroforming processes for the self-selective memory cells. Three typical cycles during switching are shown.



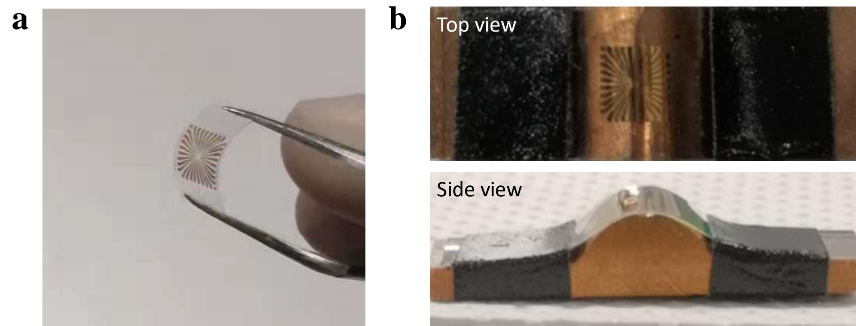
Supplementary Figure 9 Device-to-device variations of HRS and LRS tested on 144 devices.



Supplementary Figure 10 Cumulative probability and histogram of threshold and holding voltage. Once the device is formed (as shown in Supplementary Figure 7a), our devices show a reliable threshold and holding voltage.



Supplementary Figure 11 Readout margin for three different wire resistances between neighboring cells simulated by using SPICE modelling. A one-third voltage scheme was used for this simulation showing a similar result to that obtained using a one-half voltage scheme (Figure 2c). The red, purple and black curves indicates wire resistances of 0 Ω, 1 Ω, 10 Ω, respectively.



Supplementary Figure 12 Optical image of a flexible device on a PET substrate. **a**, an optical image of a device fabricated on flexible substrate. **b**, the top view and side vide of set-up for measurement. A typical device characteristic curve on the bent substrate is shown in Figure 4c (main text).

Structure	ON/OFF ratio	Rectification ratio	Off current	Endurance	Retention	Polarity	Ref
Cu/HfO_2/n-Si	10^4 @1 V	10^4 @±1V	1 nA@1V	50 (DC)	2000 s@85℃	unipolar	[1]
Pt/NbO_x/TiO_y/NbO_x/TiN	10^2 @3V	10^5	1 pA @3V	5000 (DC)	10 yrs	bipolar	[2]
p-Si/SiO_2/n-Si	>10^4 @1.5 V	10^5 @±1.5 V	10 nA @2 V	>100 (DC)	>2×10^5 s @ 300℃	unipolar	[3]
W/Al_2O_3/TaO_x/TiN	>10	>5000	1 nA @0.65 V	10^8	>900h@ 85℃	bipolar	[4]
Pt/Ta_2O_5/HfO2/TiN	10^3 @6 V	10^4 @6 V	>10 pA@±5V	10^3 (DC)	10^46@85℃	bipolar	[5]
Pd/HfO_2/WO_x/W	>10	100 @0.35 V	100 nA@-1 V	10^9	10^4 s @85℃	bipolar	[6]
Ti/SiO_xN_y/AIN/Pt	80	10^2	200 nA @±2 V	10^3	10^5 s	bipolar	[7]
Ni/HfO_2/n^+-Si	10^4 @0.1 V	10^3 @ 1V	>10 pA @±0.5 V	100 (DC)	>2×10^4 s @ 125℃	unipolar	[8–10]
Si/a-Si core/Ag nanowires	10^4	10^6 @±1.5V	1 pA @±1.5 V	10^4	>2 weeks	bipolar	[11]
Pt/Ti/Ta_2O_{5-x}/TaO_{2-x}/ Pt	10	10^5 @±0.7	10 µA @-1 V	10^9	NA	bipolar	[12]
Ag/h-BN/Graphene/ h-BN/Au	10^4	10^{10}	10 fA @±1.5V	10^4	10^6 s	bipolar	This work

Structure	Off current	On/off ratio	selectivity	Two-terminal	ref
Pt/Ag/SiO_x:Ag/Pt/Pd/Ta/Ta_2O_5:Ag/Ru	10 pA	>10	10^7	no	[13]
Ag/Defect graphene/SiO_2/Pt/HfO_2/Cu	1 pA	>100	10^9	no	[14]
Mg/MgO/W/Ag/MgO/Ag/W	10 pA	>100	10^7	no	[15]
Pt/HfO_x/Ag/W/NbOx/W	1 pA	100	10^7	no	[16]
Ti/ZrO2/Pt/Ag/ZrO2:Ag/Pt	1 nA	10	105	no	[17]
Pt/Ag/HfO_x/Ag/Pd/TaOx/Ta_2O_5/Pd	>1 pA	10	10^7	no	[18]
Ag/h-BN/graphene/h-BN/Au	10 fA	10^4	10^{10}	yes	This work

Supplementary Table 1 Comparison of the performance of previously reported NVM devices, including self-rectifying memristors (top table) and non-self-rectifying memristors (bottom table). It is clearly shown that compared with that of non-self-rectifying cells, the operation performance of self-rectifying memory cells is usually poor, although their device structure is relatively simple. However, the complex device structure, fabrication processes, and the three-terminal architectures for non-self-rectifying memory cells hinder their application for 3D integration. Our new self-selective memory cells possess the advantages of both self- and non-self-rectifying memory cells.

Supplementary References

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