Thermal transport modeling - estimation of χ_{abs}

We estimate the parameter χ_{abs} based on ideal ballistic propagation of phonons from the heater to the nanowire through the thin dielectric. To simplify the analysis, we assume that the heater instantaneously reaches the stationary response due to the dissipated power at the time when an electrical pulse is applied. Phonons in the WSi travel along ballistic trajectories with the average sound velocity v with an angle θ with respect to normal of the interface and we consider only the absorption of phonons, neglecting re-emission in this treatment. The electron system of the nanowire is assumed to have an equilibrium distribution described by the temperature T_e . Under these assumptions, the kinetic equation describing the phonon distribution in the nanowire $N_{WS_i}(\omega, z, \theta, t)$ with depth in the z direction from $0 \leq z \leq d$ is given by

$$
\frac{\partial N_{WSi}}{\partial t} + v \cos(\theta) \frac{\partial N_{WSi}}{\partial z} = -\frac{N_{WSi} - N^0 (T_e)}{\tau_{ph-e}}
$$
(1)

where $N^0(T_e)$ is the Planck distribution at the electron temperature of the nanowire and τ_{ph-e} is the phonon-electron interaction time. Under the assumption of a stationary input phonon distribution $N^H(T_H)$ from the heater at $z = 0$, the solution to this partial differential equation becomes

$$
N_{WSi}(\omega, z, \theta) = N^0(T_e) + \left[N^H(T_H) - N^0(T_e)\right]e^{-\frac{z}{l_{ph-e}\cos(\theta)}}
$$
\n
$$
\tag{2}
$$

where $l_{ph-e} = v\tau_{ph-e}$ is the energy-dependent phonon-electron interaction length. The energy transferred to the WSi is expressed as $Q_{WSi}^{in} - Q_{WSi}^{out} = P \chi_{abs} f = Q_{WSi}^{in} \chi_{abs}$. The energy flux is evaluated according to

$$
Q(z) = \int_0^{\omega_D} d\omega \rho(\omega) \hbar \omega v \int_0^{\theta_m} d\theta \sin(\theta) \cos(\theta) N(\omega, z, \theta)
$$
 (3)

where $\rho(\omega)$ is the phonon density of states and ω_D is the Debye frequency. Using this form, we evaluate χ_{abs} by rearranging terms and evaluating Q_{WSi}^{in} at $z = 0$ and Q_{WSi}^{out} at $z = d$, leading to

$$
\chi_{abs} = \frac{\int_0^{\omega_D} d\omega \rho(\omega) \hbar \omega v \int_0^{\theta_m} d\theta \sin(\theta) \cos(\theta) \left[N^H(T_H) - N^0(T_e) \right] \left(1 - e^{-\frac{d}{l_{ph-e} \cos(\theta)}} \right)}{\int_0^{\omega_D} d\omega \rho(\omega) \hbar \omega v \int_0^{\theta_m} d\theta \sin(\theta) \cos(\theta) N^H(T_H)} \tag{4}
$$

We take a series expansion of the exponential function because $\frac{d}{l_{ph-e} \cos(\theta)} \ll 1$ for thin WSi nanowires. The interaction length is given by $\frac{1}{l_{ph-e}(\omega)} \approx \frac{\gamma}{v\tau}$ $\overline{v\tau_0}$ $\int \frac{\hbar \omega}{2}$ $\overline{k_B T_c}$ for $\hbar\omega \geq 2\Delta$ and 0 otherwise. This occurs because only phonons with energies greater than 2∆ are capable of breaking Cooper pairs. The parameter $\gamma = \frac{8\pi^2}{5}$ $\frac{\pi^2}{5} \frac{C_e}{C_{pl}}$ $\overline{C_{ph}}$ $\Big|_{T_c}$ describes the ratio of electron to lattice heat capacity at T_c . We can neglect the $N^0(T_e)$ term in (4) because the WSi temperature is significantly less than the heater temperature for the power dissipation levels measured experimentally, and we confirm that this approximation is valid by numerical calculation of the full and approximate expressions. Under these simplifications, and assuming low temperature, we arrive at the expression

$$
\chi_{abs} = \frac{1}{\cos\left(\frac{\theta_m}{2}\right)^2} \frac{\gamma d}{v\tau_0} \left(\frac{T_H}{T_c}\right) \frac{\int_{2\Delta/k_B T_H}^{\infty} dx \frac{x^4}{e^x - 1}}{\int_0^{\infty} dx \frac{x^3}{e^x - 1}}.
$$
\n
$$
\tag{5}
$$

To determine χ_{abs} , we estimate $\tau_0 = 5000 \,\text{ps}$ based on measurements[1] of τ_{ep} and the parameters listed in the main text. The heater temperature is determined using thermodynamic properties of Au and Pd and an estimated phonon escape time of 100 ps.

Supplementary Figure 1. Estimation of χ_{abs} as a function of input power density. The value of χ_{abs} has a weak dependence on temperature in the range of interest.

This calculation leads to a value of χ_{abs} which is between 0.01 and 0.03 over the dissipated power range measured in the turn-on delay experiment, which is the same range needed to match experiment based on the simple fixed χ_{abs} model. The absorption fraction increases as the dissipated power increases due to the increased number of high energy phonons present in the heater radiation. These high energy phonons have a shorter $l_{ph-e}(\omega)$, leading to a higher fraction of energy absorbed in the nanowire. However, this simplified model neglects the influence of $SiO₂$ scattering, which also increases as phonon energy increases and is expected to limit the magnitude of this change in χ_{abs} . Consequently, the ballistic propagation assumption used in this model is violated for these higherenergy phonons. A fully quantitatively accurate model of phonon transport must also consider the reflection of phonons off both the SiO_2/WSi and SiO_2/Si interfaces. While transmission from $SiO₂$ to WSi is estimated to be approximately 70% based on the acoustic mismatch model for most incident angles, total internal reflection of acoustic modes is predicted at the SiO_2/Si interface for incidence angles greater than 50 degrees, which will increase the number of phonons available for absorption in the nanowire layer.

Crosstalk and lateral heat transport

In order to determine whether the device had significant in-plane heating, we designed a device with a narrow heater-resistor centered in a nanowire meander. The geometry can be seen in Supplementary Figure 2. In this experiment, we applied power to the resistor and measured the resulting resistance of the nanowire meander. The results, shown in Supplementary Figure 2b, indicate that there is very little in-plane heating: at powers around D_c , we see a resistance in the nanowire form that is equivalent to the superconducting material directly underneath the resistor becoming normal. Only at much greater applied powers (∼1 mW) does this resistance

Supplementary Figure 2. Design and results of edge-leakage test. (a) Geometry of the edgeleakage test, showing a narrow resistor element (red) routed through the middle of a large nanowire meander (black). (b) Experimental data and theoretical modeling of the device resistivity as a function of temperature for the edge-leakage test. Adding a temperature dependence of the resistance versus temperature curve would smooth the onset of finite resistance at low heater power.

increase significantly indicating that a much greater amount of power is necessary to heat the superconducting material in the neighborhood of the resistor–likely due to heating the entire device substrate, as was observed in Ref. [2].

The experimental results are consistent with thermal modeling of the lateral heat transport in thin SiO_2 . By using the approach of Ref. [2] with the same form and value of the thermal coupling between the $SiO₂$ and Si for a bath temperature of 1 K, we calculated the temperature of the dielectric layer as a function of distance from the edge of the heater using a worst-case scenario where the device was always being heated. The resulst are shown in Supplementary Figure 3. We found that the surrounding temperature–and thus thermal crosstalk–falls off within a distance of a few micrometers. The upper limit of scalability ultimately depends on the thermal coupling from the substrate to the cold bath and the cooling power of the fridge, but for this particular material stack, the devices could be patterned quite densely.

Supplementary Figure 3. Distance from the edge of the heater at which the dielectric reaches a given temperature as a function of heater power density.

References

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