Supporting Information: Semiconductor Epitaxy in Superconducting Templates

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SUPPORTING INFORMATION 1: HYBRID-TASE EPITAXY ALONG LOW SYMMETRY DIRECTIONS

Uniform III-V semiconductor growth inside hybrid-TASE templates in multiple crystallographic directions can be of great importance for applications that require engineering of spin-orbit interaction [1–3]. In the Main Text (Fig. 3e-h) we demonstrated that an isotropic growth rate in high-symmetry directions was accomplished via growth at As rich atmosphere with V/III=150. In Fig. S.1 we demonstrate growth in the lower symmetry ⟨113⟩, ⟨114⟩, ⟨115⟩ and ⟨116⟩ directions. The same results were obtained for templates oriented in ⟨115⟩, ⟨116⟩, ⟨221⟩, ⟨331⟩ and ⟨441⟩ direction (not shown). As discussed below, these results are not only a consequence of the global growth conditions in the reactor but also due to the presence of an exposed TiN surface inside the template cavities.

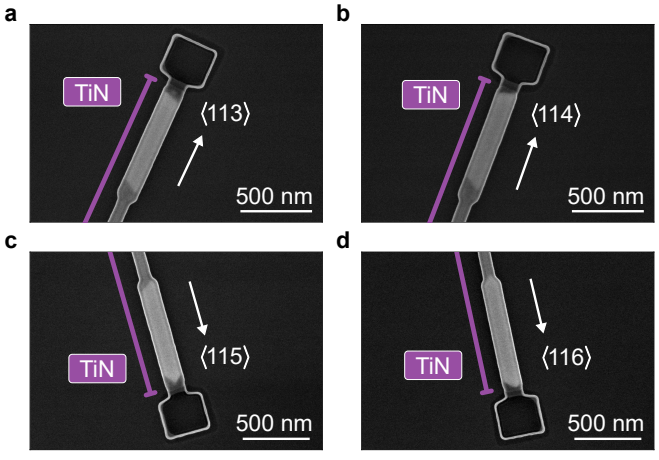

FIG. S.1. **Hybrid-TASE InAs epitaxy in lower symmetry directions.** Templates have similar aspect ratio and equal growth conditions as devices shown in Fig. 3 of the Main Text but different crystallographic alignment in **a** ⟨113⟩, **b** ⟨114⟩, **c** ⟨115⟩ and **d** ⟨116⟩ direction, respectively. Purple lines indicate the extent of TiN stripes inside hybrid templates.

SUPPORTING INFORMATION 2: INAS EPITAXY DYNAMICS IN HYBRID-TASE TEMPLATES

InAs epitaxy inside hybrid-TASE templates exhibited significantly altered growth dynamics compared to TASE epitaxy inside full SiO_2 templates. Our observations include a change of facet morphology and increased axial growth rate. In the following, we investigate these effects at a range of epitaxy conditions and draw a direct comparison to TASE reference growth.

To study the impact of exposed TiN inside the templates, we patterned SiO_2 reference templates on the same chips as hybrid-TASE templates, thereby ruling out parameter variations between epitaxy runs as the origin of our observations. To pattern TASE cavities, we extended the area of TiN etching in Fig. 1c of the Main Text to remove TiN on the entire NW length.
Growth inside normal reference templates is presented in Fig. S.2. The reference templates have similar aspect ratio and equal crystal orientation as hybrid templates shown in Fig. 3 of the Main Text. While the uniformity of growth rates along ⟨110⟩, ⟨111⟩, ⟨112⟩ and ⟨100⟩ template directions was reproduced in normal templates, the axial NW growth rate was reduced by more than a factor of two compared to hybrid epitaxy. {110}, {111}B and {112} facets at the InAs growth front can be discerned in Fig. S.2, viewed through the thin SiO_2 template layer. These results are consistent with faceting observed in previous studies on epitaxy in normal SiO_2 templates [4, 5]. The high growth uniformity and radial filling of the templates as well as the formation of prominent {111}B facets at As rich epitaxy has been attributed to enhanced growth of {110} facets and suppressed growth in ⟨111⟩ direction due to As trimer formation on the {111}B facet [6–8]. We note that this was particularly apparent in normal templates along the ⟨111⟩ and ⟨112⟩ direction (Fig. S.2b and c), where we observe formation of single {111}B facets, indicating that {110} facets are grown out completely, despite the growth front is still deep inside the template.

Results presented in Fig. 3 of the Main Text, and Figs. S.1 and S.2 were obtained by growth in As rich atmosphere with V/III=150. Reducing the V/III precursor ratio to 70 and decreasing the TBAs and TMIn flows to 137 μmol/min and 1.9 μmol/min, respectively, allowed us

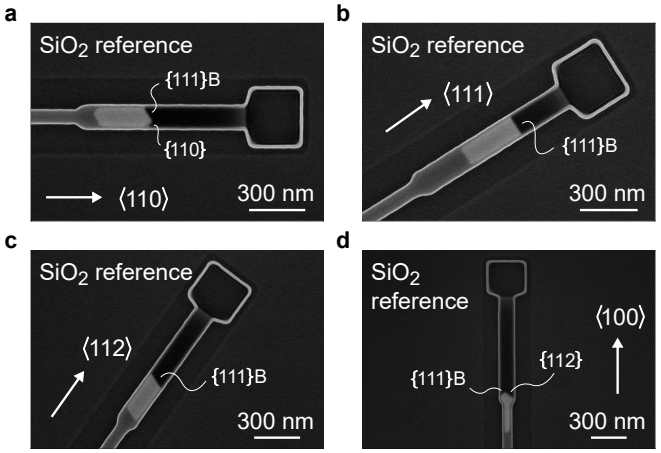

FIG. S.2. **TASE reference epitaxy.** InAs growth inside TASE templates without integrated TiN surface. Reference templates have a similar aspect ratio and were exposed to equal growth conditions as hybrid-TASE templates presented in Fig. 3 of the Main Text. Crystallographic alignment of normal reference templates in **a** ⟨110⟩, **b** ⟨111⟩, **c** ⟨112⟩ and **d** ⟨100⟩ direction is equal to hybrid-TASE devices in the Main Text.

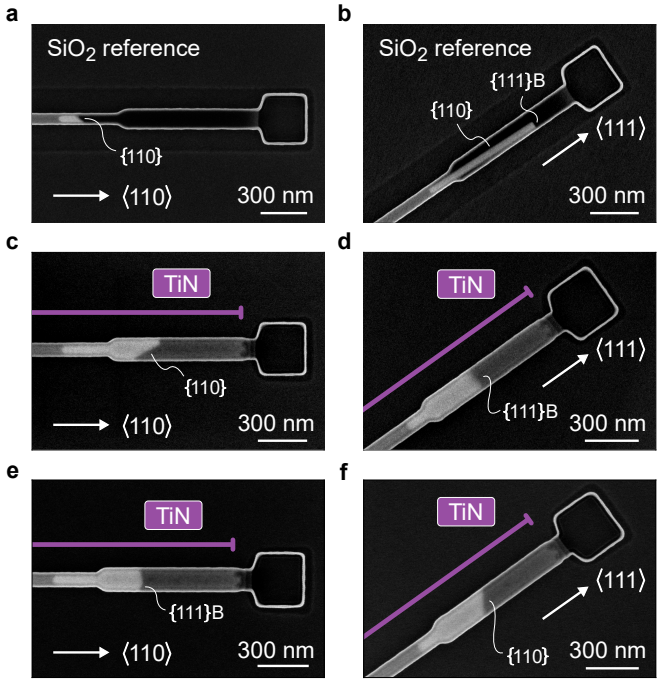

FIG. S.3. **Comparison of TASE and hybrid-TASE InAs epitaxy at low As flow.** InAs epitaxy with reduced precursor flow and V/III=70 inside TASE templates aligned along the **a** ⟨110⟩ and **b** ⟨111⟩ direction and inside hybrid-TASE templates along the **c, e** ⟨110⟩ and **d, f** ⟨111⟩ direction, respectively. Purple lines indicate the extent of TiN stripes integrated into hybrid templates.

to study the dependence of the apparent growth rate enhancement inside hybrid-TASE templates as a function of crystal direction. Under these conditions, a growth time of 42 min was required to obtain devices presented in Fig. S.3. Importantly, the effective V/III ratio inside the templates was further decreased as a consequence of the high aspect-ratio of our template geometry [9]. Hence, the new growth conditions resulted in an As sparse atmosphere. In Fig. S.3 we compare epitaxy along the ⟨110⟩ and ⟨111⟩ direction inside normal and hybrid templates. When grown at low As flux, InAs does not cover exposed Si areas after nucleation [10, 11]. To prevent the size of the Si seed to impact our comparison between TASE and hybrid-TASE growth in Fig. S.3, we etched cavities deep enough as to reach a constriction with lithographically defined cross section of 40 nm × 70 nm. The constriction smoothly expanded into a cavity with cross section 100 nm × 70 nm, as the InAs growth front progressed.
In Figure S.3a we present InAs growth inside a normal template aligned along the ⟨110⟩ direction. In this geometry we consistently obtained short wires that did not extend beyond the seed constriction but exhibited distinct {110} facets. This behavior is consistent with growth at low V/III ratio, where growth of the {111}B facet far exceeded that of the {110} facet. For growth inside normal ⟨111⟩ aligned templates (Fig. S.3b) this behavior was further emphasized as growth of the {111}B facet was not limited by the template side walls. This resulted in a 770 nm long wire with a single {111}B growth facet. Growth of the six {110} NW side facets was suppressed completely and the NW diameter was effectively determined by the Si seed cross section and not by the template. The suppression of {110} side facet growth corroborates the lack of group-V precursor molecules [12, 13], since they access the template predominantly via Knudsen diffusion [9, 14] and are then incorporated at the {111}B facet.

The situation changed when a TiN surface was present in the cavity. In the ⟨110⟩ aligned hybrid template (Fig. S.3c) the InAs crystal extended into the wide cavity region and radially expanded to the template walls. The increase in both radial and axial growth rate points towards a faster growth of {110} facets compared to the reference growth in SiO_2 templates. While the wire exhibited a {110} facet as in the reference example, there was a second, most likely {111}B facet, that is not grown out entirely, indicating a more balanced growth between {110} and {111}B facets. Again, our findings are confirmed by epitaxy in ⟨111⟩ direction (Fig. S.3d) where a single {111}B facet formed, similar to the reference (Fig. S.3b). However, the cavity was radially filled similar to growth in ⟨110⟩ direction (Fig. S.3c), confirming faster growth of {110} facets when a TiN surface was present. The NW in Fig. S.3d was 260 nm shorter than the reference, since the higher growth rate of {110} facets caused a competition between {110} and {111}B facets for precursor material. We emphasize that

such a decrease in axial growth rate was observed only in this specific situation, that is at reduced precursor flow in ⟨111⟩ oriented templates. In all other growth regimes investigated in this work, accelerated growth in ⟨110⟩ direction resulted in longer wires.

While growth in normal templates with the conditions of Fig. S.3 always resulted in the growth morphology presented in Fig. S.3a and b, we observed a higher variability in faceting for the hybrid case. Two further examples are presented in Fig. S.3e and f where we observe at least one {111}B facet in a ⟨110⟩ hybrid template and a single {110} facet in a ⟨111⟩ hybrid template. A wide range of possible facet morphologies has previously been observed for GaAs and InAs epitaxy in TASE templates [4, 5]. The variability in morphology between individual wires has been ascribed to microscopic details of the Si seed morphology and nucleation on it. Consequently, the multitude of facet configurations in hybrid-TASE growth of Fig. S.3c-f points towards a more balanced growth equilibrium compared to epitaxy in reference templates of Fig. S.3a and b. In the latter case, the InAs facet morphology was entirely dominated by the As supply limited growth conditions.

Increased semiconductor growth rates have previously been reported in literature in the context of vapor-liquid-solid (VLS) NW growth and selective area growth (SAG) using a metal mask. Catalytic decomposition of group-III precursors molecules on the Au droplet surface caused a faster growth of GaP, GaAs and InAs VLS NWs [15] while fast lateral growth in SAG was attributed to enhanced surface diffusion of group-III precursors on a W mask surface [16, 17]. Growth selectivity in the latter process was found to significantly decrease for low growth temperature and rough metal surfaces [18, 19]. We stress that in our work the smooth back face of an integrated TiN layer was exposed, the roughness of which was set by the native SiO_2 layer below (see Fig. 3 of the Main Text). We speculate that the smooth TiN surface morphology lead to a more homogeneous surface energy that was less dominated by anisotropic surface energies of grain facets [20], enabling selectivity during hybrid-TASE epitaxy.

To summarize, fast epitaxy in hybrid-TASE templates could be the result of enhanced precursor surface diffusion on the integrated TiN segment. The change in facet morphology from TASE reference epitaxy to hybrid-TASE epitaxy (Fig. S.3) indicated an increased effective V/III material ratio at the growth front. The increase in {110} facet growth rate leads us to the conclusion that the origin of the V/III ratio increase is a locally enhanced As vapor pressure rather than a reduced In pressure inside template cavities. We are not aware of previous work where an increased efficiency of group-V precursor incorporation by means of a metal surface was reported. Future work will include a detailed study of growth dynamics in the presence of metal surfaces.

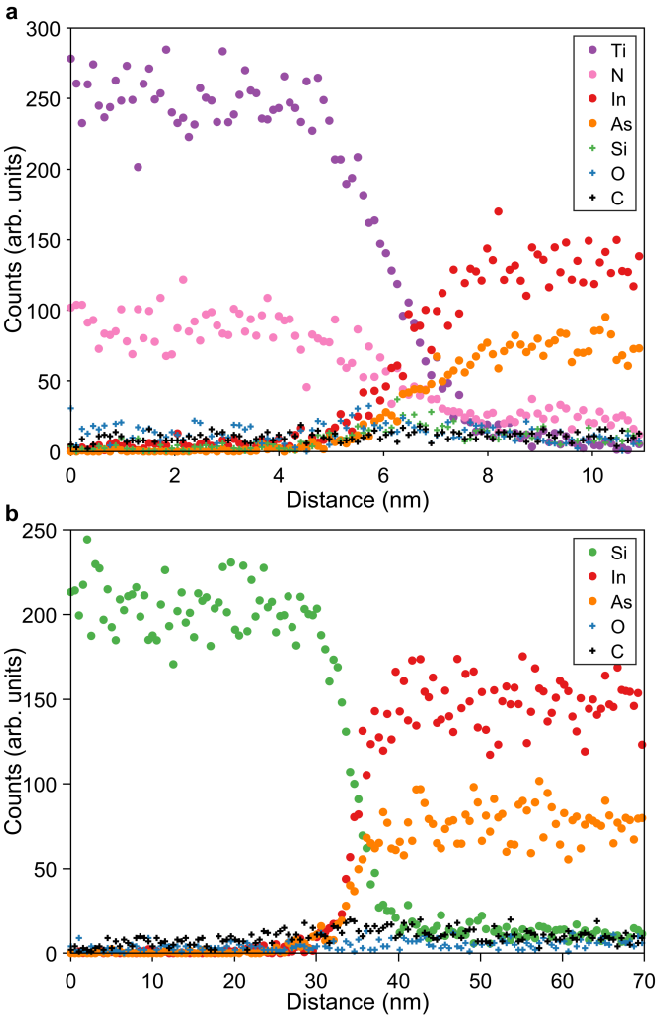

FIG. S.4. **EDX elemental line profiles. a** EDX line scan of the hybrid TiN/InAs interface of Fig. 2e of the Main Text. **b** EDX line scan of the Si/InAs seed interface of Fig. 3a of the Main Text.

SUPPORTING INFORMATION 3: EDX ANALYSIS OF HYBRID-TASE INTERFACES

The characteristics of the hybrid TiN/InAs interface and the Si/InAs seed interface were discussed in the Main Text. Figures S.4a and b show EDX lines profiles of the interfaces presented in Figs. 2e and 3a of the Main Text, respectively.

SUPPORTING INFORMATION 4: SEED MORPHOLOGY

We obtained the lateral ADF-STEM images of a hybrid-TASE NW presented in Fig. 2d and Fig. 3a of the Main Text by cutting a lamella parallel to the ⟨110⟩ nanowire axis. This scenario is sketched in the schematic top view of Fig. S.5a. To highlight the V-shaped seed morphology, the figure only shows the Si seed (green) and the InAs nanowire (red) and we omit a layer of native SiO_2 on top of the seed and a stripe of TiN covering both the seed and the InAs NW. In Fig. S.5b we show a schematic representation of the ⟨100⟩ zone axis view of the lamella, similar to the ADF-STEM image shown in Fig. 2d of the Main Text. The {111} facet planes of the Si seed are inclined by an angle of 54.7 ° with respect to the nanowire axis. Consequently, the zone axis of the high resolution ADF-STEM image of the seed in Fig. 3a of the Main Text is not perpendicular to the Si/InAs interface. This has two important consequences: First, the imaged Si/InAs interface does not show an abrupt transition from Si to InAs. This is a consequence of the geometrical projection of the inclined interface on the viewing plane. Secondly, the layer of native SiO_2 is only present at the Si/TiN interface but appears to extend towards the InAs/TiN interface. This observation can be understood as a consequence of the complex seed morphology as well. We highlight the location of the native SiO_2 layer in the exploded-view drawing of Fig. S.5c. In Fig. S.5d we present an ADF-STEM image recorded in the region highlighted by the orange box in Fig. S.5b. Both geometrical projection effects discussed above can be recognized in this image: The Si/InAs interface appears smeared out and the native SiO_2 layer appears to extend to the hybrid interface only in the region where inclined Si {111} facets are present.

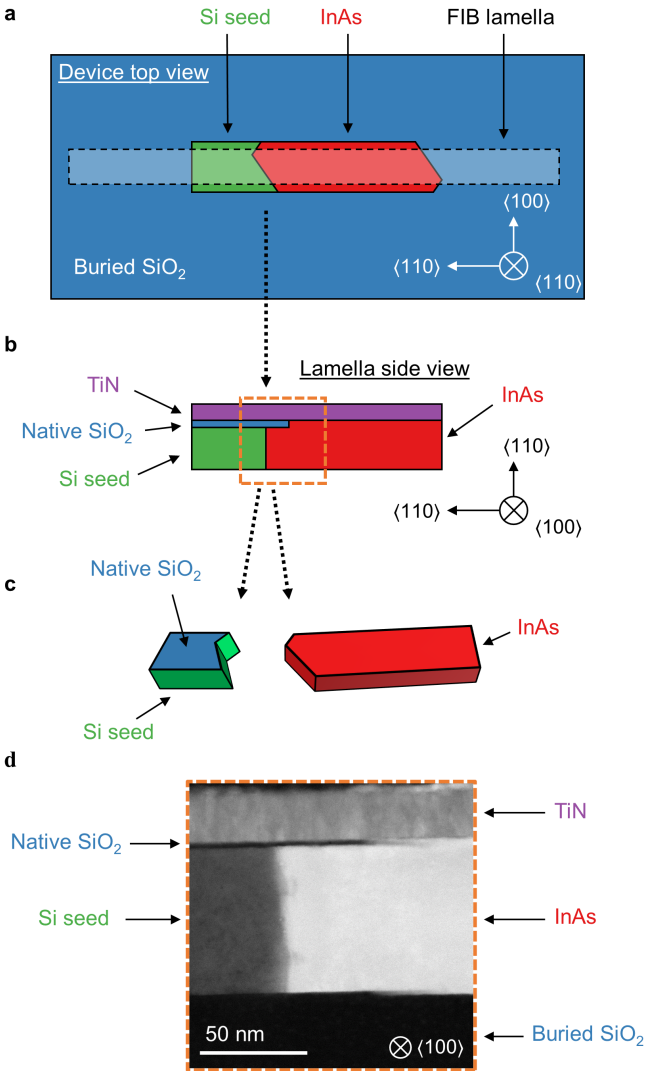

FIG. S.5. **Morphology of the Si seed.** **a** Schematic top view of a InAs NW (red) grown along the ⟨110⟩ direction. Native SiO_2 and TiN are omitted for clarity. The FIB lamella orientation of Fig. 2d of the Main Text is indicated. **b** Schematic representation of the ADF-STEM image presented in Fig. 2d of the Main Text. A thin layer of native SiO_2 (blue) is present between the Si seed layer (green) and the TiN layer (purple). **c** Exploded-view drawing of the Si/InAs seed interface. The thin native SiO_2 layer covers the V-shaped Si seed. **d** ADF-STEM overview image of the seed region indicated by the orange square in **b**.

SUPPORTING INFORMATION 5: CRYSTALLINITY OF A HYBRID-TASE NANOWIRE

In Fig. 3 of the Main Text we present Fast Fourier Transforms (FFTs) of the Si/InAs seed interface region. We conclude that InAs grows epitaxially from the Si seed. In Fig. S.6 we present further FFTs recorded at different positions along the InAs nanowire axis. The data show that the InAs nanowire is a single crystal since the epitaxial relation is maintained throughout the nanowire.

SUPPORTING INFORMATION 6: ELECTRICAL TUNING VIA A BACK-GATE

At a temperature $T = 14$ K, TiN in the device of Fig. 4a of the Main Text was resistive and we operated the metallized silicon handle wafer as a back-gate. A representative pinch-off curve is presented in Fig. S.7. Oscillations in the conductance trace were reproduced throughout several sweeps of the back-gate voltage V_{BG}, consistent with conductance fluctuations in the wire. Measurements in Fig. 4 of the Main Text were performed at $V_{BG} = -15$ V, indicated by the dashed line in Fig. S.7.

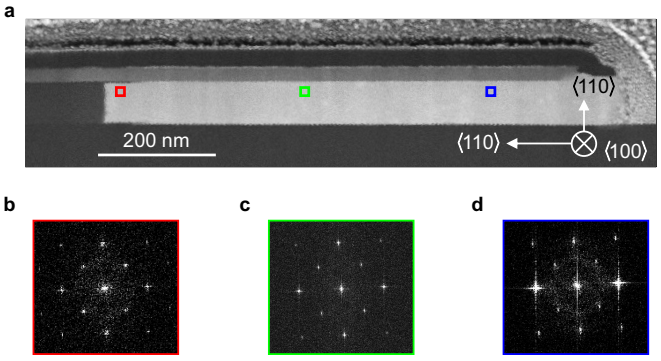

FIG. S.6. **Single-crystallinity of a hybrid-TASE nanowire.** **a** Overview of a hybrid-TASE InAs crystal cut along the nanowire axis and imaged along the ⟨100⟩ zone axis. Image is the same as Fig. 2d of the Main Text. Colored squares indicate regions where FFTs of **b**, **c** and **d** were extracted. **b** FFT of the InAs crystal close to the seed interface. Image is the same as Fig. 3d of the Main Text. **c** FFT of the InAs crystal in the center region of the nanowire. **d** FFT of the InAs crystal close to the template opening.

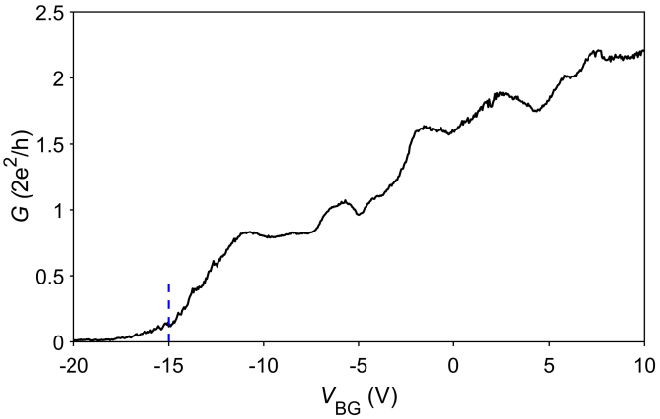

FIG. S.7. **Back-gate tuning of a hybrid-TASE device.** Tuning of a hybrid-TASE nanowire using the Si back-gate at $T = 14$ K. Blue dashed line ($V_{\mathrm{BG}} = -15$ V) indicates the operating point of measurements in Fig. 4 of the Main Text.

SUPPORTING INFORMATION 7: TITANIUM NITRIDE SUPERCONDUCTING GAP

We investigated the impact of template fabrication on the superconducting properties of TiN. For this purpose, we characterized TiN NWs after exposure to different steps of the hybrid-TASE fabrication scheme. The NWs were dry etched from a 20 nm thick layer of TiN, they were 80 nm wide and 2 μm long. The patterning was performed in analogy to the TiN dry etching presented in the hybrid-TASE process flow (see Methods Section of the Main Text). In Fig. S.8 we present the critical current I_{C} of a typical NW as a function of temperature T. The NW was not exposed to further fabrication and we use it as a reference in the following comparison. We

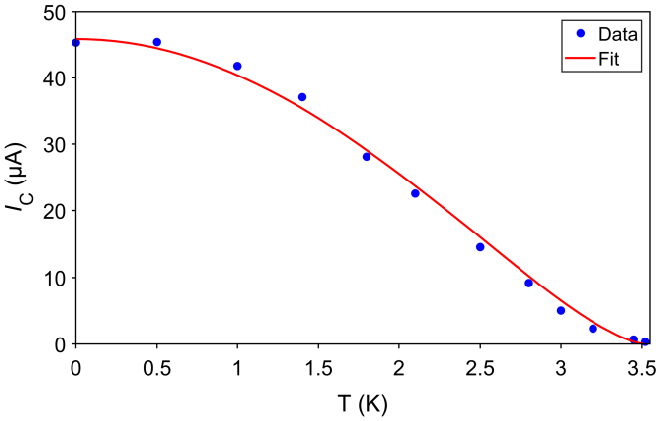

FIG. S.8. **TiN nanowire critical current.** Critical current of a patterned TiN NW on a Si substrate as a function of temperature. Bardeen's formula was used to fit the data.

fit I_{C} with Bardeen's formula [21]:

$$I_{\mathrm{C}}(T) = I_{\mathrm{C0}}\left(1 - \frac{T^2}{T_{\mathrm{C}}^2}\right)^{\frac{3}{2}} \tag{S.1}$$

where I_{C0} is the critical current at $T = 0$ and T_{C} is the critical temperature. Both quantities are fit parameters and we obtain $I_{\mathrm{C0}} = 46$ μA and $T_{\mathrm{C}} = 3.5$ K which corresponds to a superconducting gap $\Delta(T = 0) = 1.76 k_{\mathrm{B}} T_{\mathrm{C}} = 531$ μeV, consistent with [22]. In [23] we presented an extensive study on etched TiN NW devices and obtained similar values of T_{C} for more than 20 devices, irrespective of the NW width or length. This confirms that the extracted value of T_{C} is representative of the TiN quality prior to any further template fabrication. We list the superconducting properties as Stage 1 in Table I.

Next, we investigated NWs that were encapsulated in a 40 nm SiO_2 template using the same plasma-enhanced ALD process as for hyrbid-TASE devices (see Methods Section of the Main Text). For these devices, we measured a critical temperature of 3.3 K (Stage 2a in Table I). At Stage 3a we annealed wires encapsulated in SiO_2 for 30 s at 600°C in Ar/H_2 atmosphere, similar to the annealing process we performed during template fabrication of hybrid-TASE devices (see Methods Section of the Main Text). After this short annealing step, wires showed a significantly reduced T_{C} of 2.8 K. We attribute the degradation to the partial oxidation of TiN in the presence of SiO_2 at the annealing temperature. Note that in this experiment devices were annealed only for a short time of 30 s. During InAs epitaxy, devices are exposed to similar temperatures for much longer times of approximately 30 min. Therefore, it is reasonable to assume that the superconductor will degrade even further during InAs epitaxy.

To investigate the influence of template material on TiN degradation we encapsulated TiN NWs in a SiN_x tem-

TABLE I. **Comaparison of TiN NWs at different fabrication stages.** TiN NWs were exposed to different stages of the hybrid-TASE process flow and the critical temperature was measured after each step. **Stage 1** TiN NWs were patterned on a Si substrate. **Stage 2a** TiN NWs were encapsulated in a SiO_2 template. **Stage 3a** NWs encapsulated in SiO_2 were annealed at 600°C for 30 s. **Stage 3b** NWs encapsulated in a SiN_x template were annealed at 600°C for 30 min.

Fabrication stage	T_C (K)	Δ (μeV)
Stage 1 NW patterned	3.5	531
Stage 2a, SiO_2 NW encapsulated	3.3	500
Stage 3a, SiO_2 NW annealed for 30 s	2.8	425
Stage 3b, SiN_x NW encapsulated and annealed for 30 min	3.7	561

plate using plasma-enhanced ALD and annealed the devices at 600°C for 30 min (Stage 3b in Table I). Note that this annealing time and temperature were representative of the conditions during InAs epitaxy in hybrid-TASE templates. Despite the long annealing time, T_C of these devices did not decrease compared to the reference devices. This finding corroborates our interpretation that the presence of a SiO_2 template during high-temperature processing is the main source of TiN degradation in our process flow. We envision that future devices will employ SiN_x as the template material to preserve the superconducting properties of integrated nitride superconductors.

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