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Supplemental information

A synthetic distributed genetic multi-bit counter

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Supplementary Information for "A synthetic distributed genetic multi-bit counter"

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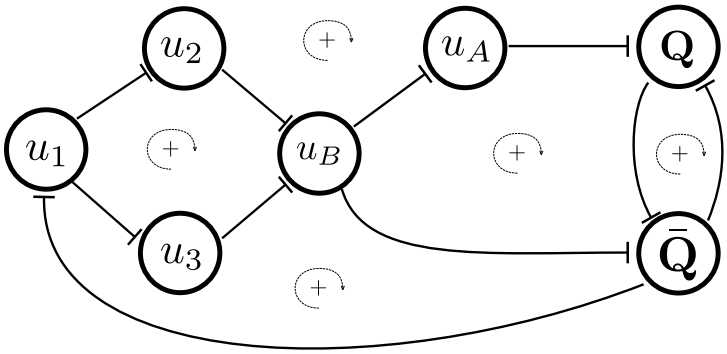
1 Long-term behavior of the autonomous one-bit counter

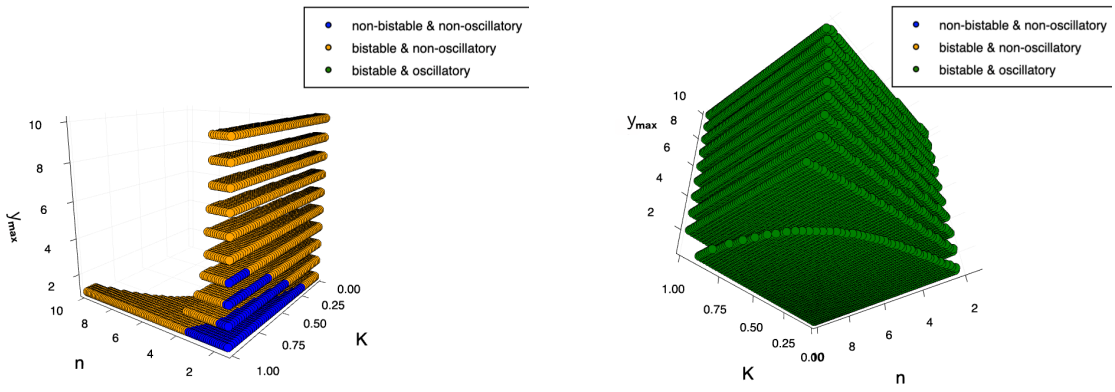
In the absence of an external input, the 1-bit counter depicted in Fig. 2-A is a dynamical system capable of exhibiting multi-stationarity for certain parameter ranges. But in order to show that it is indeed a multi-stable system, we need to prove that every trajectory converges to a steady state. To that end, we can use known results [1] to show that the autonomous 1-bit counter is a monotone system that enjoys generic convergence to steady-states under mild conditions. This precludes the possibility of oscillatory or chaotic behaviors. An informal proof can be achieved by examining the influence graph of the network and verifying that every single loop has a positive sign as can be seen in Supplementary Figure 1. More details on the specifics of the method can be found in [1].



Supplementary Figure 1: **Graphical test of monotonicity.** Related to Figure 2. Every (undirected) loop in the influence graph of the autonomous 1-bit counter has a positive sign. Every edge of the form "⊣" is assigned a negative sign. The sign of a loop is the product of the signs of the constituent edges.

2 Parameters that give rise to bistability and oscillation

In the main paper, we have discussed how bistability and oscillatory dynamics arise when varying the parameters K, n, and $y_{\max}$. For each point in the 3D parameter space, we evaluate if the corresponding parameter set produces multiple steady states for the 1-bit counter. This is accomplished by computing the trajectories corresponding to 100 random initial conditions to evaluate the number of distinct steady state solutions in the absence of an external input signal. Similarly, we find the parameter sets that allows the 1-bit counter to exhibit an oscillatory behavior when a constant input signal is applied. Combining these two numerical studies, we partition the 3D phase space into three distinct regions based on our simulation results. Supplementary Figure 2-(a) marks the regions "not bistable and not oscillatory", "bistable and not oscillatory" and "bistable and oscillatory". We select our parameters from the last region which has the potential of producing a functional 1-bit counter.



(A) Regions that are "not bistable & not oscillatory" and "bistable & not oscillatory".

(B) The region which shows "bistable & oscillatory".

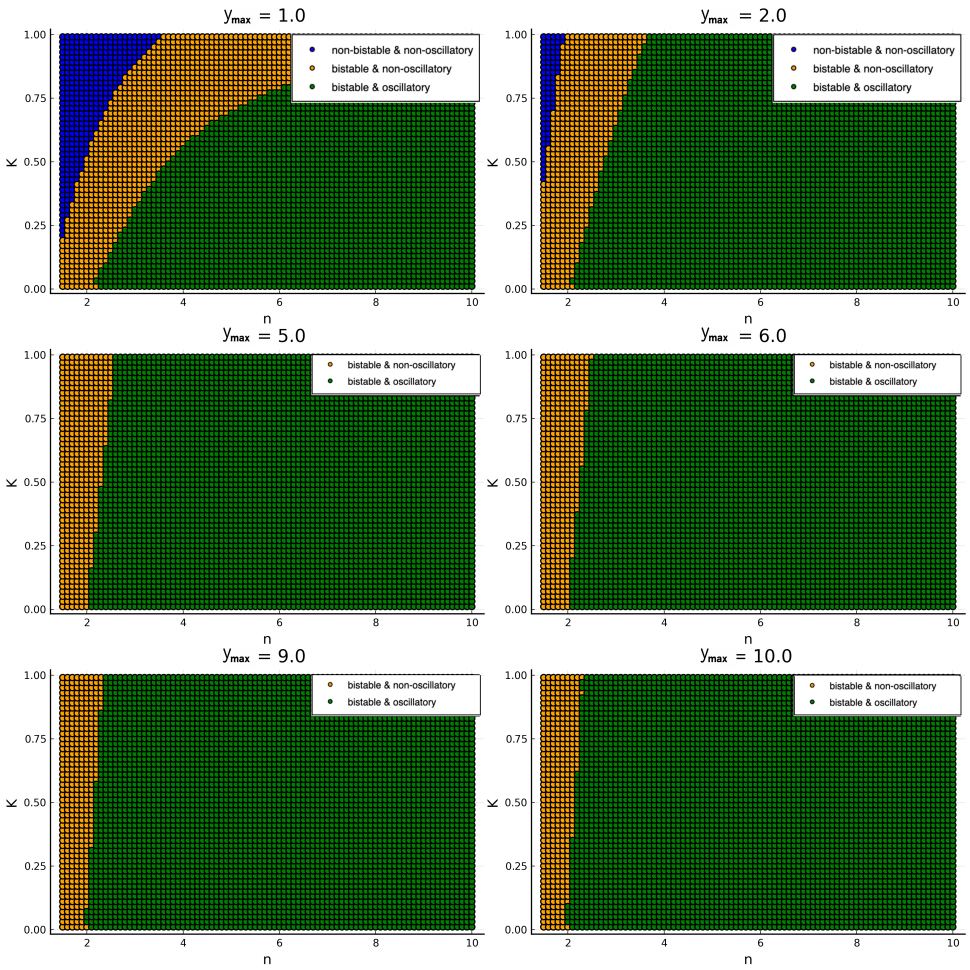
Supplementary Figure 2: **3D bifurcation plots**. Related to Figure 5. (A) The layered 3D scatter plot shows which parameters give rise to "not bistable and not oscillatiory" or "bistable and not oscillatory" systems. One can see a trend that as $y_{\max}$ goes up, the blue region becomes smaller and smaller. (B) This layered 3D scatter plot shows the parameter sets that correspond to "bistable and oscillatory". We notice that as $y_{\max}$ becomes higher, the corresponding region in the space becomes larger.

3 Dynamics at the transition.

In the main paper, Figures 9 and 10 show examples of the dynamics of the 2-bit and 3-bit counters. We indicate the external input pulses with green dots. However, due to the long relaxation times between consecutive pulses, the two green dots indicating the start and the end of a pulse can hardly be distinguished. Supplementary Figure 4 shows a zoom-in inset figure that clarifies the dynamics around the input pulse.

4 The N-bit counter ($N = 8$).

The scalability of a distributed system is an essential aspect when constructing larger circuits. We have shown systematically how to build a single bit counter, a two bit counter and a 3-bit counter in the main



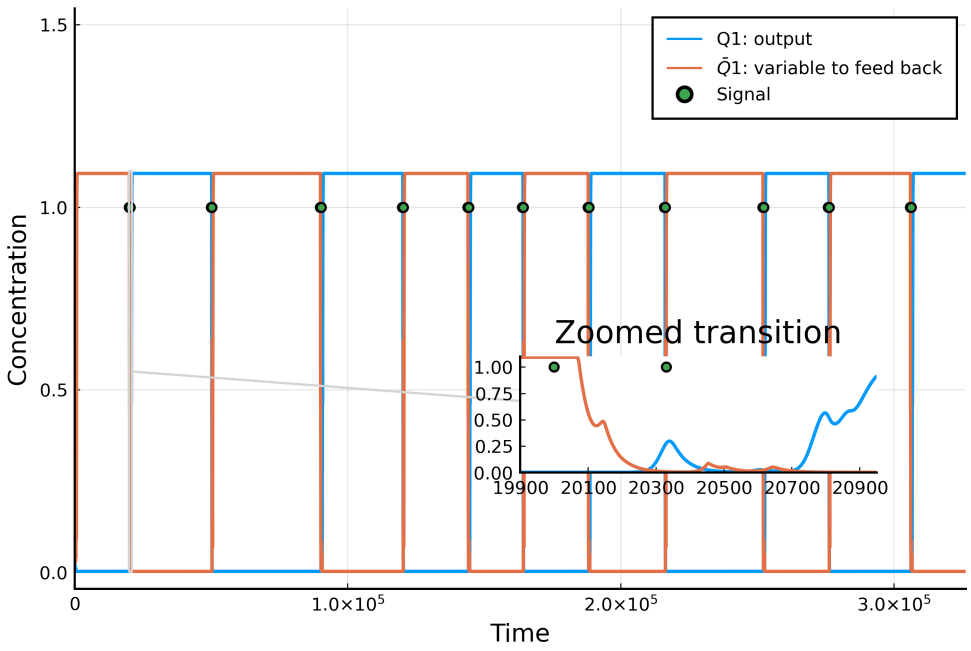
Supplementary Figure 3: **A detailed layer-by-layer plot of the 3D bifurcation plot**. Related to Figure 5.

paper. In order to demonestrate the scalability of the design, we design an 8-bit counter using the same principle. We show the simulation in Supplementary Figure 5 which demonstrates that all the bits switch as required.

5 Single-bit counter circuits implemented with seven unique gates in *E. coli*

In the main paper, we have shown an example of a single-bit counter design associated with an optimized range of the input signal duration δ. However, the Cello pipeline did not directly generate it. For our designed counter, Cello aims at generating the best candidate circuit with respect to several criteria. However, Cello does not take the range of δ into consideration. Here, we list seven feasible 1-bit counter circuits, each of which consists of seven unique repressors sampled from the *E.coli* experimental gate database.

Table 1 shows a comparison between the ranges of δ for these seven circuits. Each circuit is implemented with a unique set of seven gates sampled from the *E.coli* database. Circuit No. 1 in Table 1 was generated



Supplementary Figure 4: **Transition dynamics in the 1-bit counter**. Related to Figures 9 & 10. A inset plot for the dynamics in the interval $t \in [19900, 20900]$ is shown in the right lower corner. When zoomed in, one can clearly see that there are actually two green dots indicating the start and the end of the corresponding pulse.

using the modified Cell 2.0 pipeline. We then changed one gate at a time in circuit No. 1, and replaced it with a gate sampled from the remaining gate pool in the *E.coli* database. We extensively tested all 42 possible combinations of gate replacements to search for a feasible counter. This has resulted in only 7 feasible designs. Note that δ_{range} and δ_{cv} of circuit No. 4 are significantly higher than those of circuit No. 1. This is not surprising since Cello generates a feasible set of gate assignments, but does not optimize δ_{range}. Furthermore, to better visualize the distribution of δ, we show a box plot in Figure 6 for the seven circuits. Supplementary Figures 7-13 display the circuit plasmids, the gate assignments, and examples of the circuit dynamics with δ = 400 for each of the seven circuits.

6 Contour plots

In the main paper, Figure 16 shows a comparison between δ-mean and δ-std for both the 1-bit and the 2-bit counters. Here we show an alternative representation as contour plots in Figure 14. These plots allow one to see how the δ-mean and the δ-std change when the number of bits in the counter are increased.

References

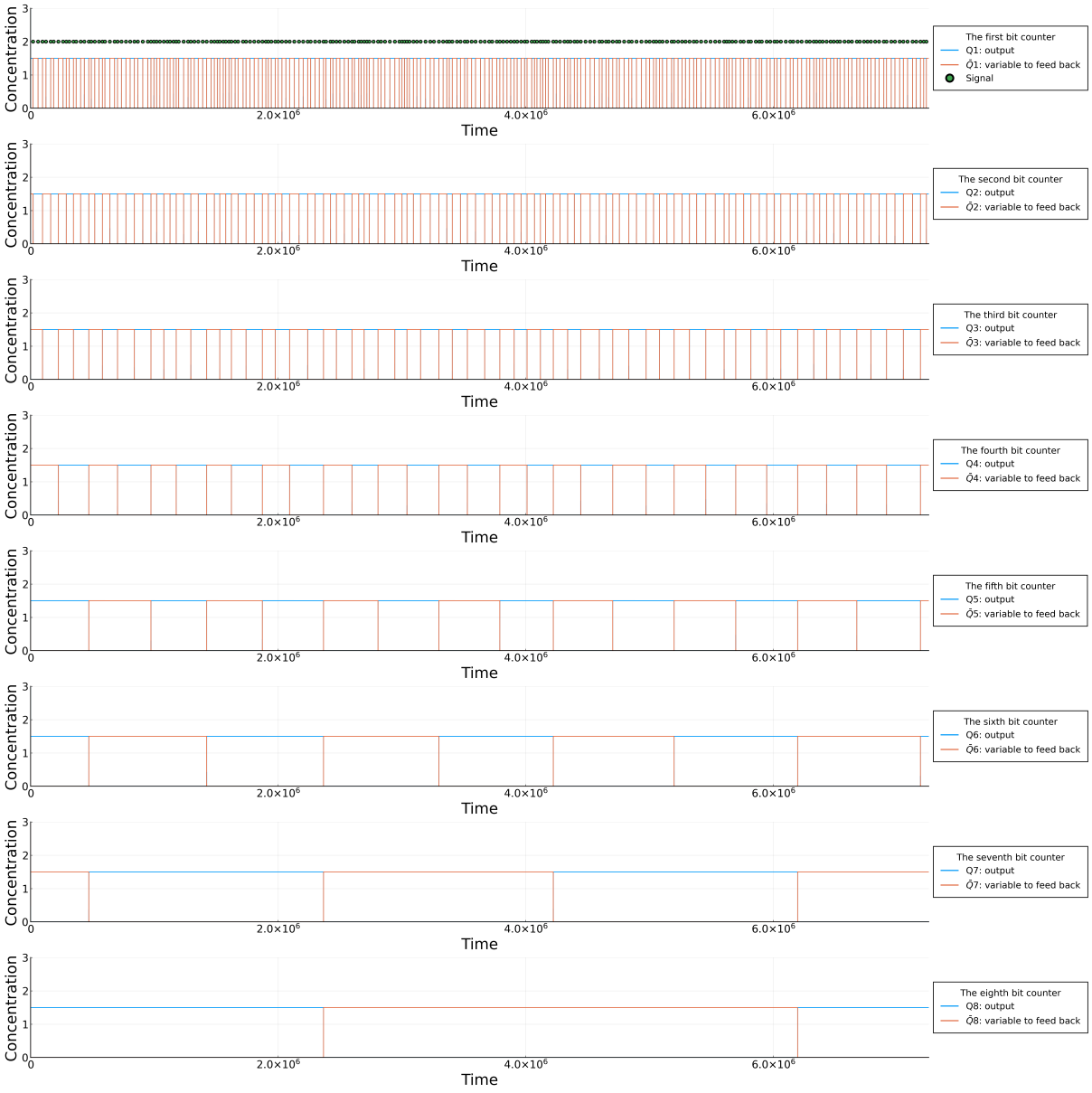
[1] Eduardo D Sontag. Monotone and near-monotone biochemical networks. *Systems and Synthetic Biology*, 1(2):59–87, 2007.

Circuit NO.	δ_{min}	δ_{max}	δ_{range}	δ_{cv}
1	375	460	85	0.184783
2	360	470	110	0.234043
3	325	505	180	0.356436
4	300	550	250	0.454545
5	385	455	70	0.153846
6	320	515	195	0.378641
7	345	490	145	0.295918

Table 1: Comparison between the ranges of δ for the seven single-bit counter circuits. Each circuit is implemented with a unique set of seven gates from the *E.coli* database. δ_{min} is the minimum value of δ to produce a feasible 1-bit counter, while δ_{max} is the maximum value of δ that allows for building a feasible 1-bit counter. δ_{range} is the difference between δ_{max} and δ_{min}. δ_{cv} tells the percentage of the coverage for the input signal duration within the counter's maximum allowed δ range.

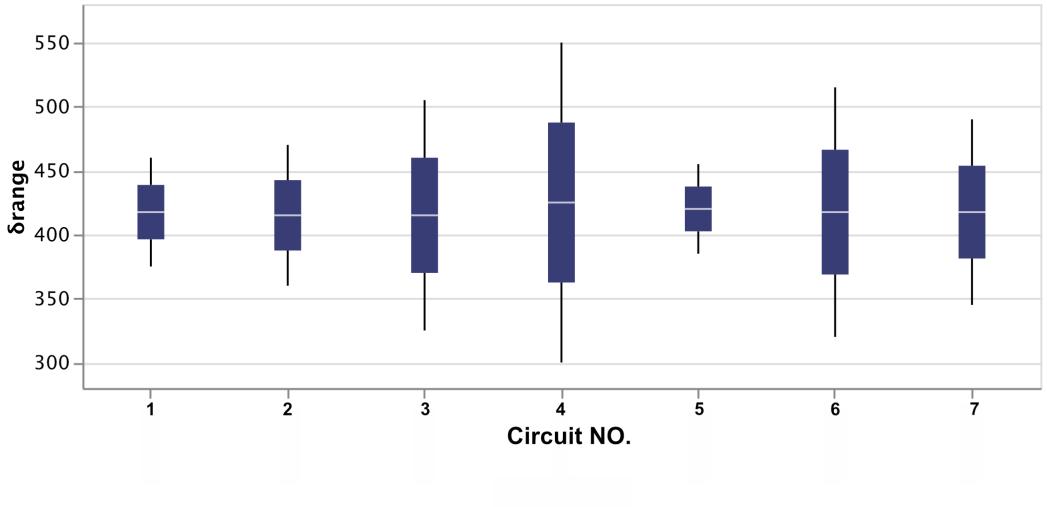
Circuit NO.	Gate1	Gate2	Gate3	Gate4	Gate5	Gate6	Gate7
1	H1_HlyIIR	N1_LmrA	S4_SrpR	B3_BM3R1	P1_PhlF	R1_PsrA	E1_BetI
2	H1_HlyIIR	F1_AmeR	S4_SrpR	B3_BM3R1	P1_PhlF	R1_PsrA	E1_BetI
3	H1_HlyIIR	N1_LmrA	S4_SrpR	B3_BM3R1	Q1_QacR	R1_PsrA	E1_BetI
4	Q2_QacR	N1_LmrA	S4_SrpR	B3_BM3R1	P1_PhlF	R1_PsrA	E1_BetI
5	H1_HlyIIR	N1_LmrA	S4_SrpR	B3_BM3R1	P1_PhlF	R1_PsrA	Q2_QacR
6	A1_AmtR	N1_LmrA	S4_SrpR	B3_BM3R1	P1_PhlF	R1_PsrA	E1_BetI
7	L1_LitR	N1_LmrA	S4_SrpR	B3_BM3R1	P1_PhlF	R1_PsrA	E1_BetI

Table 2: The gate assignments for the seven circuits. To match to Cello 2.0 style, we have concatenated the associated RBS name (the first 2 letters of the gate name) with each gate name as a whole.

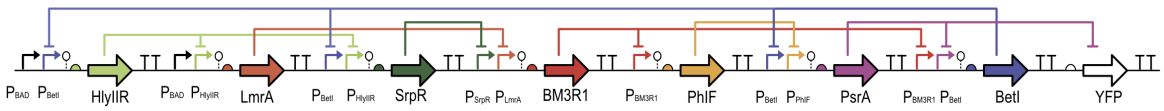


(A) 8-bit counter circuit dynamics

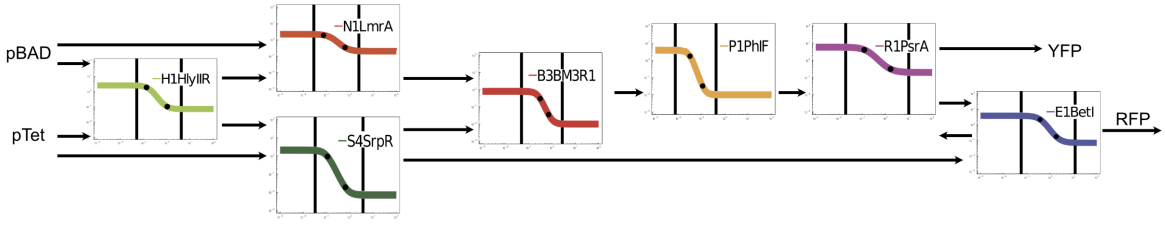
Supplementary Figure 5: **Simulation of the dynamics of an 8-bit counter**. Related to Figure 6. The bits are ordered from the least significant bit to the most significant bit. The top panel is the first bit and the green dots indicate the input signals. The parameters are: the scaling factor ξ = 0.025, the degradation rate $\gamma = 0.025$, the equilibrium constant $K = 0.081$, the cooperativity coefficient $n = 2.81$, the duration of external signal $\delta = 270$, the amplitude of the external signal $A = 20$, the shifted hill coefficient maximum value $y_{max} = 1.5$, the shifted hill coefficient minimum value $y_{min} = 0.002$, and the initial and between signals relaxation times $\Delta = 20000$. Note that the pulses are applied at random non-uniform intervals, which represents an asynchronous counting situation. However, the spacing between the bits looks more uniform for the more significant bits. This can be explained as follows. Suppose that the pulses are separated by random independent and identically distributed inter-arrival times; by the central limit theorem, the net effect of N pulses will be distributed with a Gaussian distribution that has a variance which is proportional to $1/\sqrt{N}$.



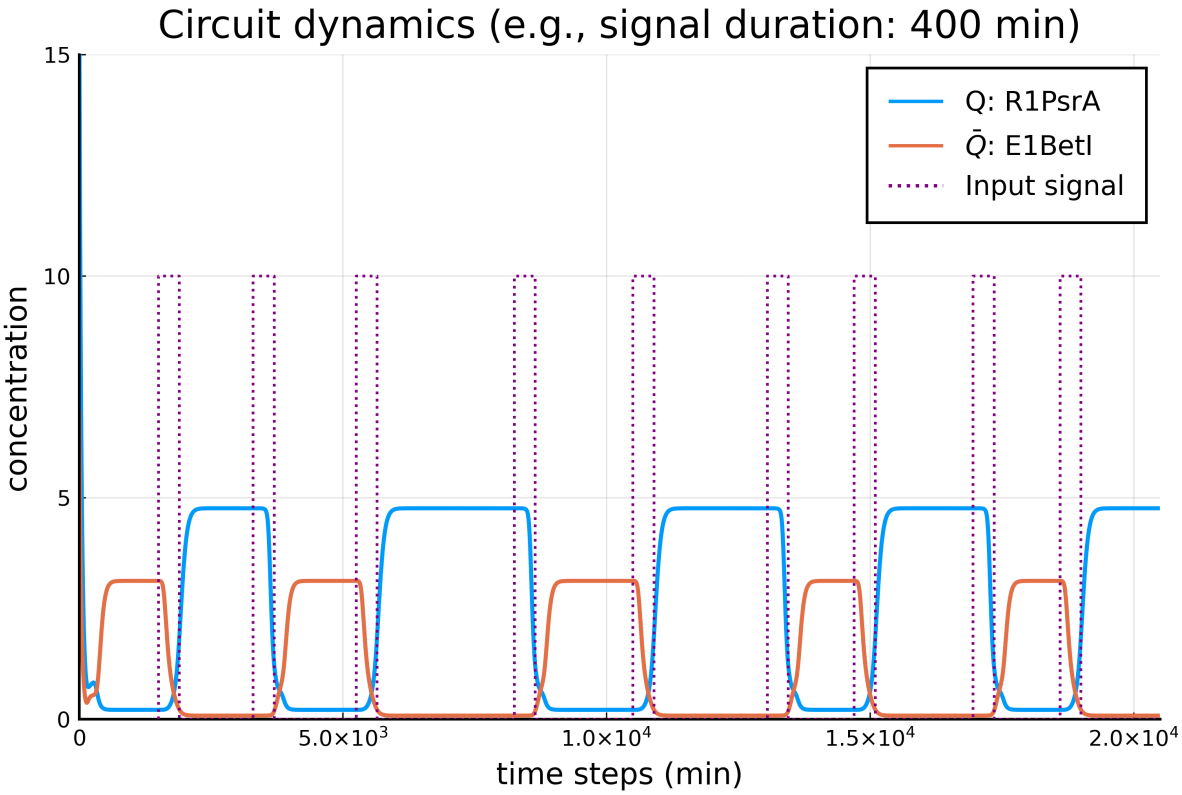
Supplementary Figure 6: **The distribution and the feasible ranges of δ for all the seven 1-bit counter circuits**. Related to Figure 2 & 15. Note that circuit No. 4 has the largest range of δ.



(A) The 1st 1-bit counter circuit plasmid design

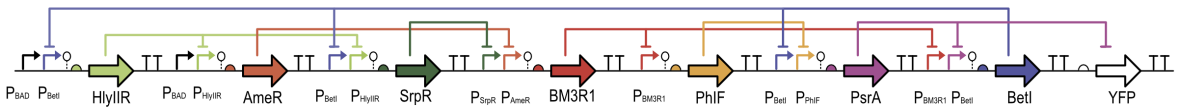


(B) The 1st 1bit counter circuit gate assignments

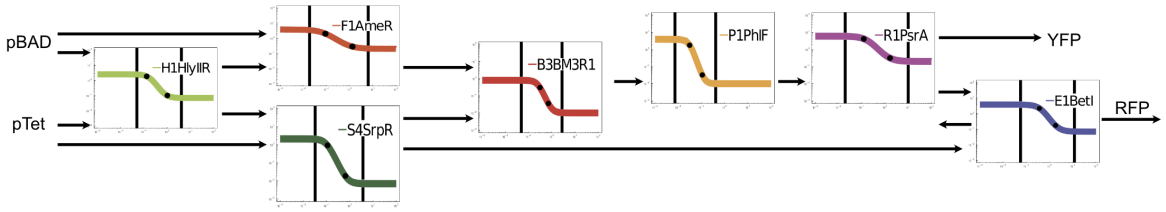


(C) The 1st 1-bit counter circuit dynamics

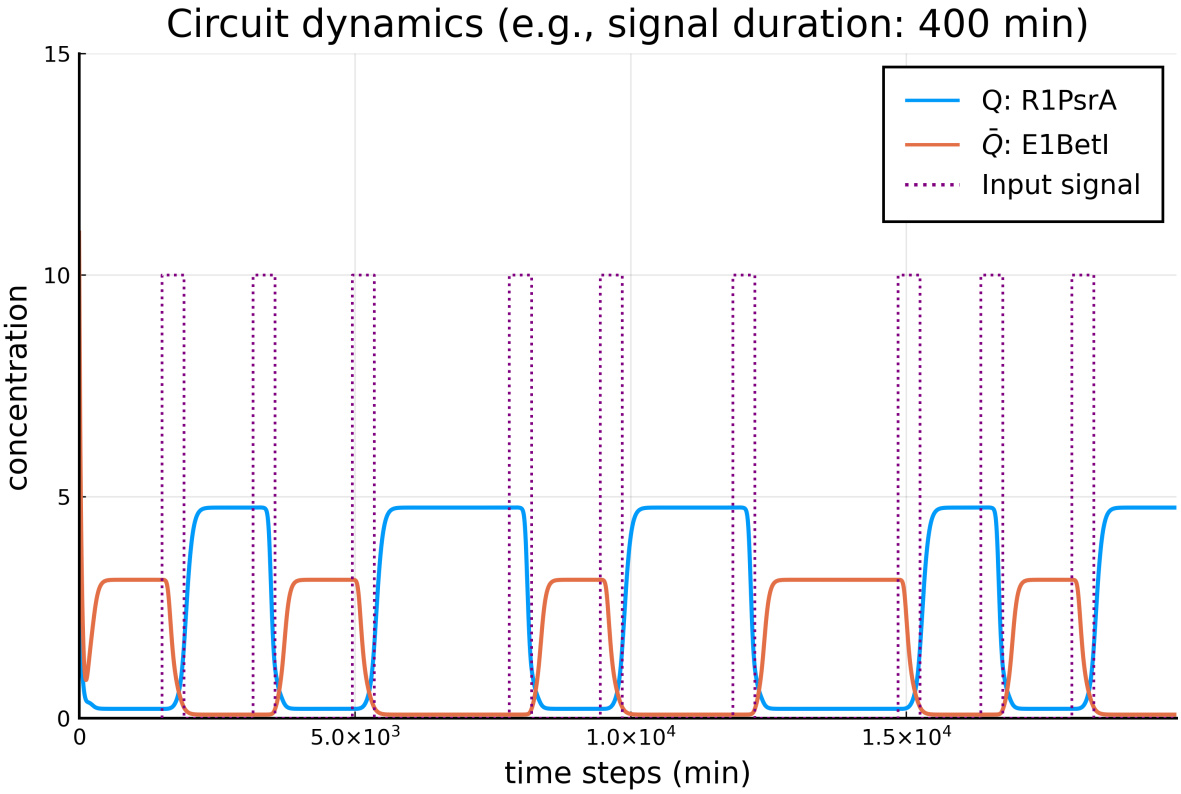
Supplementary Figure 7: Related to Figure 2 & 15. The first 1-bit counter circuit with 7 unique experimental gates. This specific design is the output from the Cello 2.0 pipeline. (A) The circuit plasmid design. (B) The gate assignments for the associated plasmid in (A). (C) An example of the counter dynamics with $\delta = 400$.



(A) The 2nd 1-bit counter circuit plasmid design

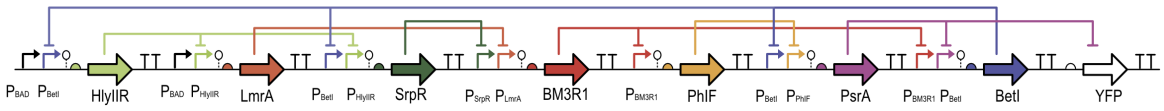


(B) The 2nd 1-bit counter gate assignments

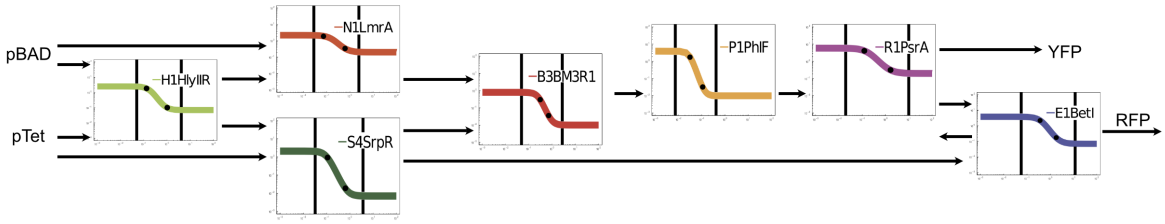


(C) The 2nd 1-bit counter circuit dynamics

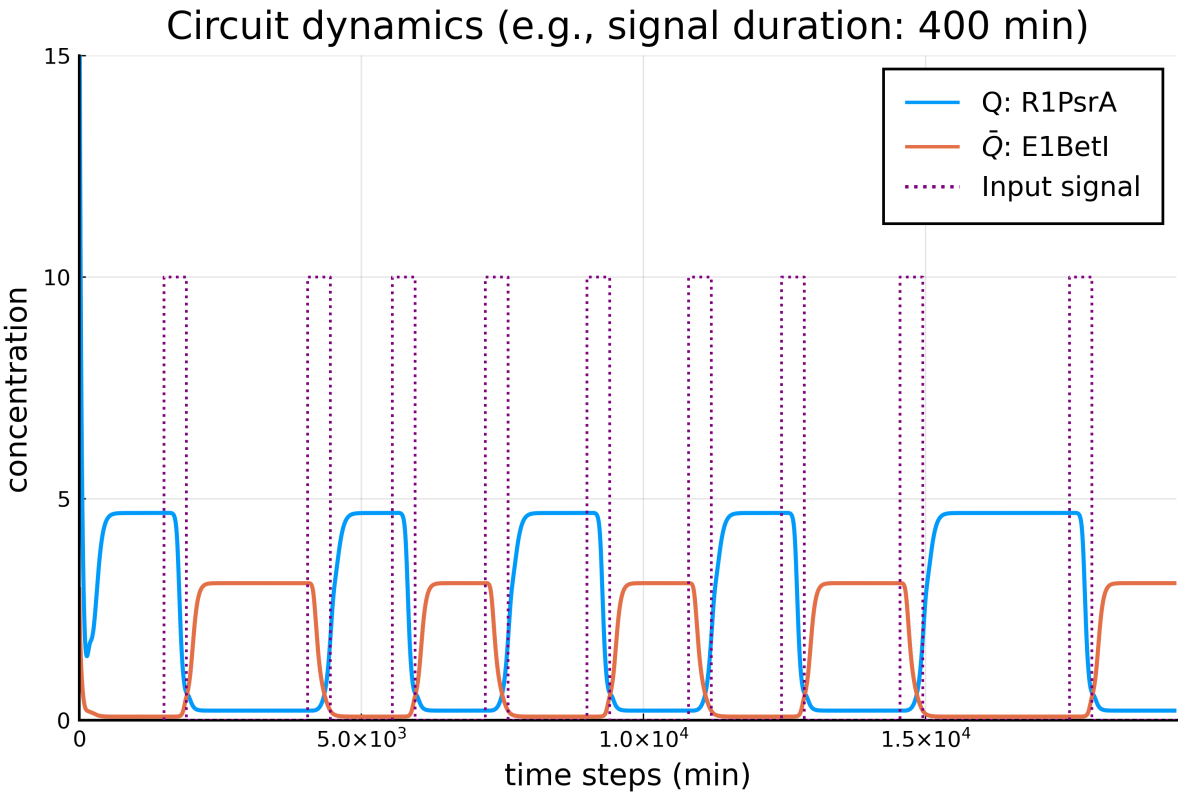
Supplementary Figure 8: Related to Figure 2 & 15. The second 1-bit counter circuit with seven unique experimental gates. (A) The circuit plasmid design. (B) The gate assignments for the associated plasmid in (A). (C) An example of the counter dynamics with $\delta = 400$.



(A) The 3rd 1-bit counter circuit plasmid design

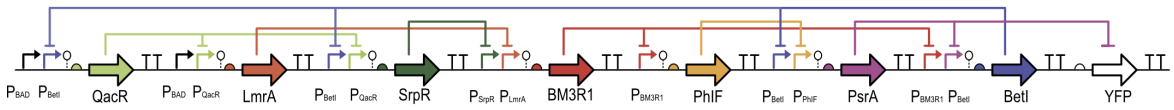


(B) The 3rd 1-bit counter circuit gate assignment

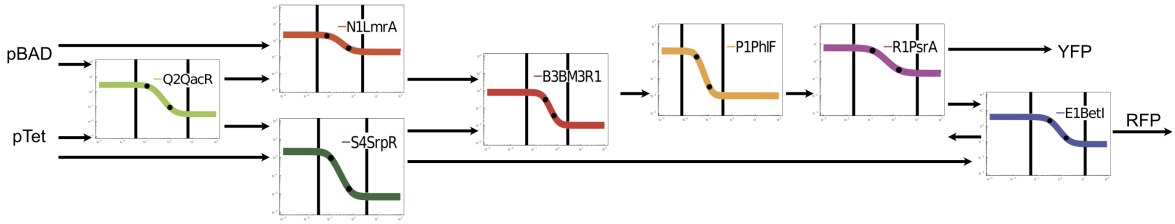


(C) The 3rd 1-bit counter circuit dynamics

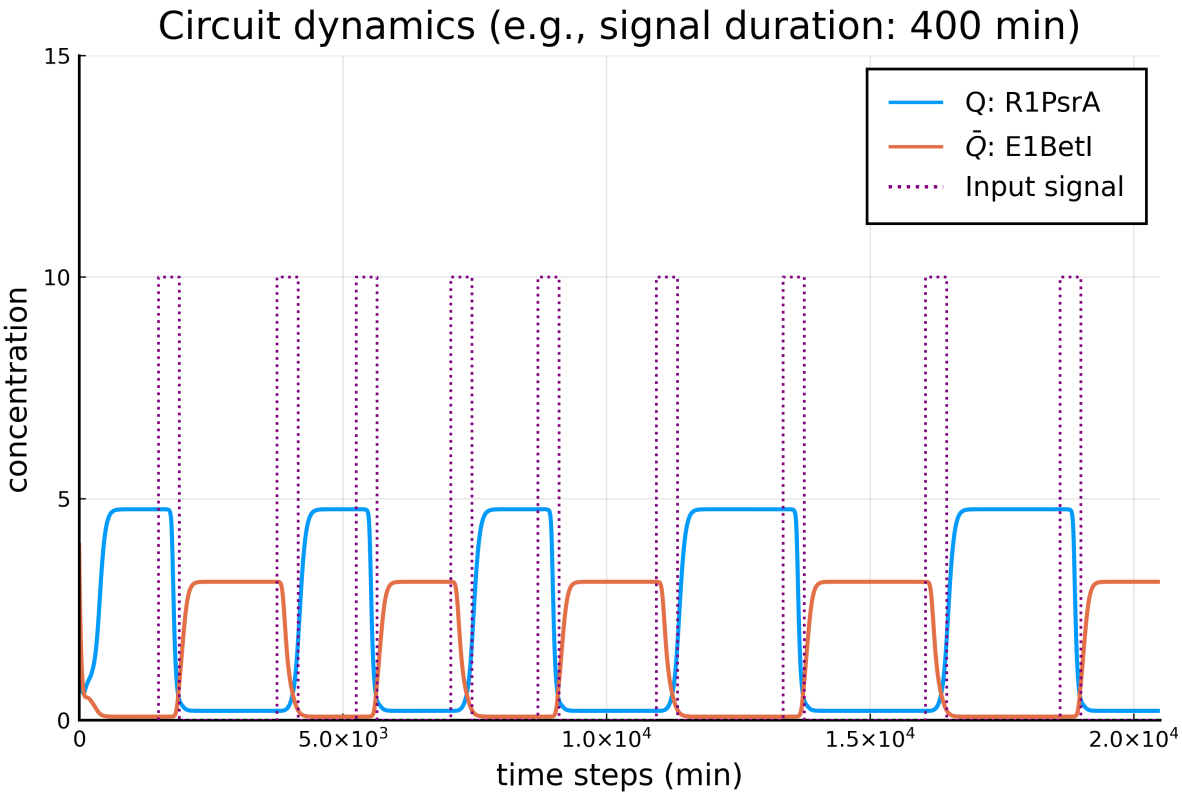
Supplementary Figure 9: Related to Figure 2 & 15. The third 1-bit counter circuit with seven unique experimental gates. (A) The circuit plasmid design. (B) The gate assignments for the associated plasmid in (A). (C) An example of the counter dynamics with $\delta = 400$.



(A) The 4th 1-bit counter circuit plasmid design

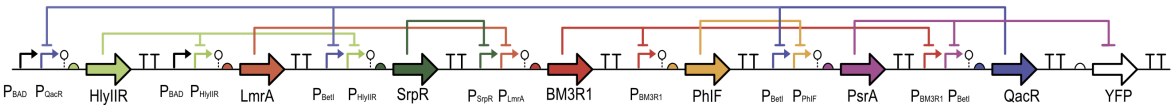


(B) The 4th 1-bit counter circuit gate assignment

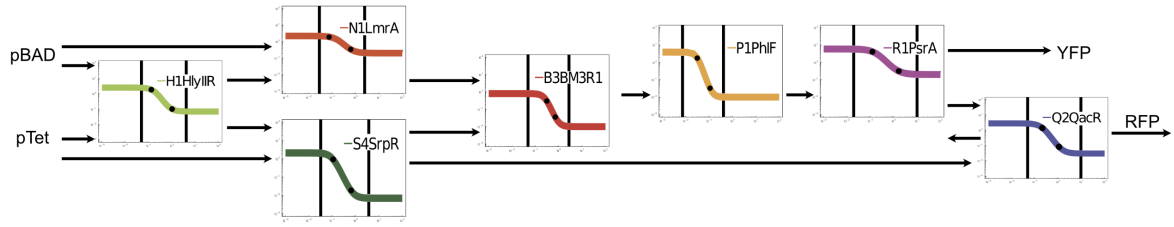


(C) The 4th 1-bit counter circuit dynamics

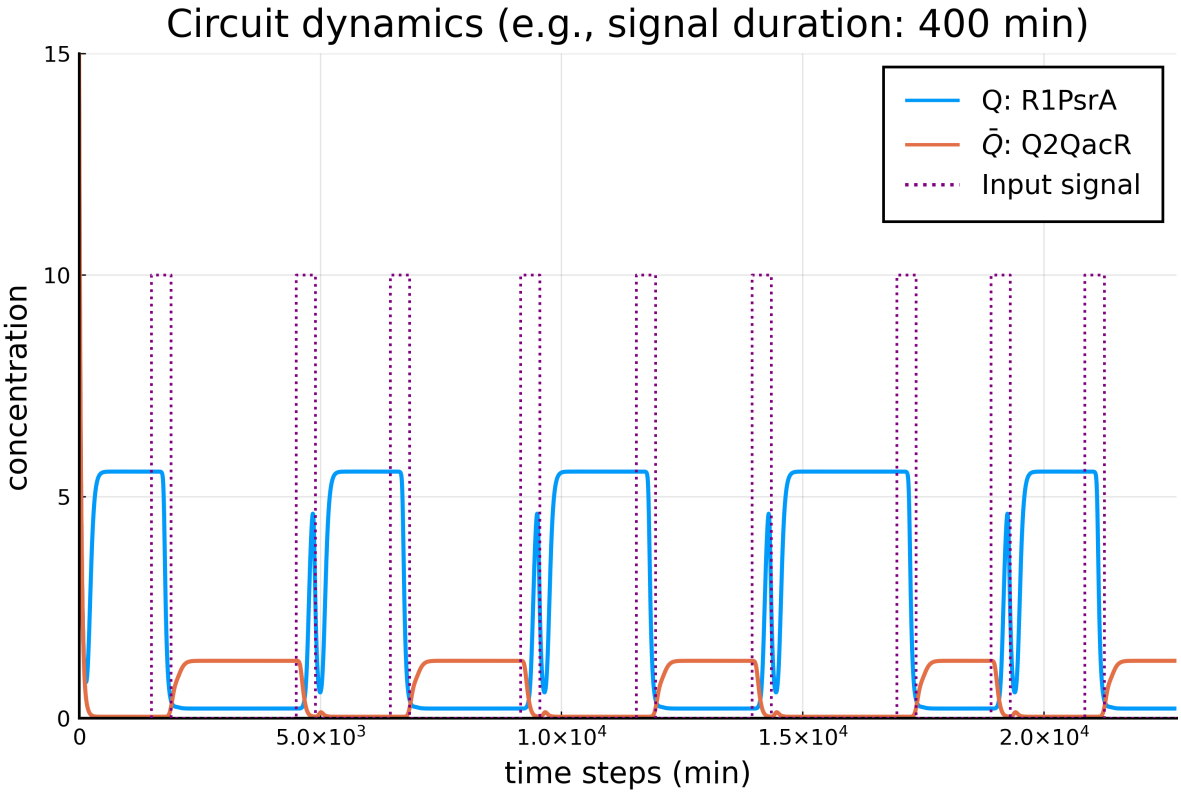
Supplementary Figure 10: Related to Figure 2 & 15. The fourth 1-bit counter circuit with seven unique experimental gates. (A) The circuit plasmid design. (B) The gate assignments for the associated plasmid in (A). (C) An example of the counter dynamics with $\delta = 400$.



(A) The 5th 1-bit counter circuit plasmid design

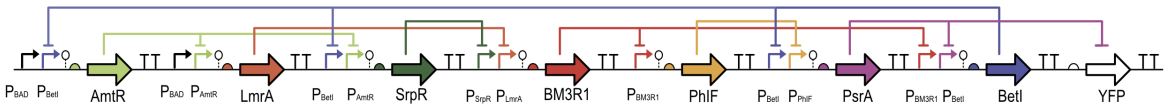


(B) The 5th 1-bit counter circuit gate assignment

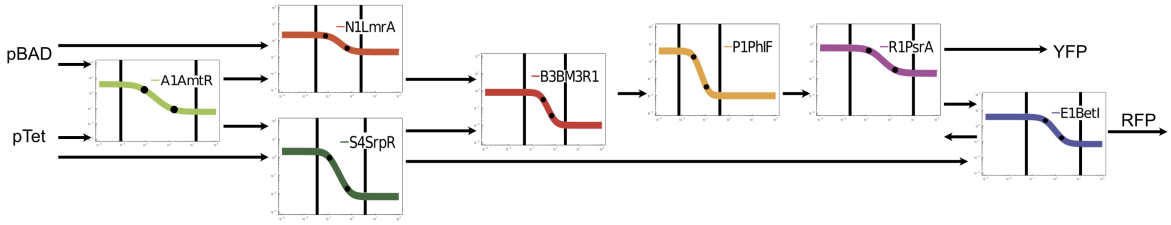


(C) The 5th 1-bit counter circuit dynamics

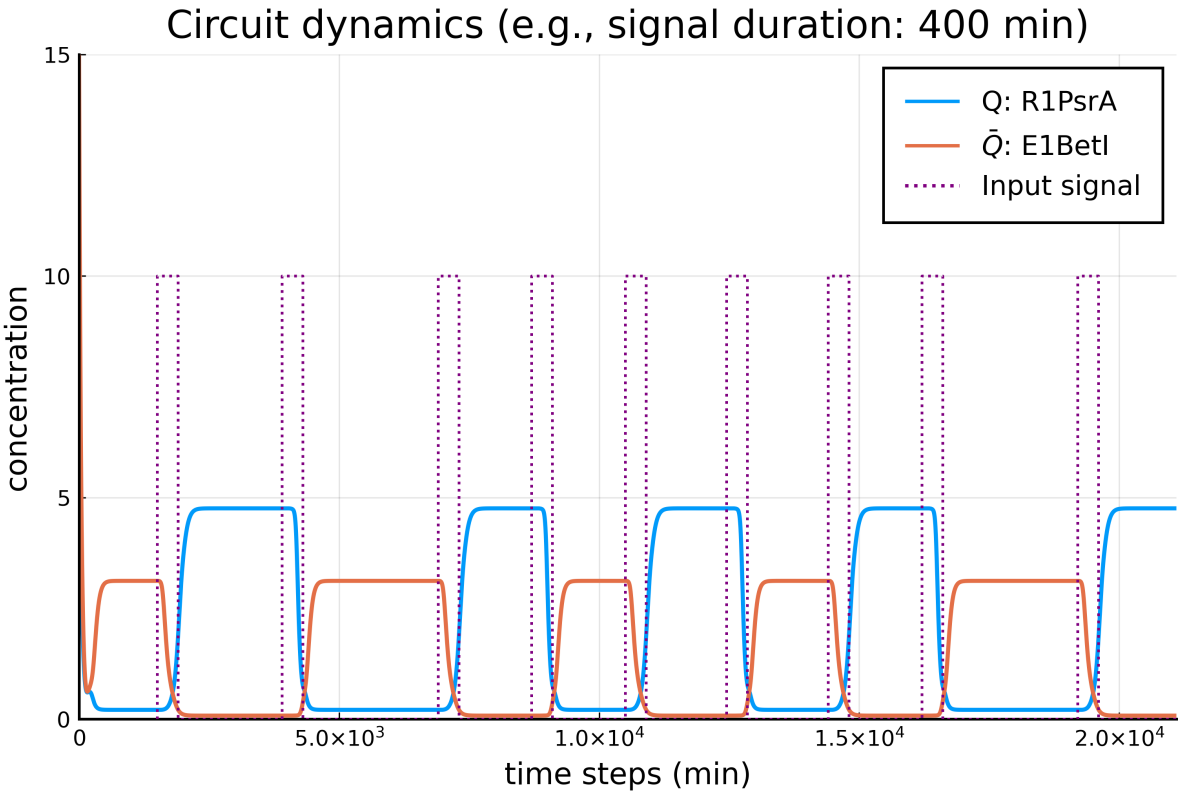
Supplementary Figure 11: Related to Figure 2 & 15. The fifth 1-bit counter circuit with seven unique experimental gates. (A) The circuit plasmid design. (B) The gate assignments for the associated plasmid in (A). (C) An example of the counter dynamics with $\delta = 400$.



(A) The 6th 1-bit counter circuit plasmid design

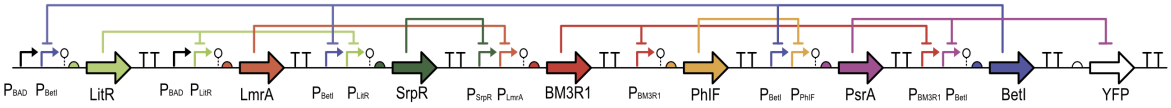


(B) The 6th 1-bit counter circuit gate assignment

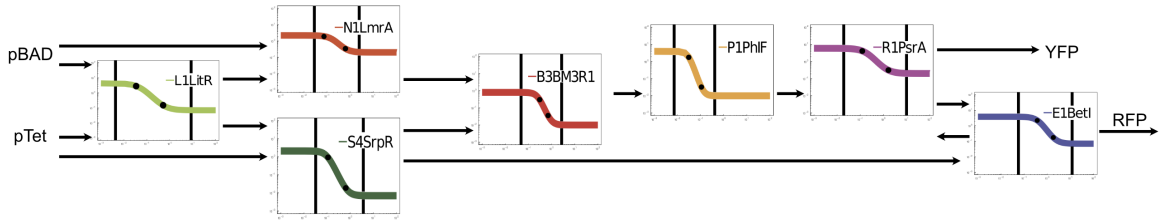


(C) The 6th 1-bit counter circuit dynamics

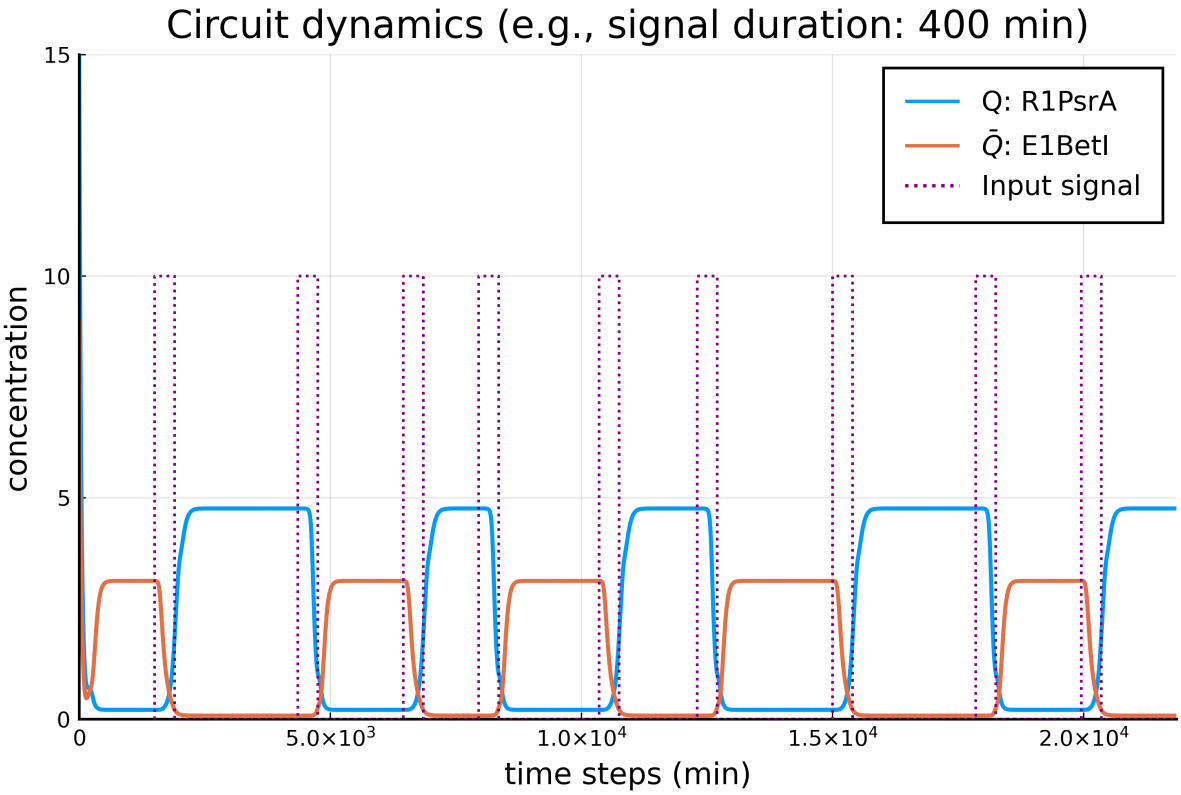
Supplementary Figure 12: Related to Figure 2 & 15. The sixth 1-bit counter circuit with seven unique experimental gates. (A) The circuit plasmid design. (B) The gate assignments for the associated plasmid in (A). (C) An example of the counter dynamics with $\delta = 400$.



(A) The 7th 1-bit counter circuit plasmid design

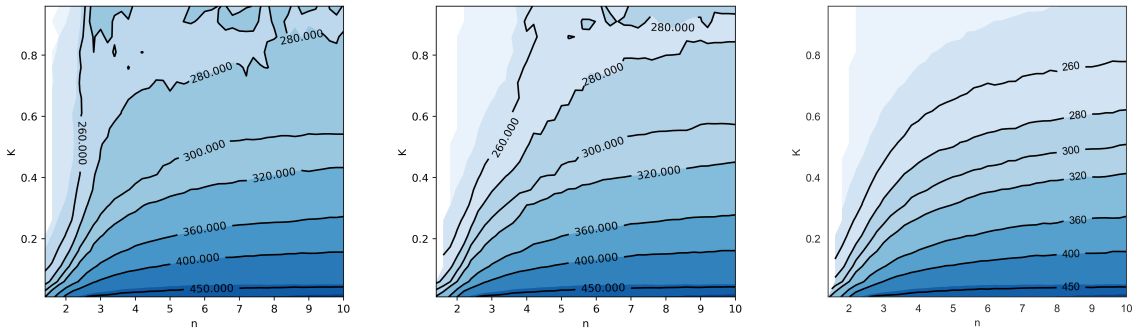


(B) The 7th 1-bit counter circuit gate assignment

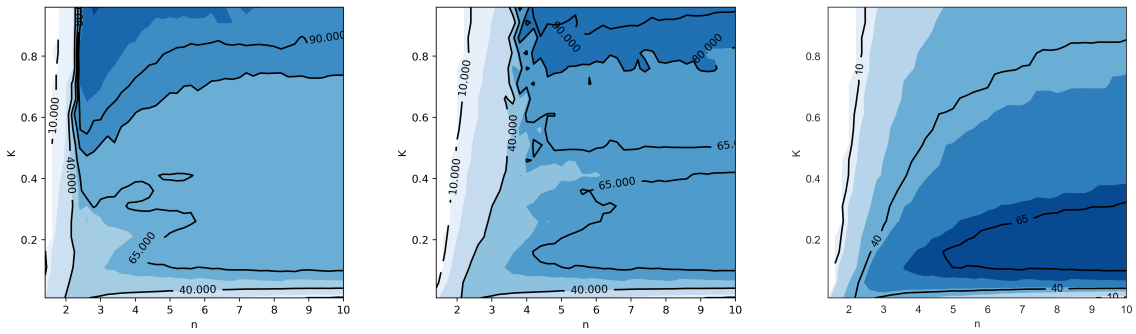


(C) The 7th 1-bit counter circuit dynamics

Supplementary Figure 13: Related to Figure 2 & 15. The seventh 1-bit counter circuit with seven unique experimental gates. (A) The circuit plasmid design. (B) The gate assignments for the associated plasmid in (A). (C) An example of the counter dynamics with $\delta = 400$.



(A) 1-bit counter δ mean (B) 2-bit counter δ mean (C) 3-bit counter δ mean



(D) 1-bit counter δ std (E) 2-bit counter δ std (F) 3-bit counter δ std

Supplementary Figure 14: Contour plots of δ-mean and δ-std comparing between 1-bit, 2-bit, and 3-bit counters. Related to Figure 12 & 13. The 1st row shows the plots for δ-mean, and the 2nd row shows the plots for δ-std.