Supplementary Material

1. System Test and Validation

Before using the Piphys system to record neural spikes, it was tested by a standard synthetic waveform for hours. The system performance was analyzed. Figure S1a shows the recording from a 500 Hz 3 mV peak-to-peak sine wave. The power spectral density is averaged over the 32 channels. Figure S1b shows the power spectral density of the recorded signal has the frequency components with a peak at 500 Hz. Both time series and power spectral density prove the system is capable of recording real-world signals. Since the Raspberry Pi is not a perfect hard real-time device, clock issue will be discussed in the following sections.

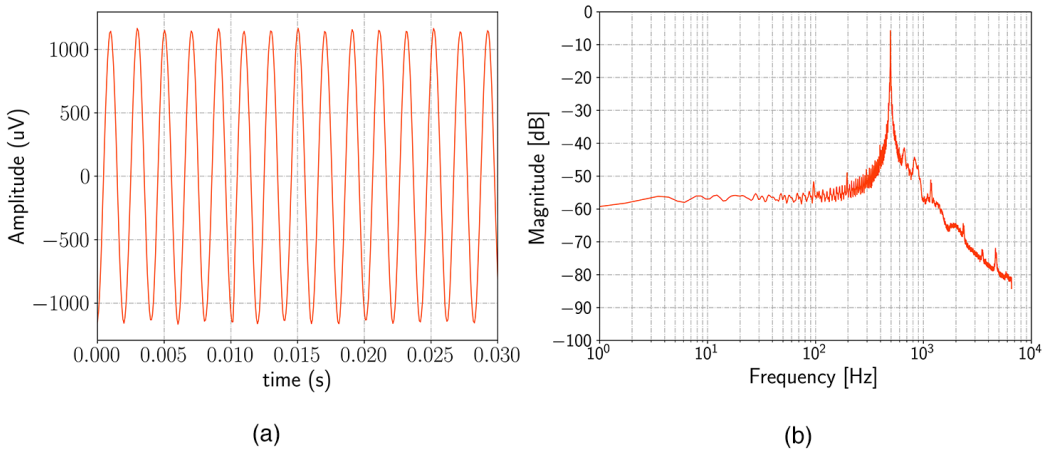


Figure S1. Recording of a sine wave using Piphys system. Signal source is a 500 Hz 3 mV peak-to-peak sinusoid wave. (a) Result in time series. The recorded signal has a peak-to-peak voltage around 2.6 mV. (b) Power spectral density of the result.

The Intan RHD bio-amplifier supports various sample rates to accommodate different experiment requirements. Sampling on the bio-amplifier needs to be driven by the SPI clock on Raspberry Pi. The speed of the required SPI clock ($SCLK_r$) can be calculated by equation 1, where 16 is the bit length for each data point, and 32 is the number of recording channels. In the hardware, Raspberry Pi's SPI clock ($SCLK_{g)}$ is generated by dividing the core clock, as shown in equation 2. The core clock frequency for Raspberry Pi 3 is set to 400 MHz. According to the BCM2835 ARM peripherals

datasheet, the divider must be a multiple of 2. However, the C library‡ used to generate the low level signal sets the divider to a power of 2. Clock jitter was measured by recording a continuous 50 Hz triangular wave in all channels with each sample rate. The average jitter rate is 0.067%. This jitter that happens during the recording is shown in Figure **??**. No evidence shows that the jitter rate correlates with the sample rate.

$$\mathrm{SCLK_r} = 16 \times 32 \times \text{sample rate} \tag{1}$$

$$\mathrm{SCLK_g} = \text{Core Clock/ CDIV} \tag{2}$$

In this case, it is hard for the Raspberry Pi to generate those preferred sample rate as shown in table S1. Instead, Raspberry Pi converts the speed parameter to equivalent SPI clock divider, giving the nearest clock rate. Since the intan bio-amplifier is a passive SPI slave device, it samples the analog signal with the clock from the host board. To compensate the overhead from task scheduling, the program is set to have the highest priority that takes two CPUs out of four while running. Due to the overhead and clock jitter, the sample rate shown in the table are averaged among seven tests and errors are calculated. Considering this unstableness of SPI clock, the sample rate with each chunk of Redis data are paired for dashboard visualization. Figure S2 is plotted based on the preferred sample rates and the generated sample rates. When analyzing the recorded data, the real sample rate should be used.

Preferred sample rate (Hz)	2000	3000	5000	6250	10000	12500	15000
Generated Sample Rate (Hz)	2716	3814	5767	6614	11103	13393	16039
Standard Deviation	11.01	20.18	21.03	17.73	74.26	107.41	178.48
Coefficient of Variance (%)	0.41	0.53	0.36	0.27	0.67	0.8	1.11

Table S1. Preferred sample rates and generated sample rates comparison.The generated sample rates are averaged from 7 tests with standard deviation and coefficient of variance calculated.

Knowing the intrinsic clock characteristic of Raspberry Pi, we plan to replace the hardware SPI interface with a FPGA chip that can generate precise clock pulses at desired frequency. As mentioned in Discussion section, the FPGA will be used to sample the intan bio-amplifier, and the Raspberry Pi will be in charge of data buffering with FPGA and IoT.

‡ https://www.airspayce.com/mikem/bcm2835/

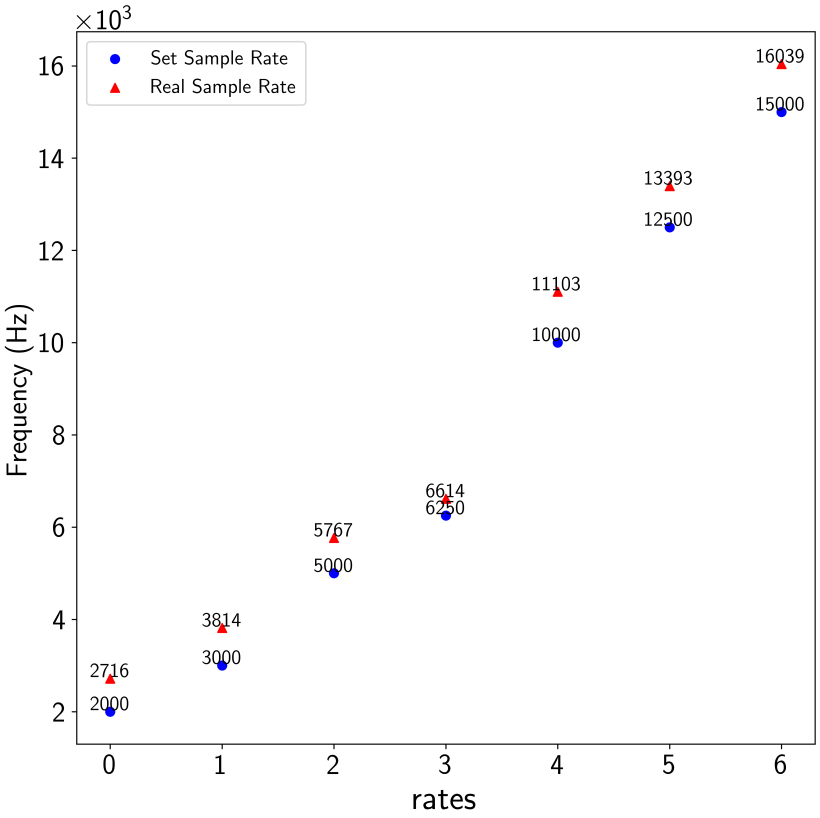


Figure S2. Desired sample rate (Set Sample Rate) and the actually generated sample rate (Real Sample Rate) from SPI clock.

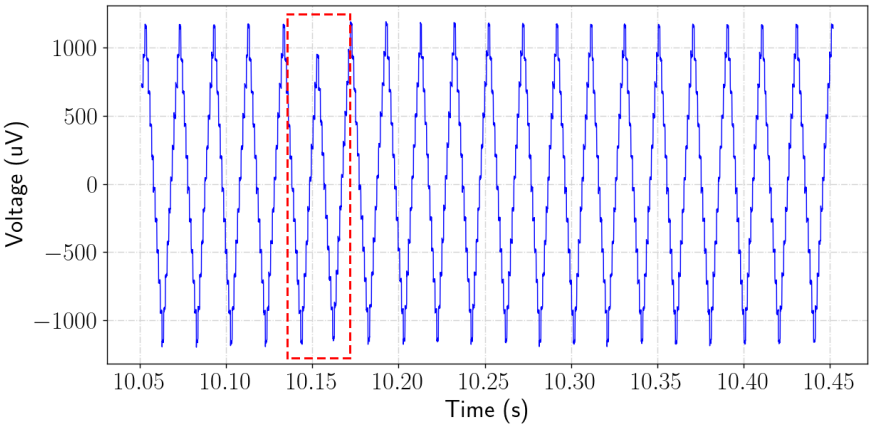
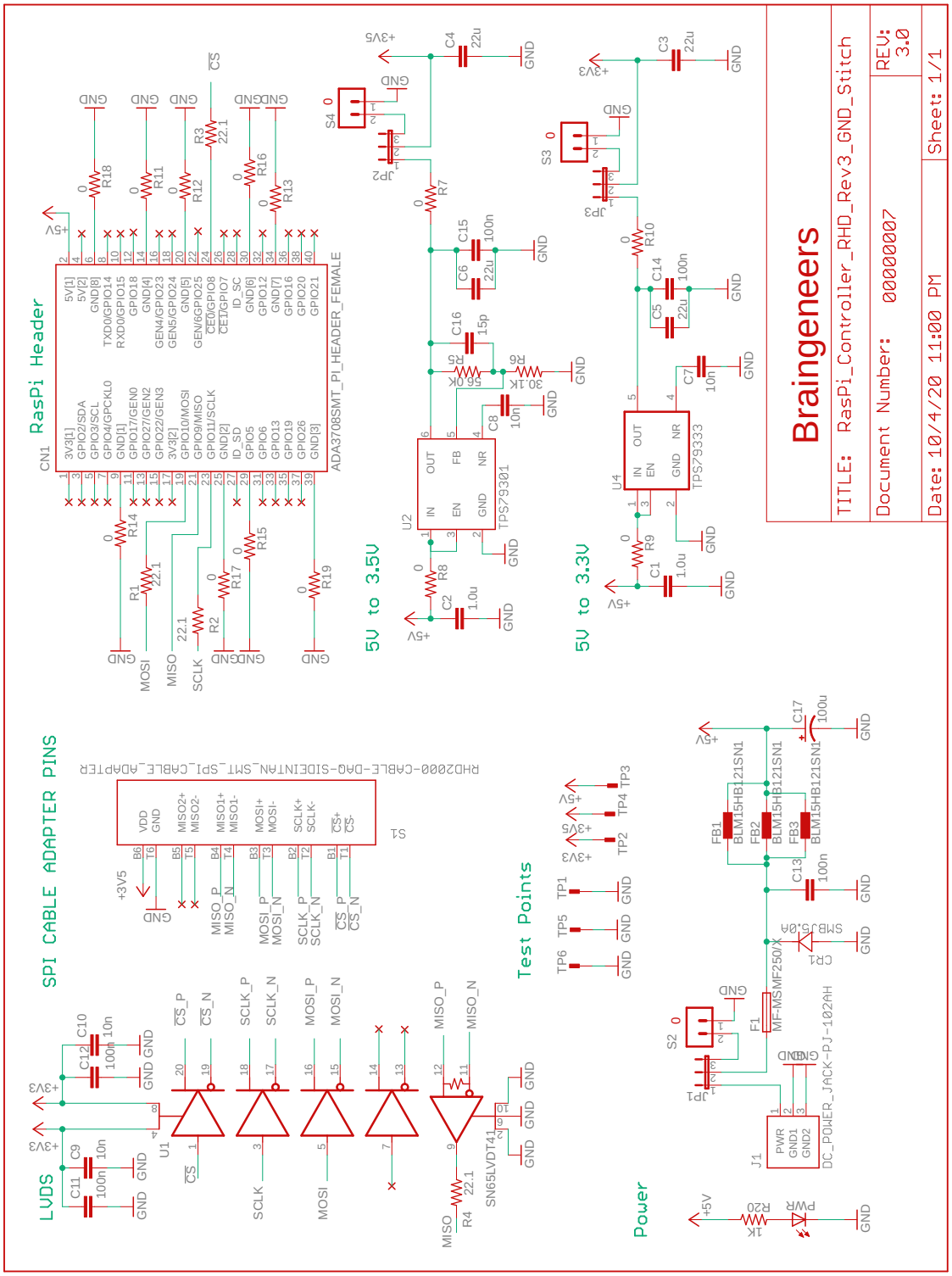
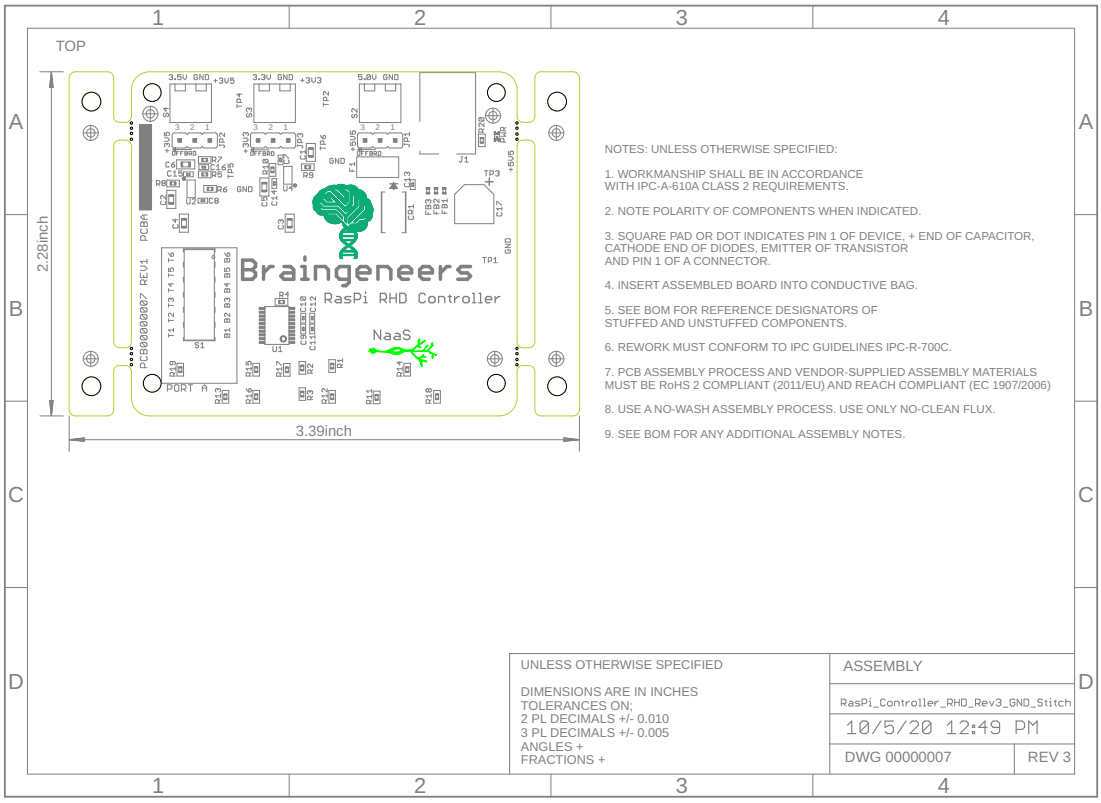


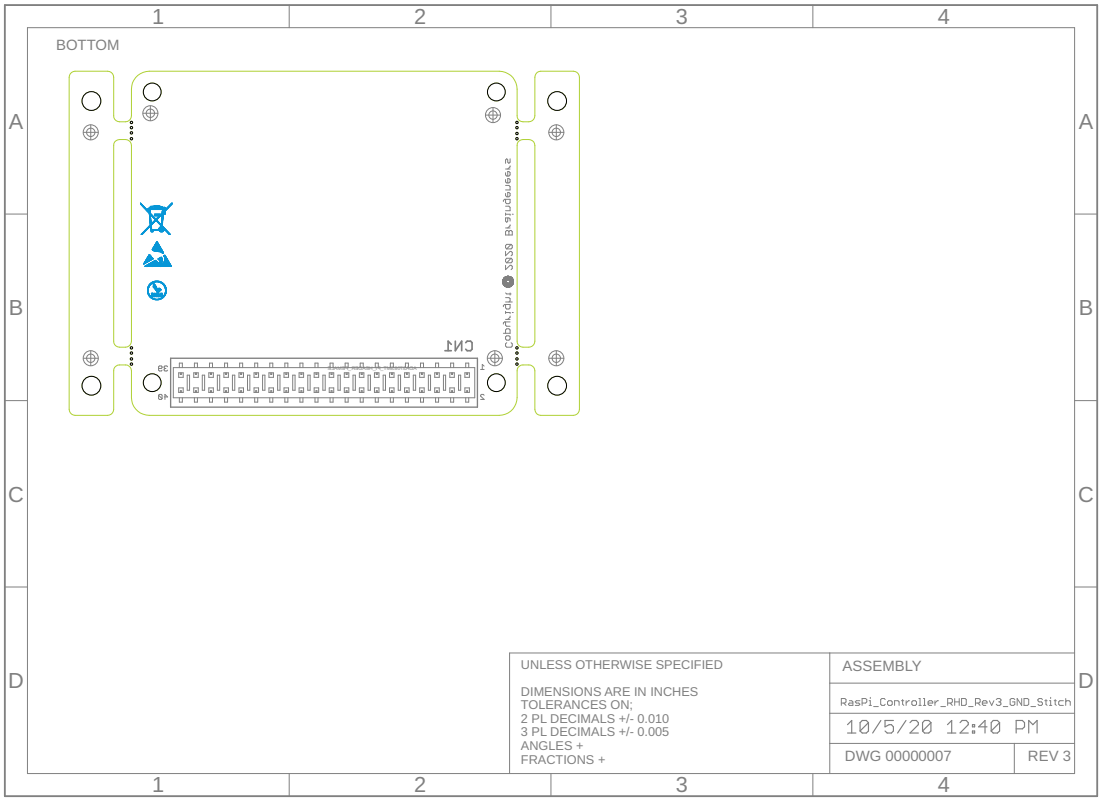
Figure S3. Recording result from 50 Hz, 3 mV peak-to-peak triangular wave shows a clock jitter (red square box). All seven sample rates are tested. The average jitter rate is 0.067%. The original signal is from the White Matter signal generator with a sampling rate of 1000 Hz. Result in the figure is sampled at 13255. Because the sample rate of the device is higher than the generator, each point of the original signal is sampled multiple times during recording, thus showing the staircase effect.

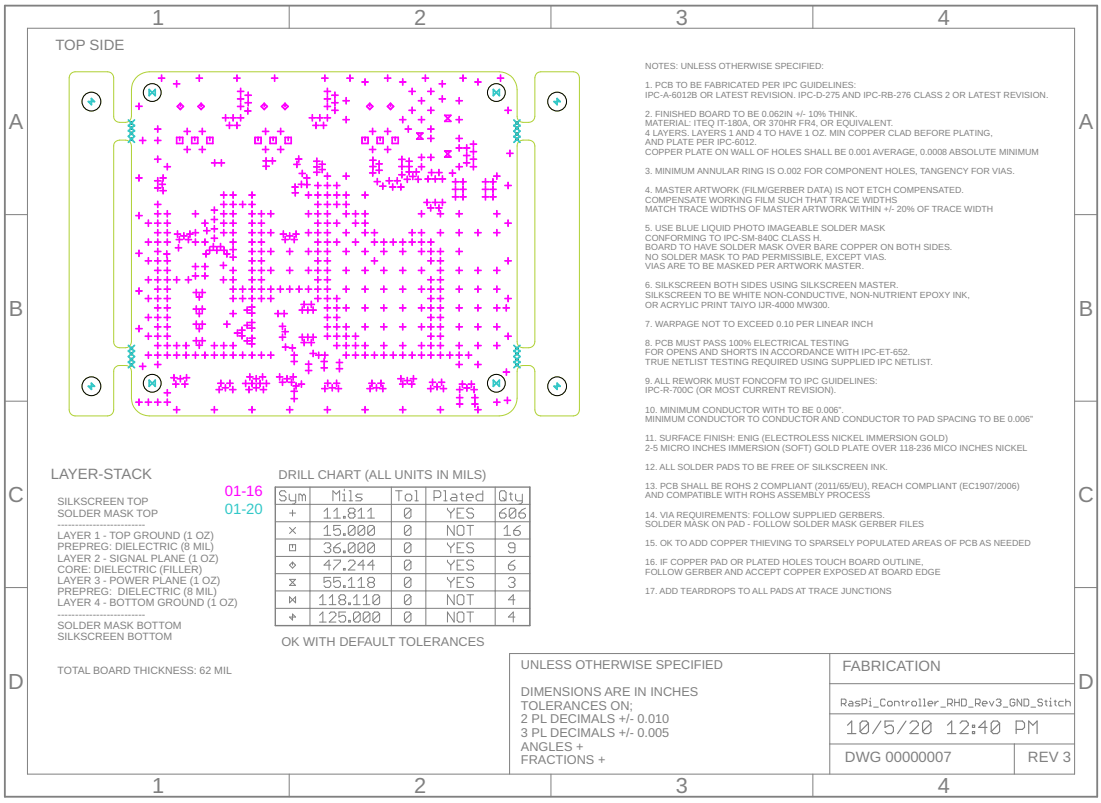
2. Hardware Schematics and Layouts

2.1. Piphys

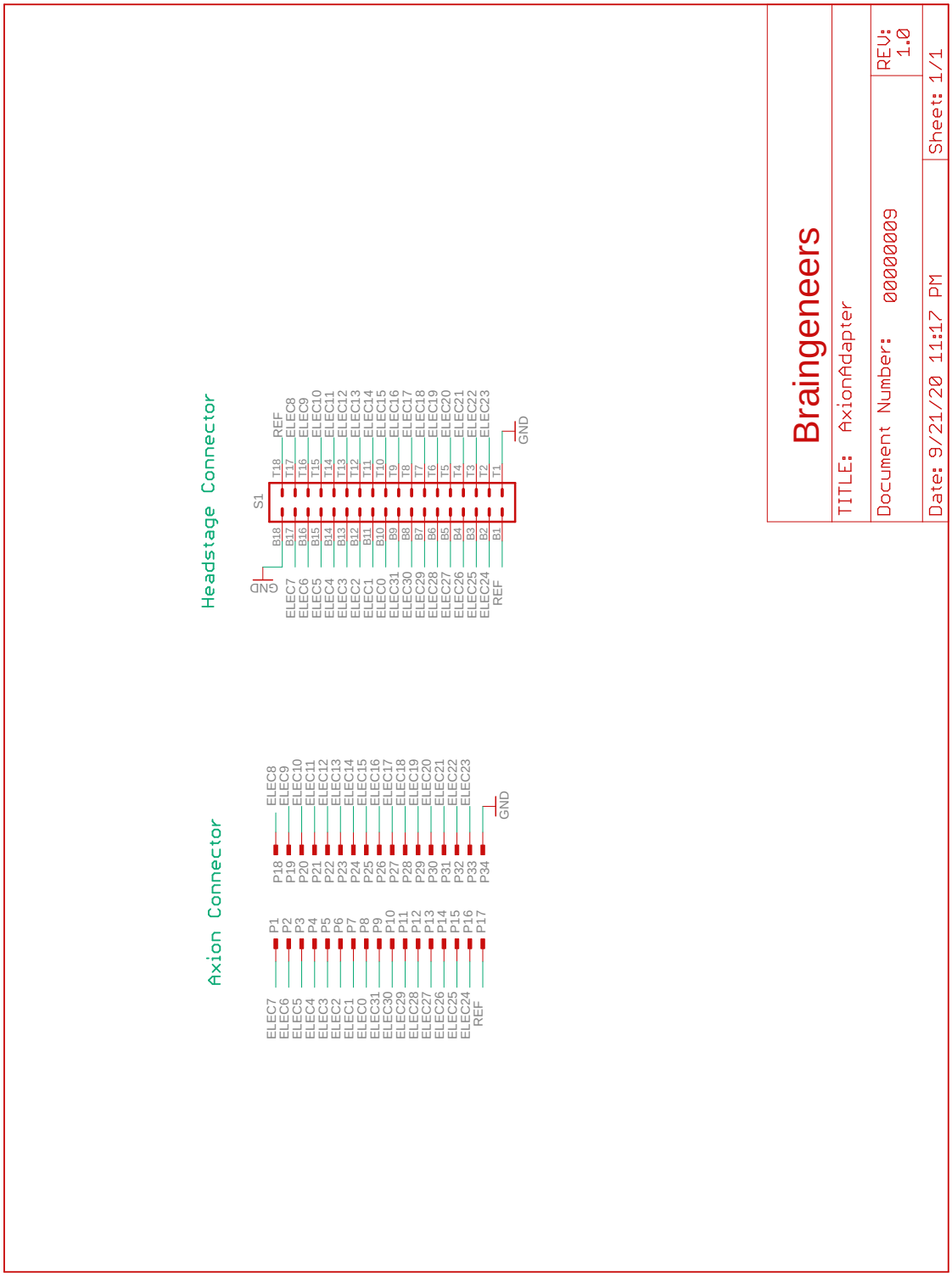


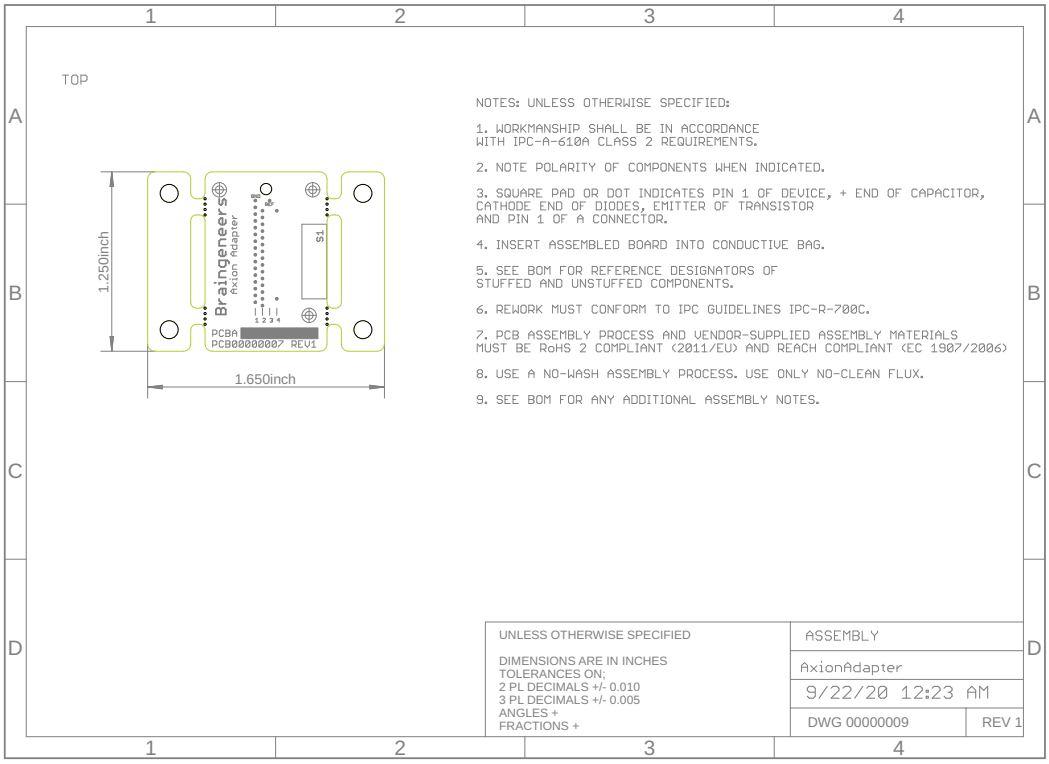

TOP
2.28inch
3.39inch
Braingeneers
RasPi RHD Controller
NaaS
PCB00000007 REV1
PCBA
NOTES: UNLESS OTHERWISE SPECIFIED:
1. WORKMANSHIP SHALL BE IN ACCORDANCE WITH IPC-A-610A CLASS 2 REQUIREMENTS.
2. NOTE POLARITY OF COMPONENTS WHEN INDICATED.
3. SQUARE PAD OR DOT INDICATES PIN 1 OF DEVICE, + END OF CAPACITOR, CATHODE END OF DIODES, EMITTER OF TRANSISTOR AND PIN 1 OF A CONNECTOR.
4. INSERT ASSEMBLED BOARD INTO CONDUCTIVE BAG.
5. SEE BOM FOR REFERENCE DESIGNATORS OF STUFFED AND UNSTUFFED COMPONENTS.
6. REWORK MUST CONFORM TO IPC GUIDELINES IPC-R-700C.
7. PCB ASSEMBLY PROCESS AND VENDOR-SUPPLIED ASSEMBLY MATERIALS MUST BE RoHS 2 COMPLIANT (2011/EU) AND REACH COMPLIANT (EC 1907/2006)
8. USE A NO-WASH ASSEMBLY PROCESS. USE ONLY NO-CLEAN FLUX.
9. SEE BOM FOR ANY ADDITIONAL ASSEMBLY NOTES.
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON;
2 PL DECIMALS +/- 0.010
3 PL DECIMALS +/- 0.005
ANGLES +
FRACTIONS +
ASSEMBLY
RasPi_Controller_RHD_Rev3_GND_Stitch
10/5/20 12:49 PM
DWG 00000007
REV 3


BOTTOM
CN1
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON;
2 PL DECIMALS +/- 0.010
3 PL DECIMALS +/- 0.005
ANGLES +
FRACTIONS +
ASSEMBLY
RasPi_Controller_RHD_Rev3_GND_Stitch
10/5/20 12:40 PM
DWG 00000007
REV 3


TOP SIDE
NOTES: UNLESS OTHERWISE SPECIFIED:
1. PCB TO BE FABRICATED PER IPC GUIDELINES:
IPC-A-6012B OR LATEST REVISION. IPC-D-275 AND IPC-RB-276 CLASS 2 OR LATEST REVISION.
2. FINISHED BOARD TO BE 0.062IN +/- 10% THINK.
MATERIAL: ITEQ IT-180A, OR 370HR FR4, OR EQUIVALENT.
4 LAYERS. LAYERS 1 AND 4 TO HAVE 1 OZ. MIN COPPER CLAD BEFORE PLATING,
AND PLATE PER IPC-6012.
COPPER PLATE ON WALL OF HOLES SHALL BE 0.001 AVERAGE, 0.0008 ABSOLUTE MINIMUM
3. MINIMUM ANNULAR RING IS 0.002 FOR COMPONENT HOLES, TANGENCY FOR VIAS.
4. MASTER ARTWORK (FILM/GERBER DATA) IS NOT ETCH COMPENSATED.
COMPENSATE WORKING FILM SUCH THAT TRACE WIDTHS
MATCH TRACE WIDTHS OF MASTER ARTWORK WITHIN +/- 20% OF TRACE WIDTH
5. USE BLUE LIQUID PHOTO IMAGEABLE SOLDER MASK
CONFORMING TO IPC-SM-840C CLASS H.
BOARD TO HAVE SOLDER MASK OVER BARE COPPER ON BOTH SIDES.
NO SOLDER MASK TO PAD PERMISSIBLE, EXCEPT VIAS.
VIAS ARE TO BE MASKED PER ARTWORK MASTER.
6. SILKSCREEN BOTH SIDES USING SILKSCREEN MASTER.
SILKSCREEN TO BE WHITE NON-CONDUCTIVE, NON-NUTRIENT EPOXY INK,
OR ACRYLIC PRINT TAIYO IJR-4000 MW300.
7. WARPAGE NOT TO EXCEED 0.10 PER LINEAR INCH
8. PCB MUST PASS 100% ELECTRICAL TESTING
FOR OPENS AND SHORTS IN ACCORDANCE WITH IPC-ET-652.
TRUE NETLIST TESTING REQUIRED USING SUPPLIED IPC NETLIST.
9. ALL REWORK MUST FONCOFM TO IPC GUIDELINES:
IPC-R-700C (OR MOST CURRENT REVISION).
10. MINIMUM CONDUCTOR WITH TO BE 0.006".
MINIMUM CONDUCTOR TO CONDUCTOR AND CONDUCTOR TO PAD SPACING TO BE 0.006"
11. SURFACE FINISH: ENIG (ELECTROLESS NICKEL IMMERSION GOLD)
2-5 MICRO INCHES IMMERSION (SOFT) GOLD PLATE OVER 118-236 MICO INCHES NICKEL
12. ALL SOLDER PADS TO BE FREE OF SILKSCREEN INK.
13. PCB SHALL BE ROHS 2 COMPLIANT (2011/65/EU), REACH COMPLIANT (EC1907/2006)
AND COMPATIBLE WITH ROHS ASSEMBLY PROCESS
14. VIA REQUIREMENTS: FOLLOW SUPPLIED GERBERS.
SOLDER MASK ON PAD - FOLLOW SOLDER MASK GERBER FILES
15. OK TO ADD COPPER THIEVING TO SPARSELY POPULATED AREAS OF PCB AS NEEDED
16. IF COPPER PAD OR PLATED HOLES TOUCH BOARD OUTLINE,
FOLLOW GERBER AND ACCEPT COPPER EXPOSED AT BOARD EDGE
17. ADD TEARDROPS TO ALL PADS AT TRACE JUNCTIONS
LAYER-STACK
01-16
01-20
SILKSCREEN TOP
SOLDER MASK TOP
LAYER 1 - TOP GROUND (1 OZ)
PREPREG: DIELECTRIC (8 MIL)
LAYER 2 - SIGNAL PLANE (1 OZ)
CORE: DIELECTRIC (FILLER)
LAYER 3 - POWER PLANE (1 OZ)
PREPREG: DIELECTRIC (8 MIL)
LAYER 4 - BOTTOM GROUND (1 OZ)
SOLDER MASK BOTTOM
SILKSCREEN BOTTOM
TOTAL BOARD THICKNESS: 62 MIL
DRILL CHART (ALL UNITS IN MILS)
Sym | Mils | Tol | Plated | Qty
+ | 11.811 | 0 | YES | 606
× | 15.000 | 0 | NOT | 16
□ | 36.000 | 0 | YES | 9
◇ | 47.244 | 0 | YES | 6
⧖ | 55.118 | 0 | YES | 3
⋈ | 118.110 | 0 | NOT | 4
✣ | 125.000 | 0 | NOT | 4
OK WITH DEFAULT TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON;
2 PL DECIMALS +/- 0.010
3 PL DECIMALS +/- 0.005
ANGLES +
FRACTIONS +
FABRICATION
RasPi_Controller_RHD_Rev3_GND_Stitch
10/5/20 12:40 PM
DWG 00000007
REV 3

2.2. Axion Adapter




TOP
1.250inch
1.650inch
Braingeneers
Axion Adapter
S1
1 2 3 4
PCBA
PCB0000000? REV1
NOTES: UNLESS OTHERWISE SPECIFIED:
1. WORKMANSHIP SHALL BE IN ACCORDANCE WITH IPC-A-610A CLASS 2 REQUIREMENTS.
2. NOTE POLARITY OF COMPONENTS WHEN INDICATED.
3. SQUARE PAD OR DOT INDICATES PIN 1 OF DEVICE, + END OF CAPACITOR, CATHODE END OF DIODES, EMITTER OF TRANSISTOR AND PIN 1 OF A CONNECTOR.
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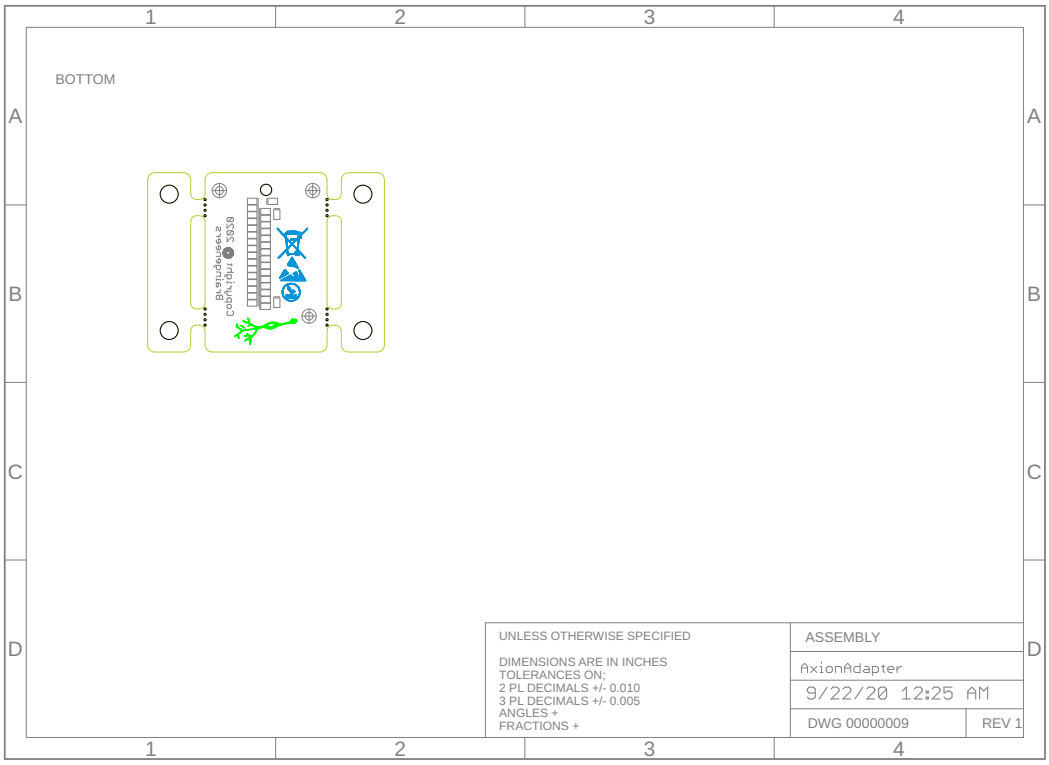
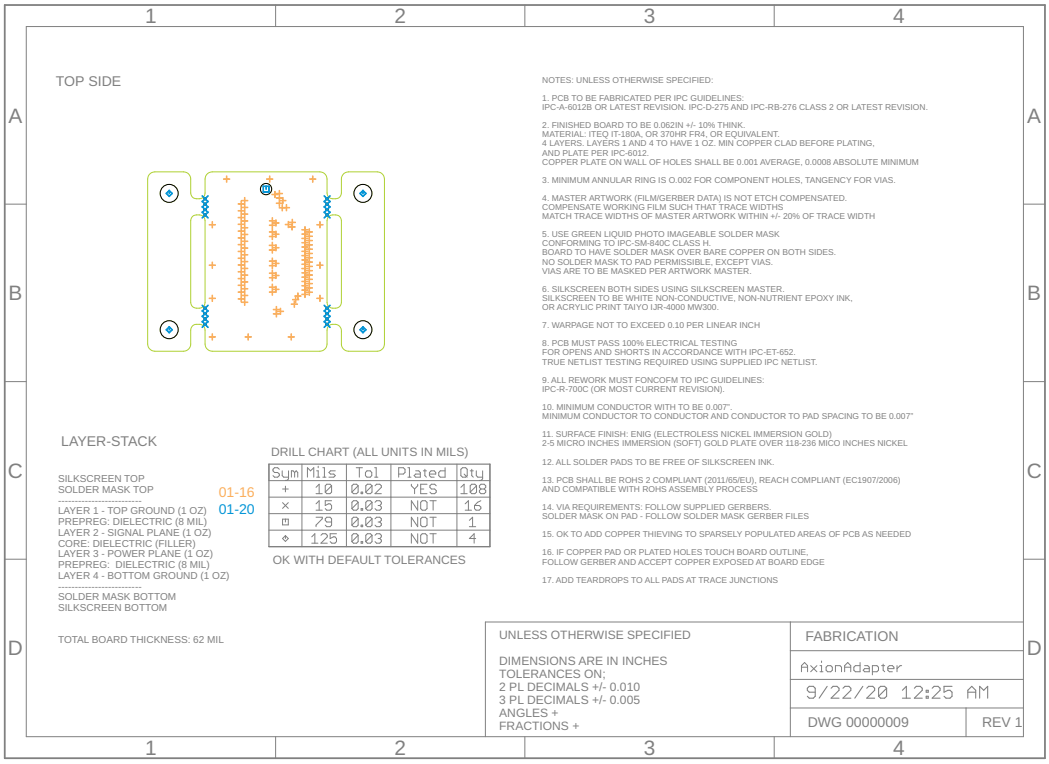
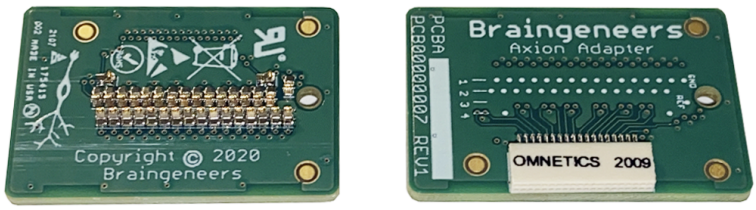
8. USE A NO-WASH ASSEMBLY PROCESS. USE ONLY NO-CLEAN FLUX.
9. SEE BOM FOR ANY ADDITIONAL ASSEMBLY NOTES.
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON;
2 PL DECIMALS +/- 0.010
3 PL DECIMALS +/- 0.005
ANGLES +
FRACTIONS +
ASSEMBLY
AxionAdapter
9/22/20 12:23 AM
DWG 00000009
REV 1


BOTTOM
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON;
2 PL DECIMALS +/- 0.010
3 PL DECIMALS +/- 0.005
ANGLES +
FRACTIONS +
ASSEMBLY
AxionAdapter
9/22/20 12:25 AM
DWG 00000009
REV 1





(a) (b)

Figure S4. (a) Top of custom connector with finger pins which face the Axion plate. (b) Bottom of connector with Intan RHD200 headstage adapter.