Science Advances
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Supplementary Materials for

Concealable physically unclonable function chip with a memristor array

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Sci. Adv. **8**, eabn7753 (2022)
DOI: 10.1126/sciadv.abn7753

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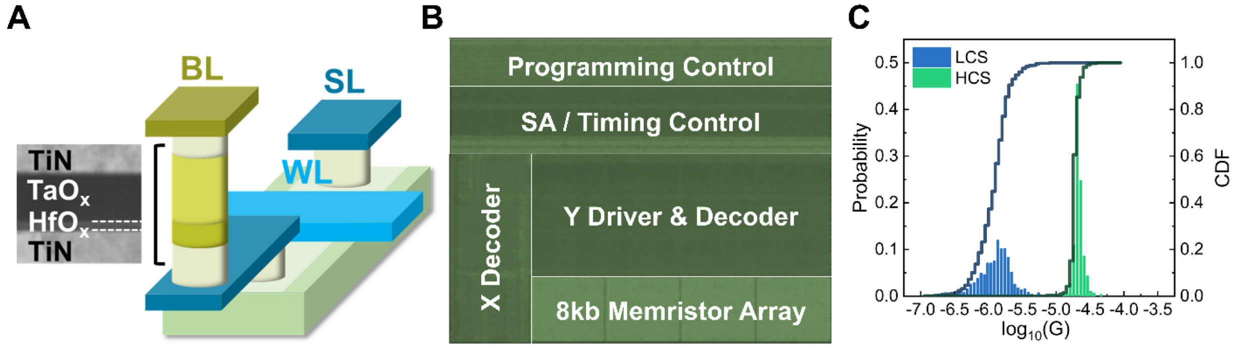


Fig. S1. PUF chip, memristor device, and D2D variation. (**A**) Basic 1T1R structure with a memristor integrated between M5 and M6. The inset is the cross-section transmission electron micrograph (TEM) of the memristor material stack. (**B**) Micrograph of the fabricated PUF chip. (C) The D2D variation in conductance values measured from 1024 memristors.

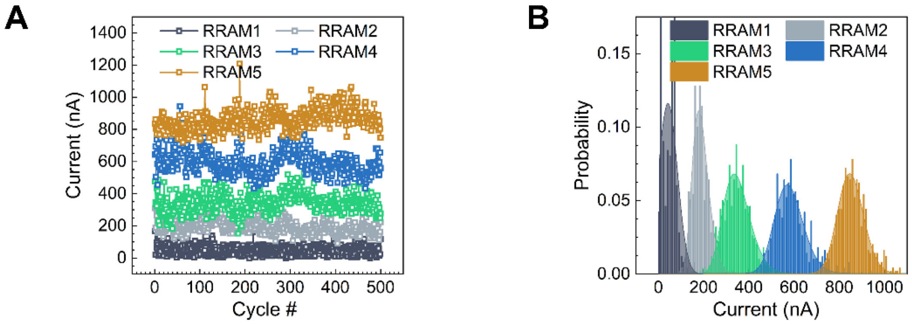


Fig. S2. C2C correlation in memristor conductance values. (**A**) The change in conductance values of 5 memristors with incremental SET/RESET cycle. The conductance values are read out after RESET. (**B**) The corresponding probability distributions of these conductance values.

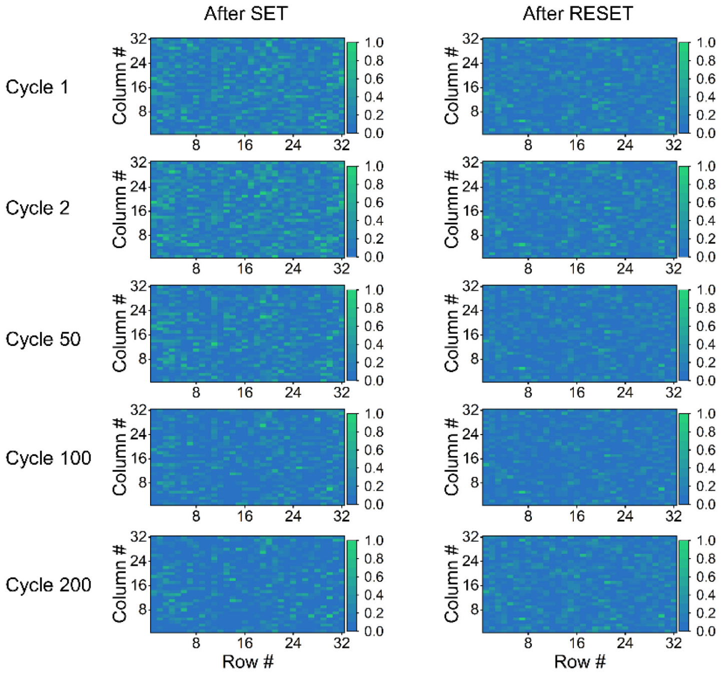


Fig. S3. Change in the conductance distributions. Colormaps of the conductance distributions for 1 kb memristors with incremental SET-RESET cycle. The conductance values are normalized for each colormap individually.

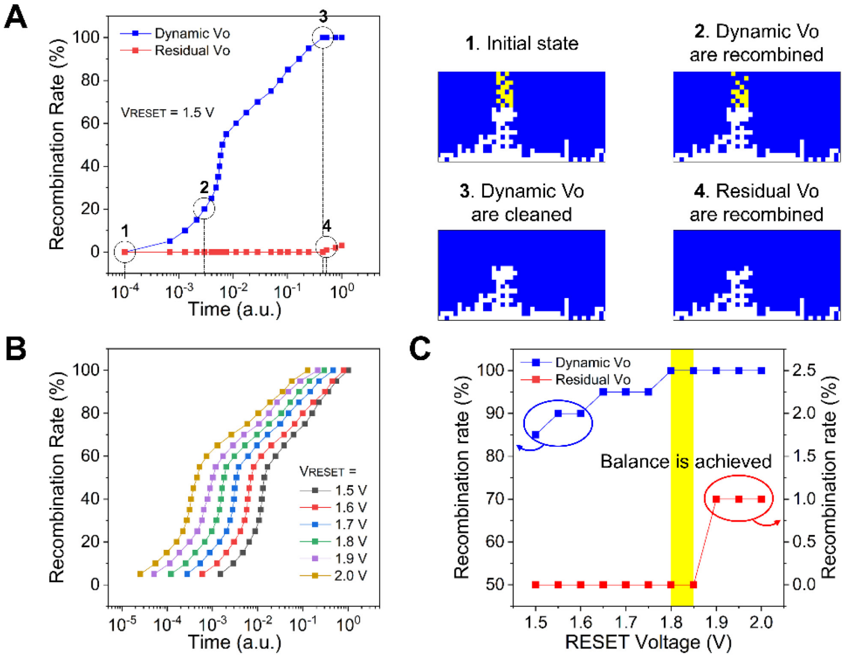


Fig. S4. Simulated change of Vo during the RESET process. (**A**) The change in the recombination rate of dynamic Vo and residual Vo with incremental RESET time. The insets show the corresponding change in filament morphology. (**B**) Dynamic Vo are combined at a higher speed with incremental RESET voltage. (**C**) The change in recombination rate of dynamic Vo and residual Vo with different RESET voltages. With RESET voltage approximately 1.825 V, a perfect balance between SET and RESET is achieved with 100% recombination of dynamic Vo and 0% recombination of residual Vo.

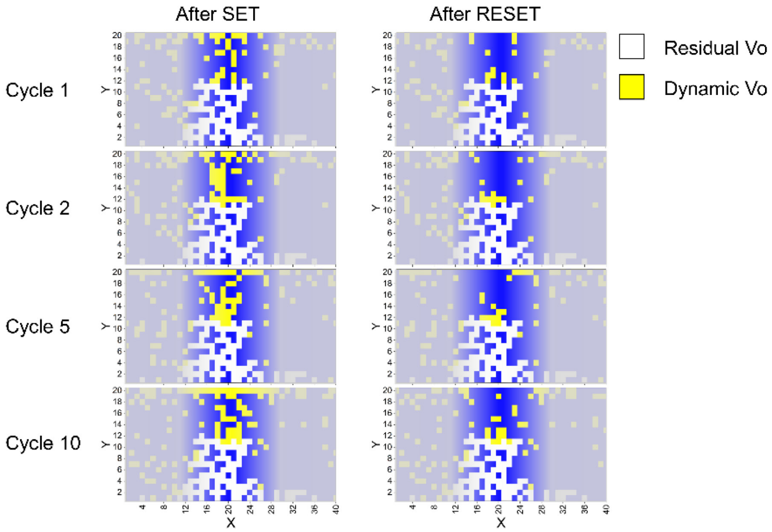
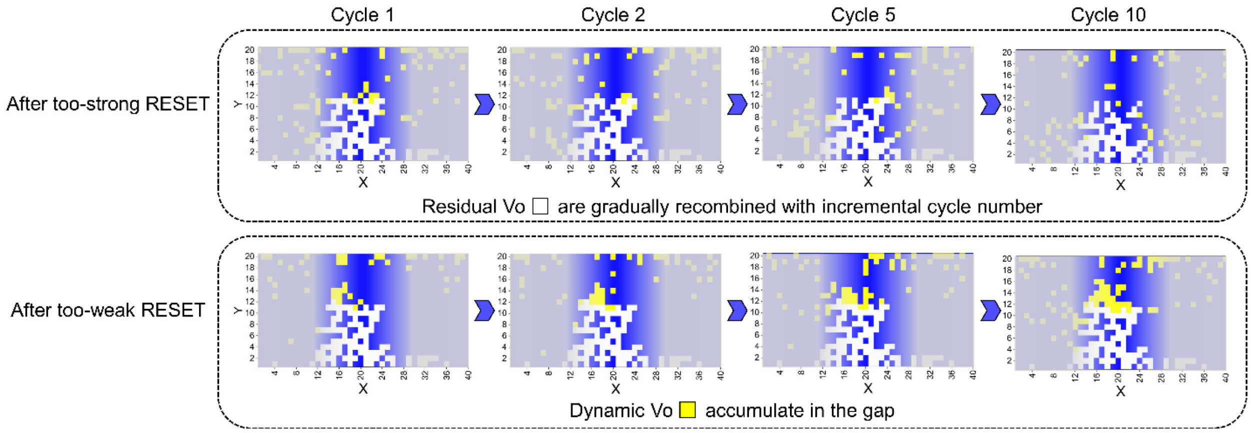


Fig. S5. KMC simulation results with balanced SET and RESET conditions. The simulated change in filament morphology after multiple RESET-SET operations. The filaments mainly formed at the center, contributing the most to the device conductivity. The other marginal parts are less important and thus are covered in translucent gray in these subfigures. The yellow cells represent the dynamic Vo, which are randomly generated in the filament gap to bridge a conductive path after SET and erased after RESET. The white cells represent the residual part, which remains unchanged among the switching cycles. The SET and RESET voltages are 1.6 V and 1.85 V, respectively.


Cycle 1

Cycle 2

Cycle 5

Cycle 10

After too-strong RESET

Residual Vo □ are gradually recombined with incremental cycle number

After too-weak RESET

Dynamic Vo 🟨 accumulate in the gap

Fig. S6. KMC simulation results with unbalanced SET and RESET conditions. The simulated change in filament morphology after RESET with RESET condition that is too strong (e.g., V_{RESET} = 2.0 V) and RESET conditions that is too weak (e.g., V_{RESET} = 1.6 V).

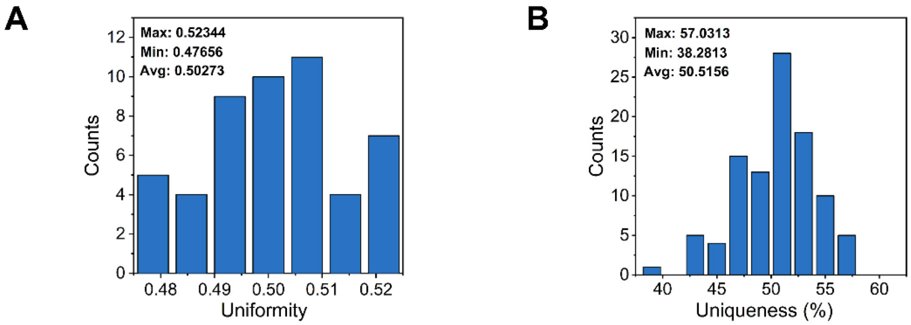


Fig. S7. Randomness evaluation results. (**A**) The uniformity distribution of 50 128-bit PUF keys. The uniformity measures the probability of a PUF bit being 1, and its ideal value is 0.5. From the distribution, the average uniformity is 0.50273. (**B**) The uniqueness distribution of 50 128-bit PUF keys collected from 5 chip (i.e., 10 PUF keys per chip). The uniqueness measures the difference between the two responses from two PUF chips which are inquired with the same challenge, and its ideal value is 50%. From the distribution, the average uniqueness is 50.5156%.

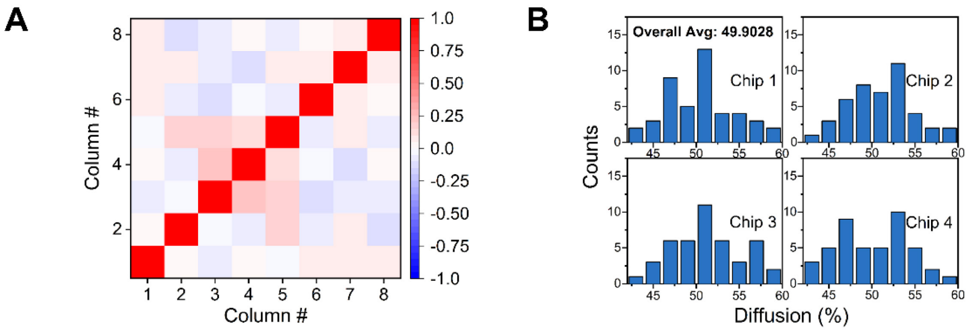


Fig. S8. Diffusion evaluation results. (**A**) The correlation coefficient matrix of the resistance values of any two columns in a PUF chip, where negligible correlation can be found, indicating that the resistance distribution is highly random. (**B**) The diffusion distribution of 40 128-bit PUF keys collected from 4 chip (i.e., 10 PUF keys per chip). The diffusion measures the difference between any two responses from one PUF chip, and its ideal value is 50%. In most case, the diffusion ranges from 43% to 57%, and the average is 49.9028%.

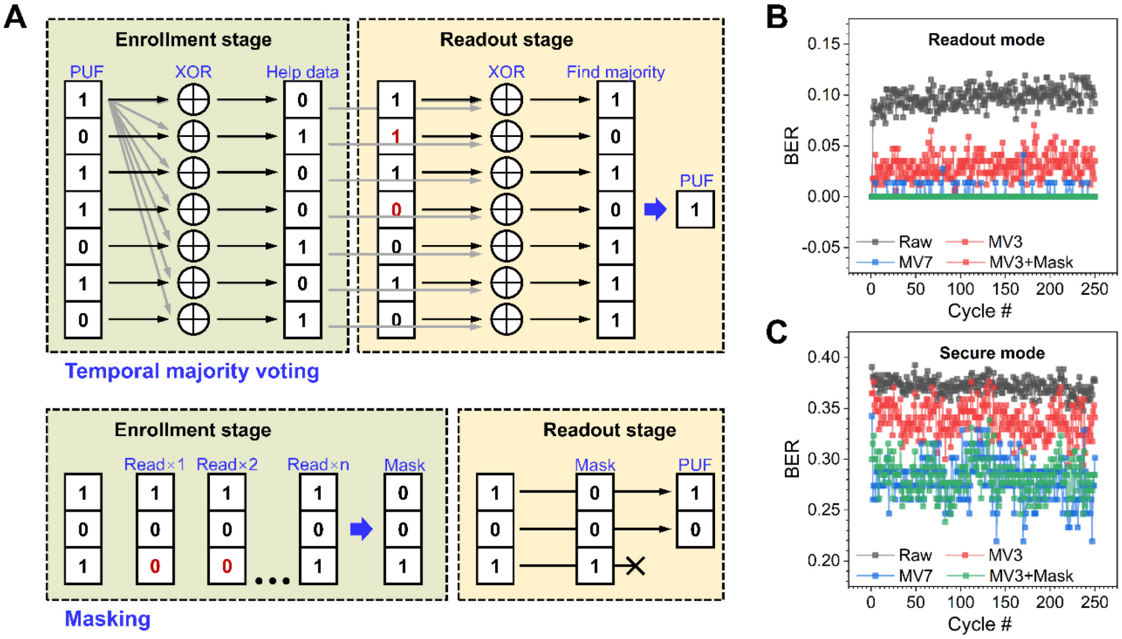


Fig. S9. Measured BER with reliability enhancement techniques. (**A**) The implementations of temporal majority voting (TMV) and masking techniques. TMVx means using x memristors to represent 1 PUF bit. (**B**) The change of BER in readout mode with different methods. (**C**) The change of BER in secure mode with different methods.

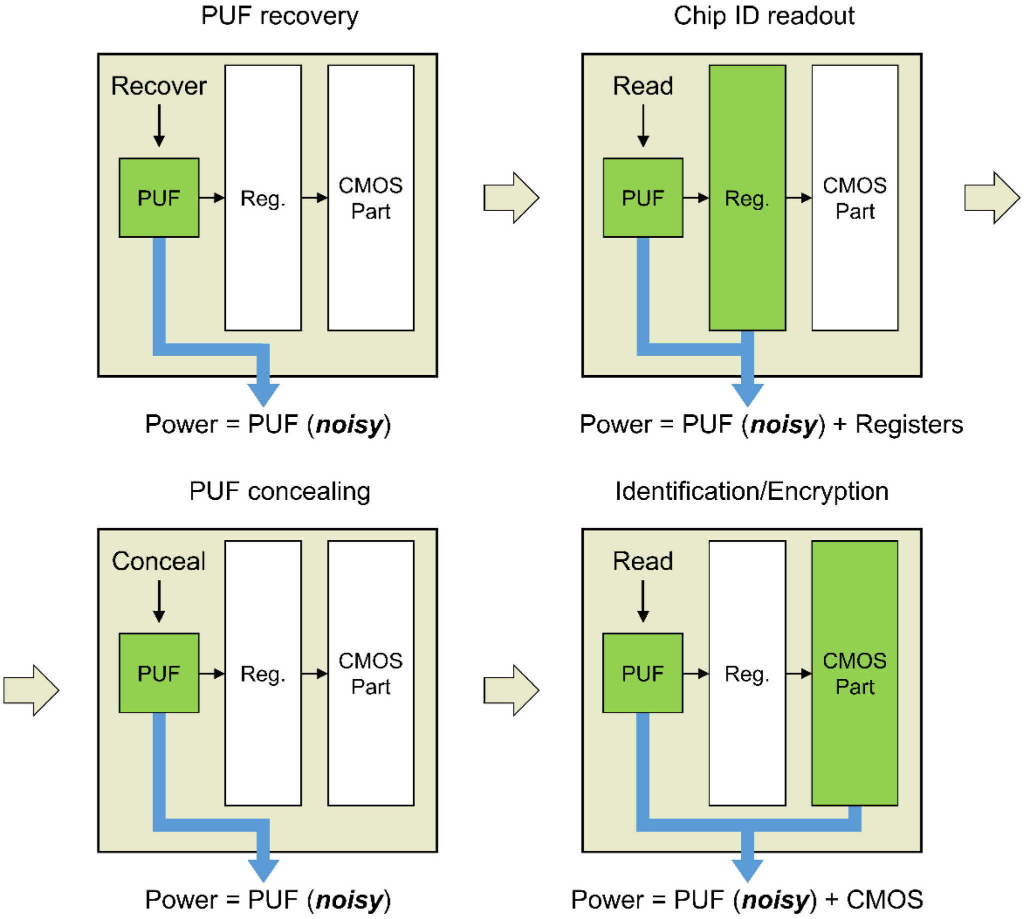

PUF recovery
Recover
PUF
Reg.
CMOS Part
Power = PUF (***noisy***)
Chip ID readout
Read
PUF
Reg.
CMOS Part
Power = PUF (***noisy***) + Registers
PUF concealing
Conceal
PUF
Reg.
CMOS Part
Power = PUF (***noisy***)
Identification/Encryption
Read
PUF
Reg.
CMOS Part
Power = PUF (***noisy***) + CMOS

Fig. S10. A side-channel secure system based on the concealable PUF . Side-channel attacks such as differential power attacks break a security system by understanding the relationship between power consumption and CMOS circuit operations. The concealable PUF provides a feasible and efficient countermeasure by leveraging its inherent write/read noise, making the side-channel signal extremely noisy whenever the chip is working.

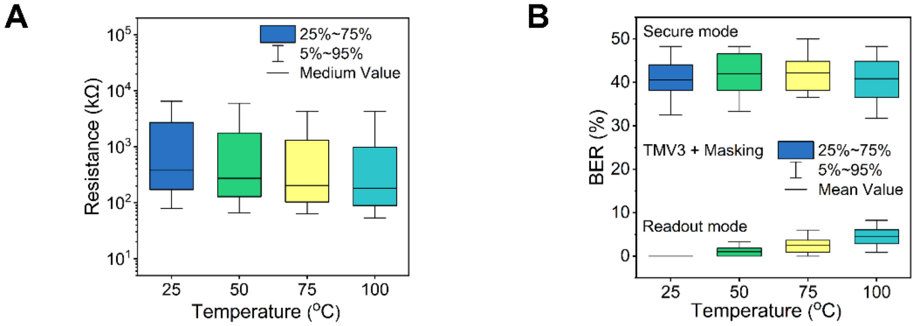


Fig. S11. High temperature test result of the concealable memristive PUF. (**A**) The change of the resistance distribution with incremental temperature. (**B**) The change of the BER in secure mode and readout mode with incremental temperature.

Table S1. NIST SP800-22 randomness evaluation results

NIST SP800-22	PUF (1280 bits per chip)				
	Chip1	Chip2	Chip3	Chip4	Chip5
1. Approximate Entropy	0.6105	0.5016	0.8116	0.8118	0.8934
2. Block Frequency	0.9110	0.2472	0.0716	0.8738	0.9989
3. Cumulative Sum	0.8768	0.7013	0.3415	0.8052	0.8982
4. FFT	0.7975	0.3049	0.1238	0.6079	0.3049
5. Frequency	1.0000	0.9554	1.0000	1.0000	1.0000
6. Longest Runs	0.9542	0.7160	0.4544	0.0633	0.8572
7. Rank	0.6937	0.6937	0.6937	0.6937	0.6937
8. Runs	0.3143	0.6149	0.4673	0.0736	0.5023
9. Serial	0.0122	0.4423	0.9218	0.1977	0.7596

Table S2. Power consumption/efficiency and delay with TMVx technique

130nm **VDD = 1.80 V** **System Clock = 10 MHz**	**Power Consumption (µW)**	**Delay (ns)**
TMV3 post-process circuit	0.891	0.0699
TMV5 post-process circuit	4.604	0.2740
D flip-flop	0.753	0.2786
SA	24.04	100.00
	Power Efficiency (pJ/bit)	**Delay (ns)**
Read without TMV circuit	2.404	100.28
Read with TMV3	7.213	300.35
Read with TMV5	12.03	500.55

Table S3. Comparison to different PUF devices

	This work	**(*7*)**	**(*38*)**	**(*22*)**	**(*52*)**	**(*53*)**	**(*54*)**
Device	Memristor	Memristor	Memristor	SRAM	Anti-fuse	CNT	MJT
Unit Area (F^2)	108	-	-	9,628	219	-	172
Uniformity	0.5013	0.501	~50	0.4805	0.5009	0.5047	0.4980
Diffuseness (%)	49.903	50.01	-	-	-	-	-
Uniqueness (%)	50.516	49.96	50.06	49	49.999	50.00	-
NIST Test	Passed	Passed	Not reported	Passed	Passed	Passed	Not reported
BER (%)	0.00	1.22	13.82	2.58	0.00	~3.00	<0.01
Concealable?	Yes	No	No	No	No	No	No

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