

Figure 1

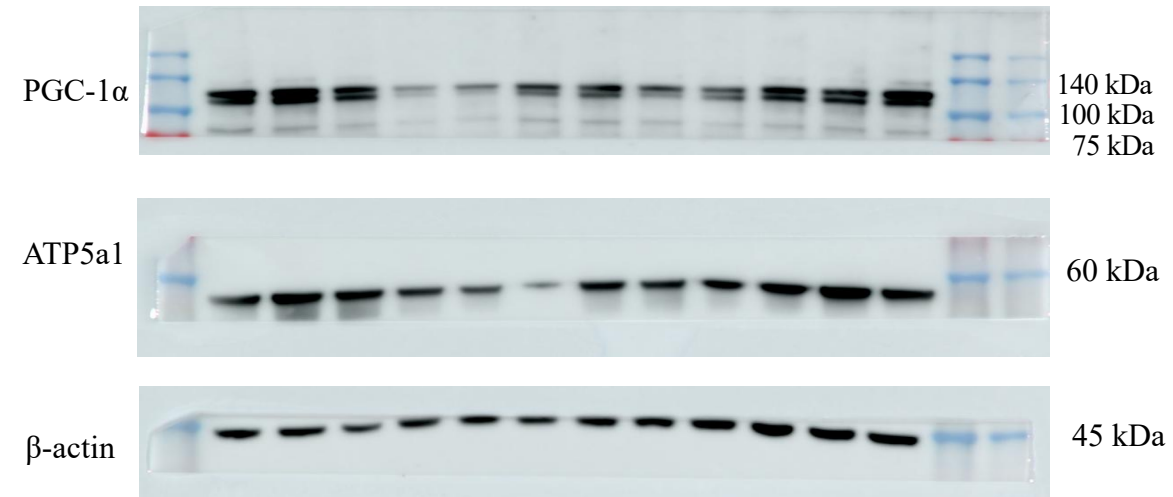
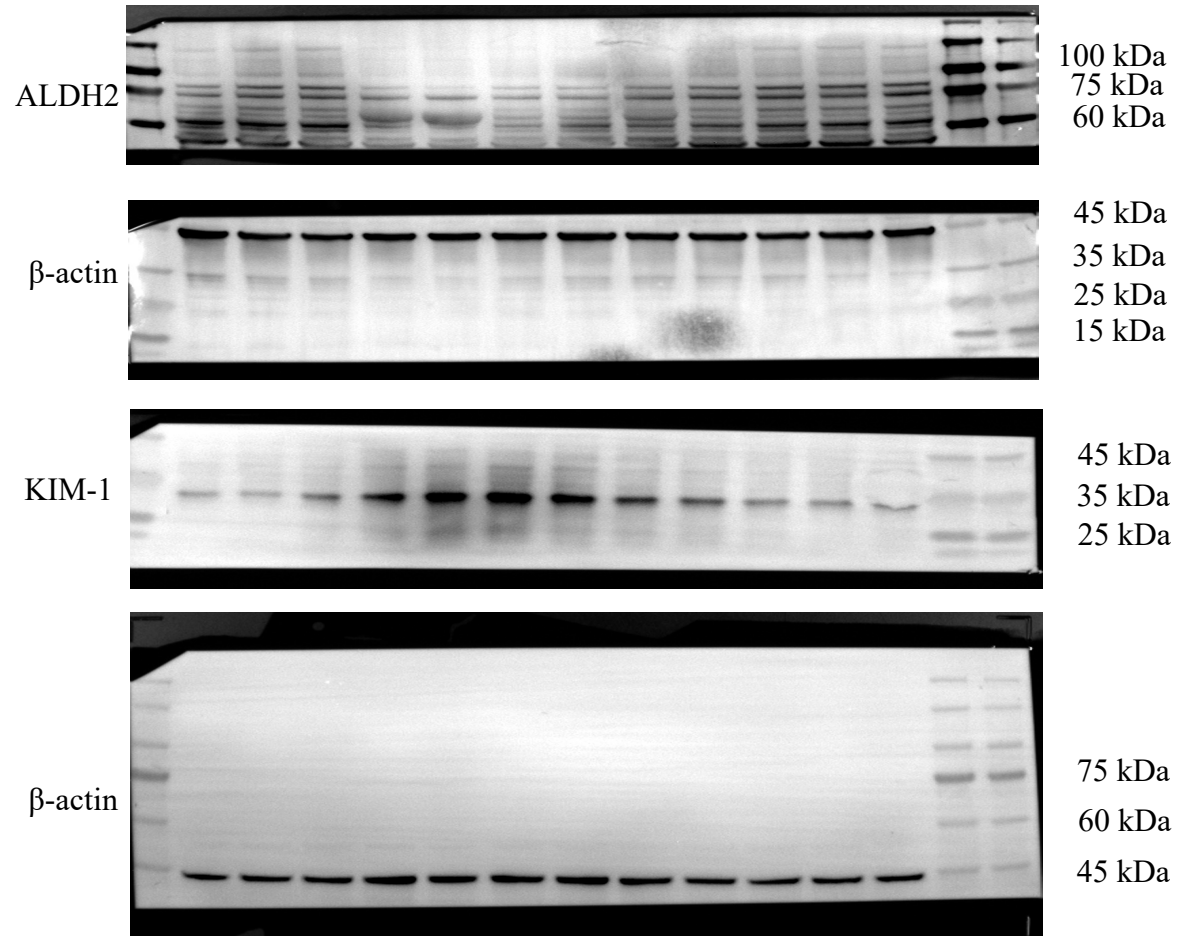


Figure 2

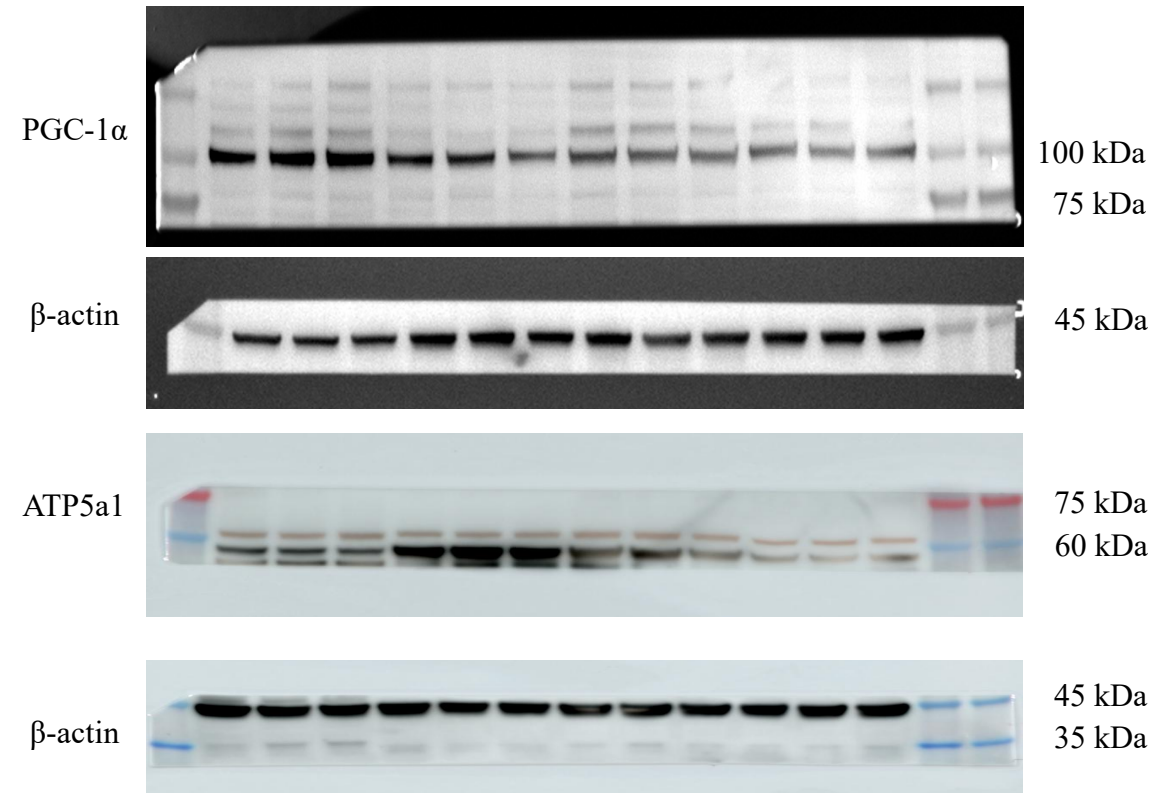
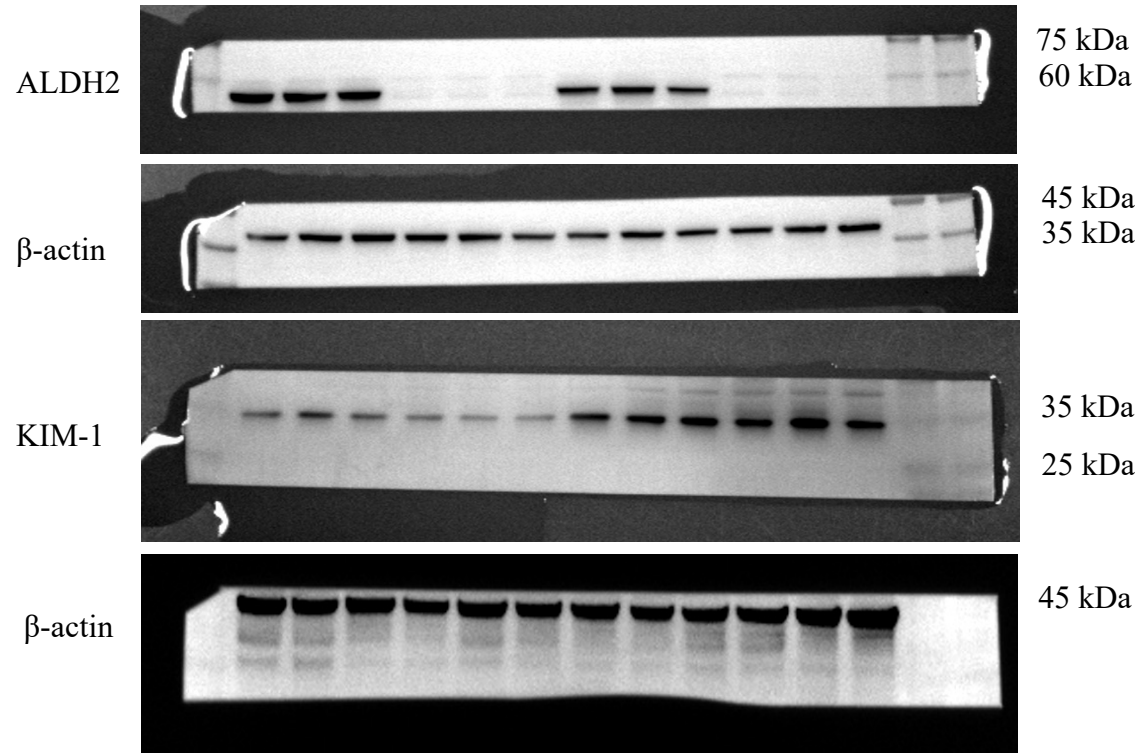


Figure 3

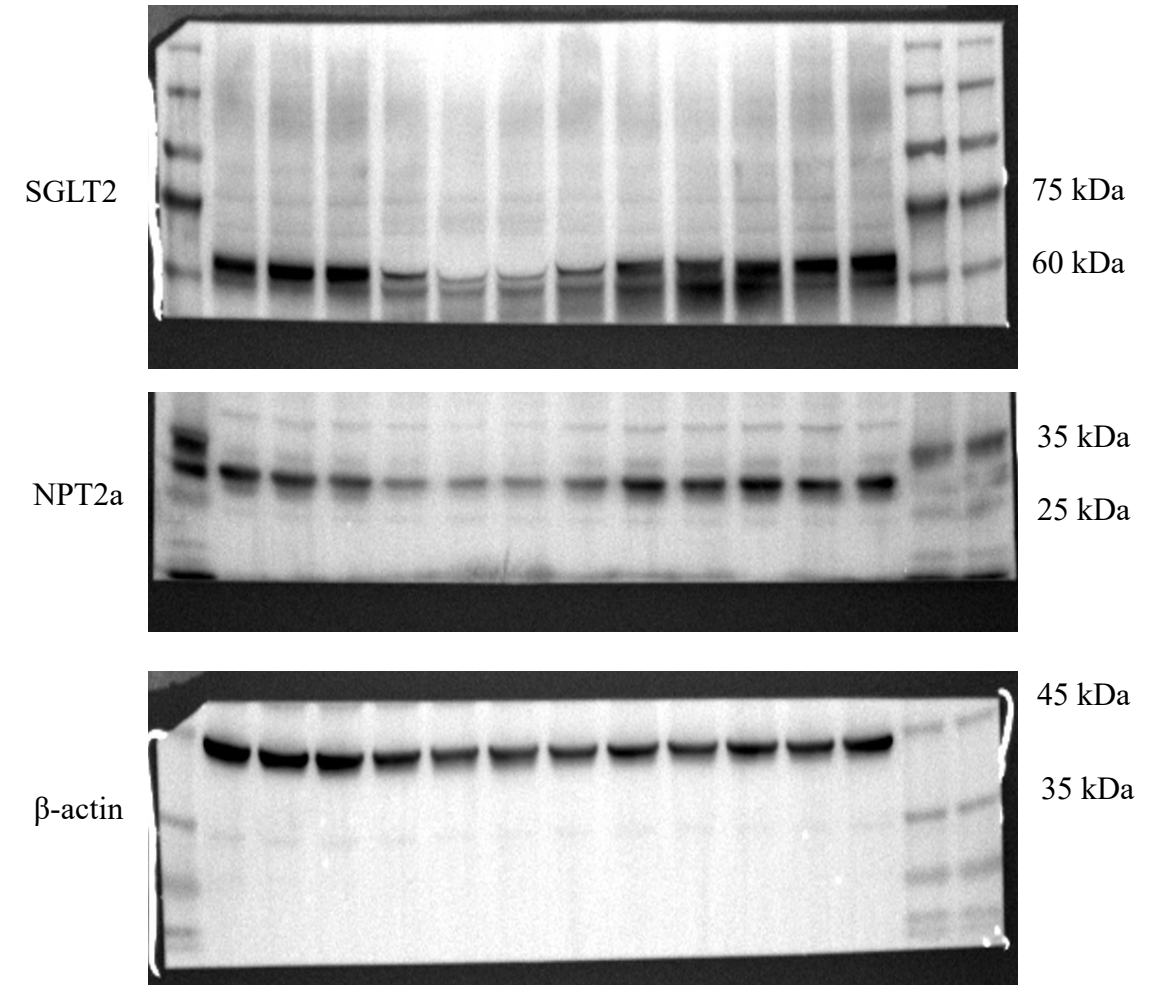
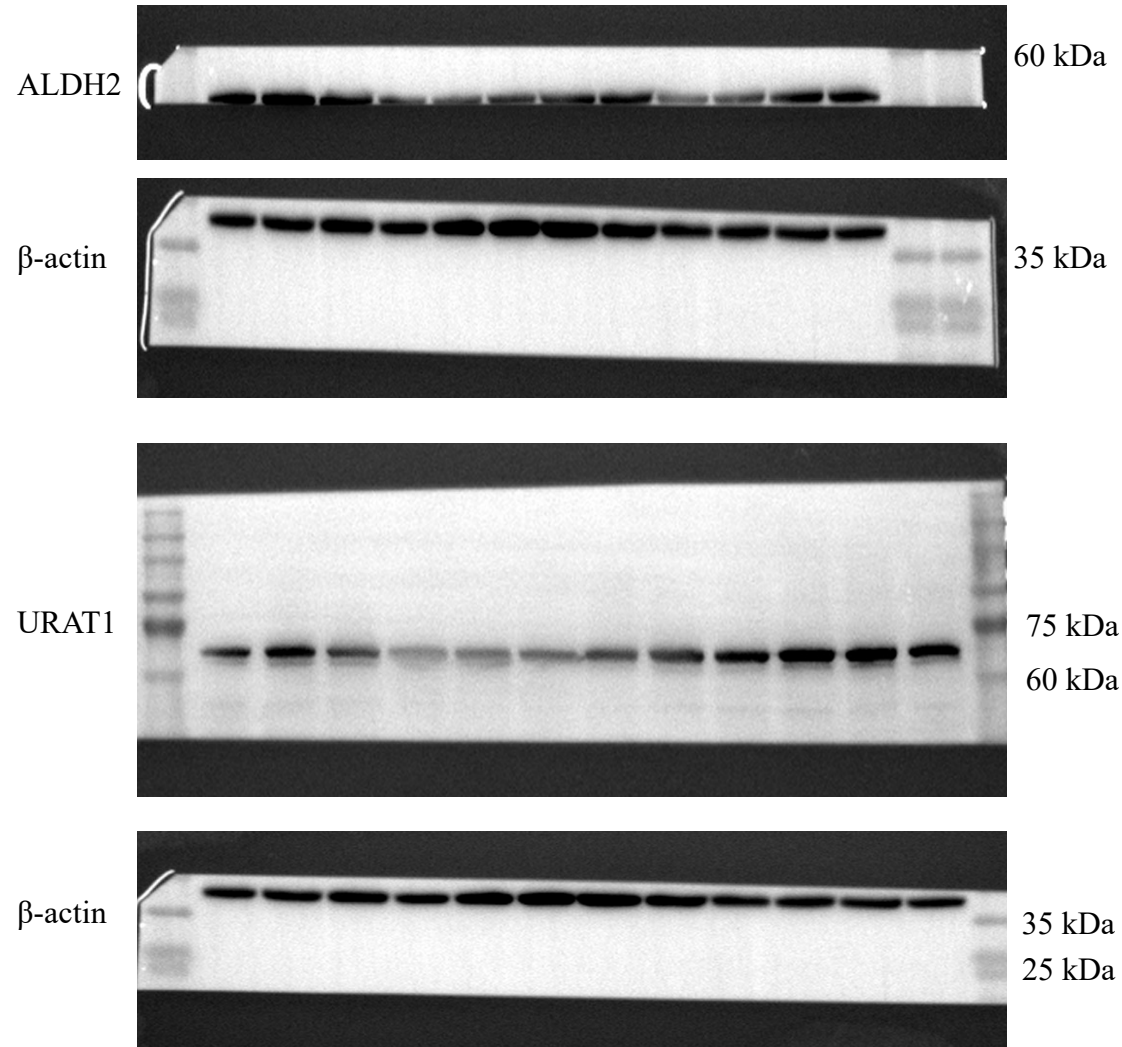


Figure 4

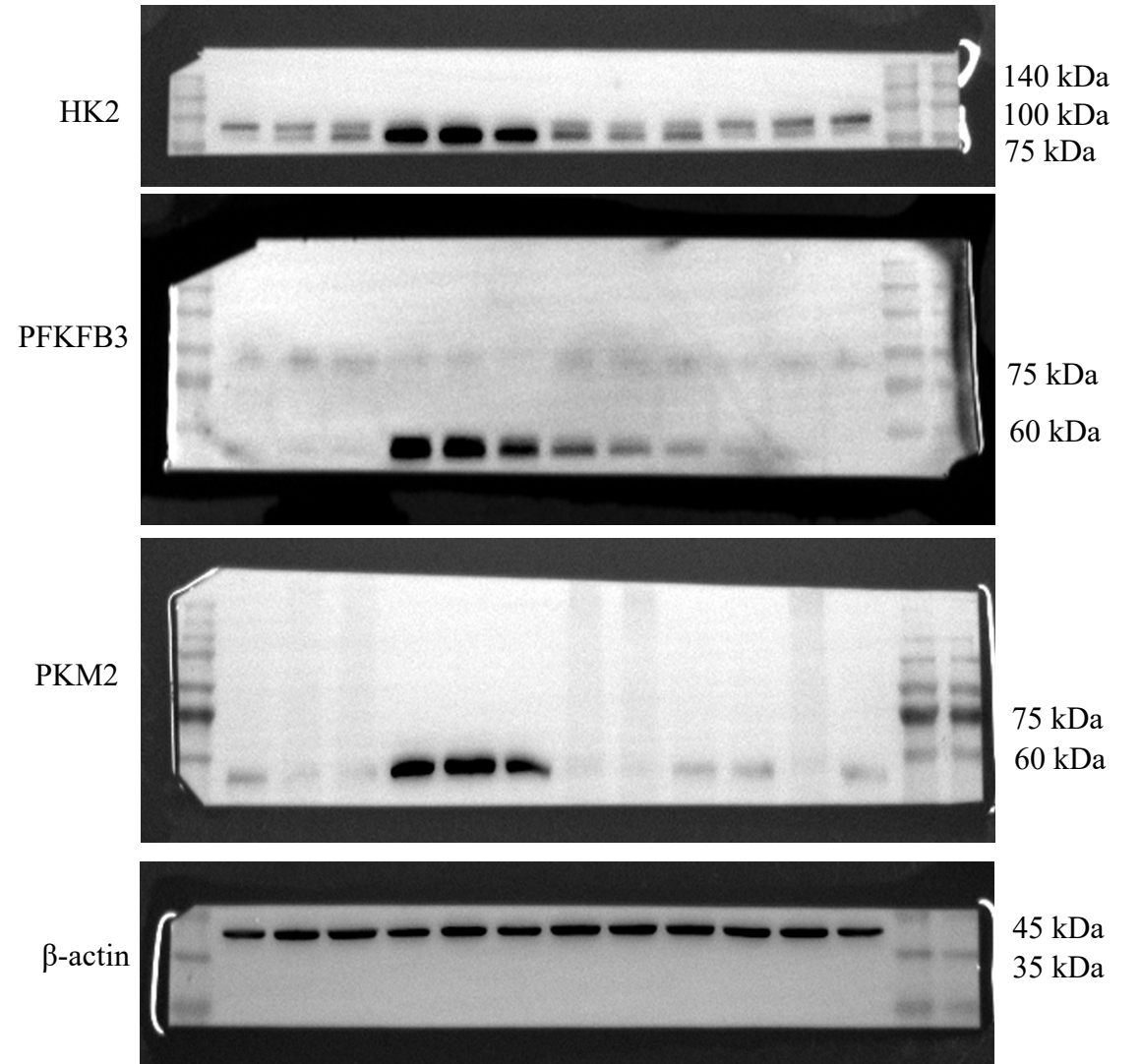
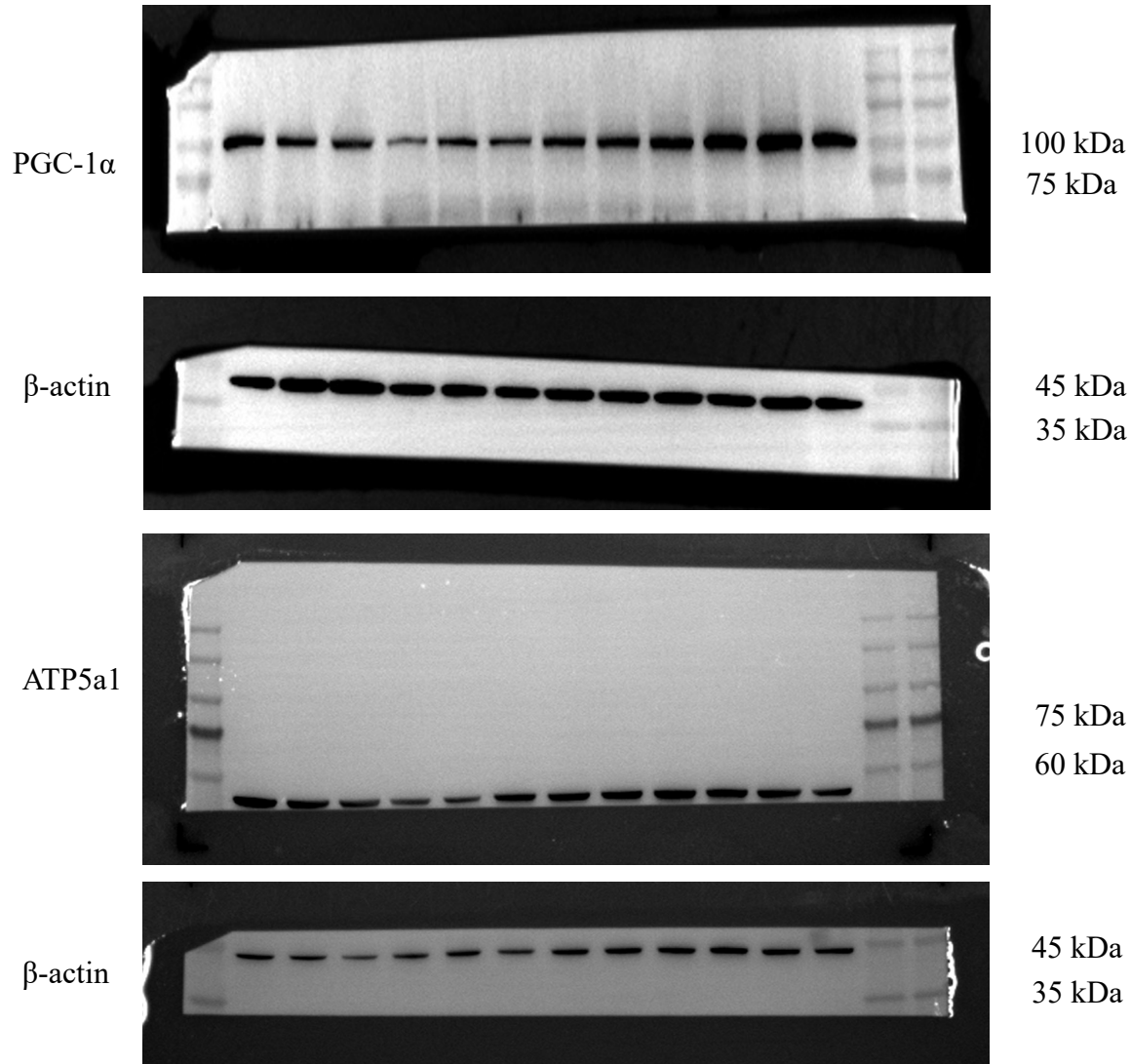


Figure 5

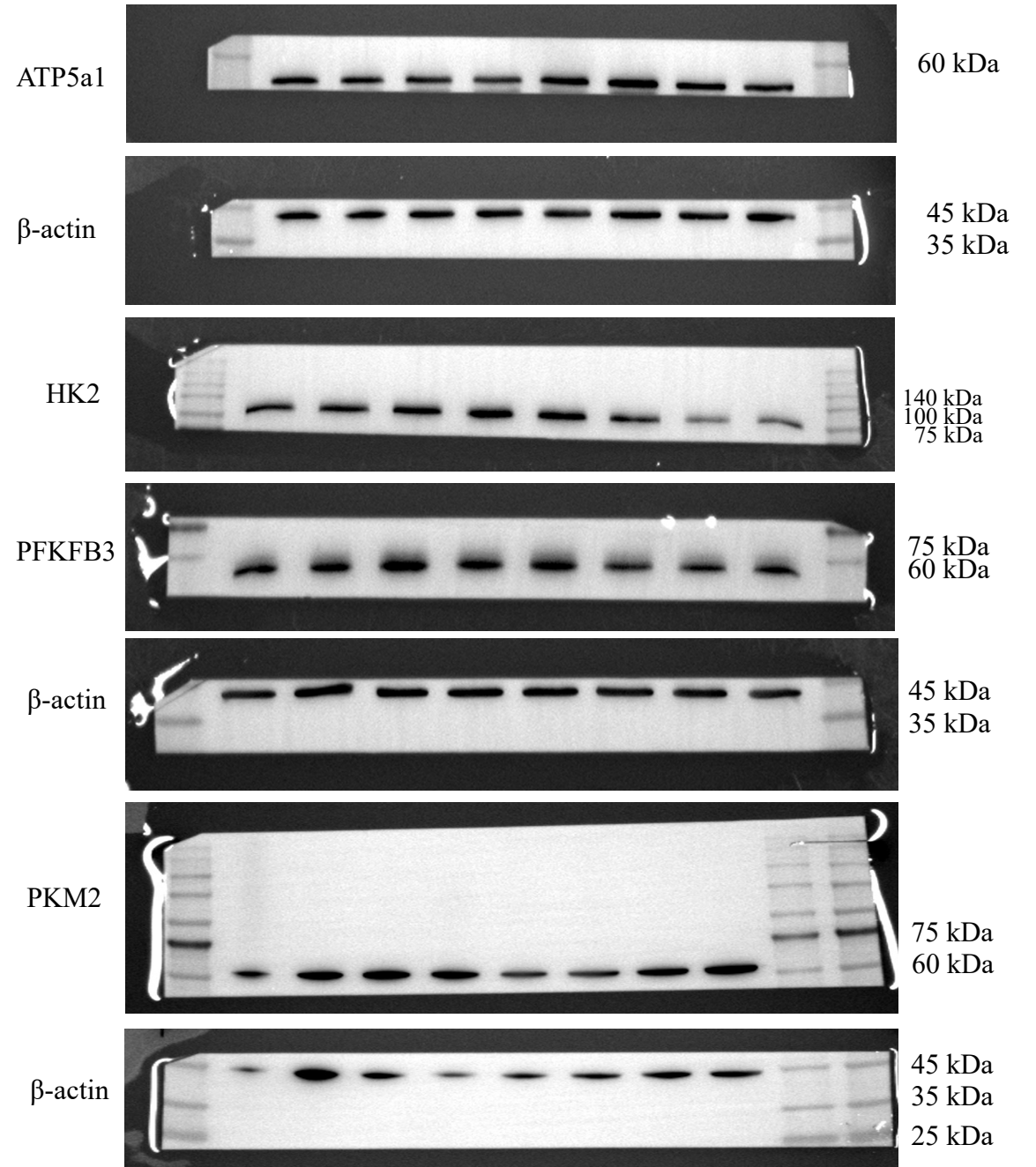
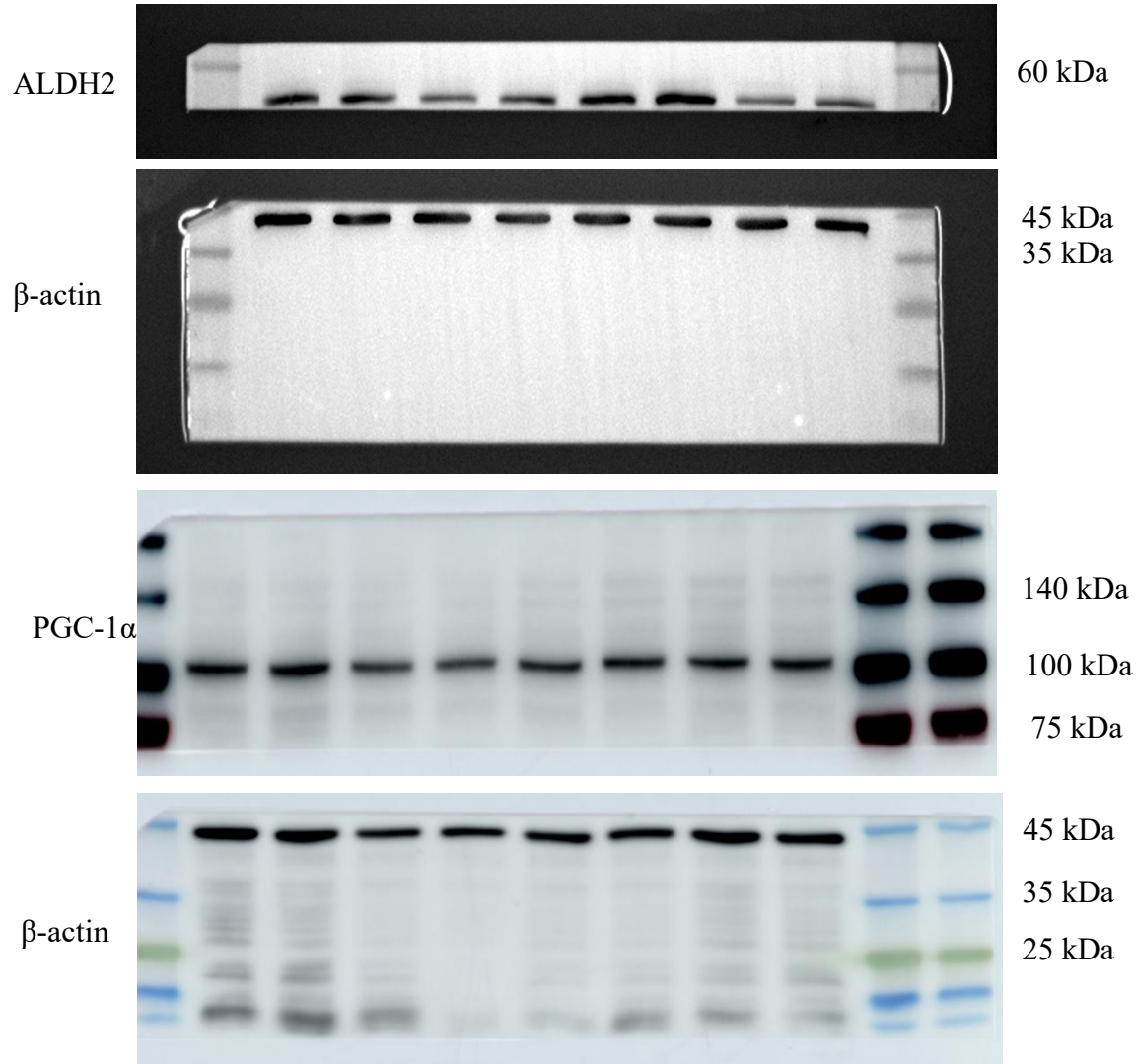


Figure 6

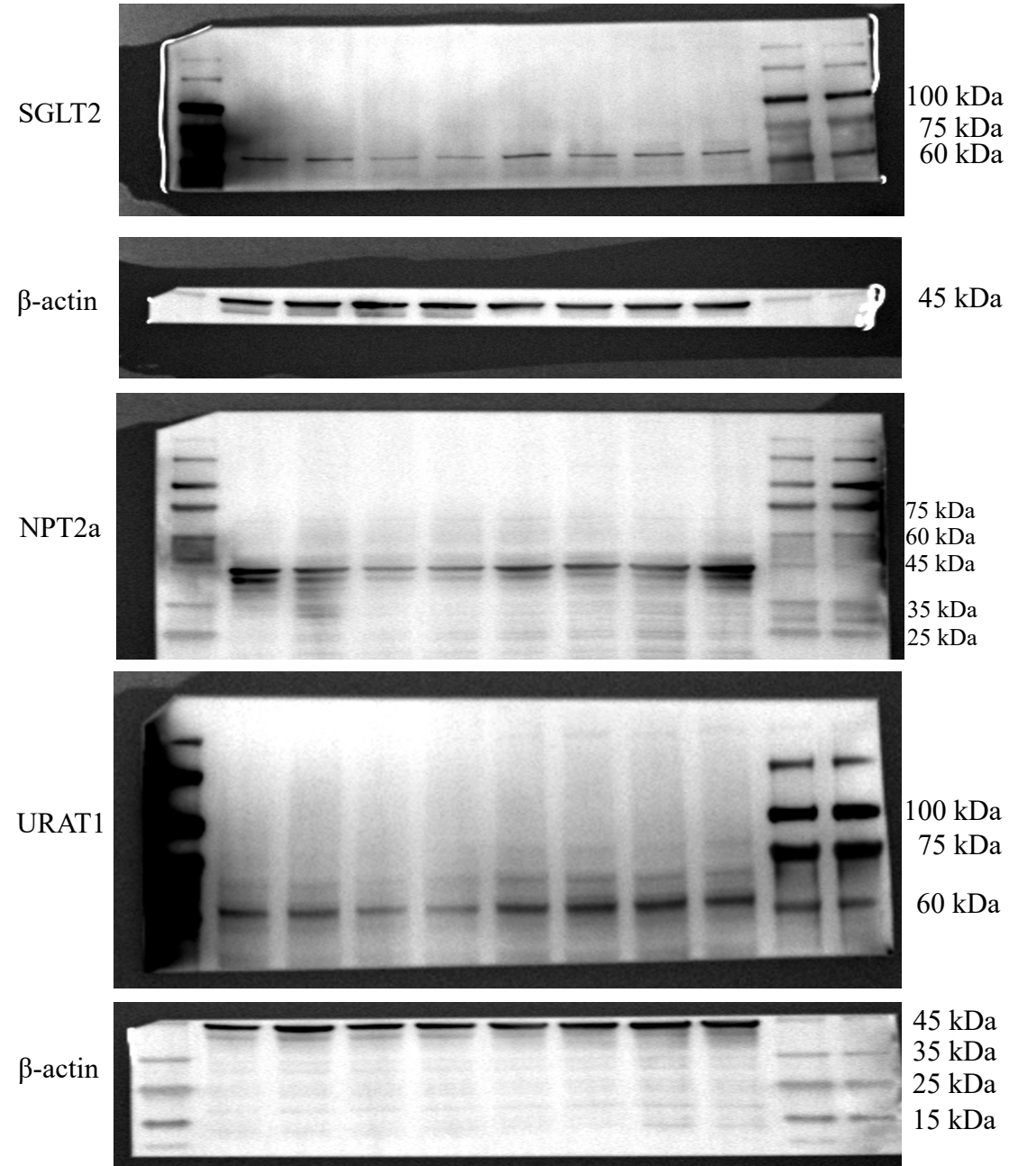
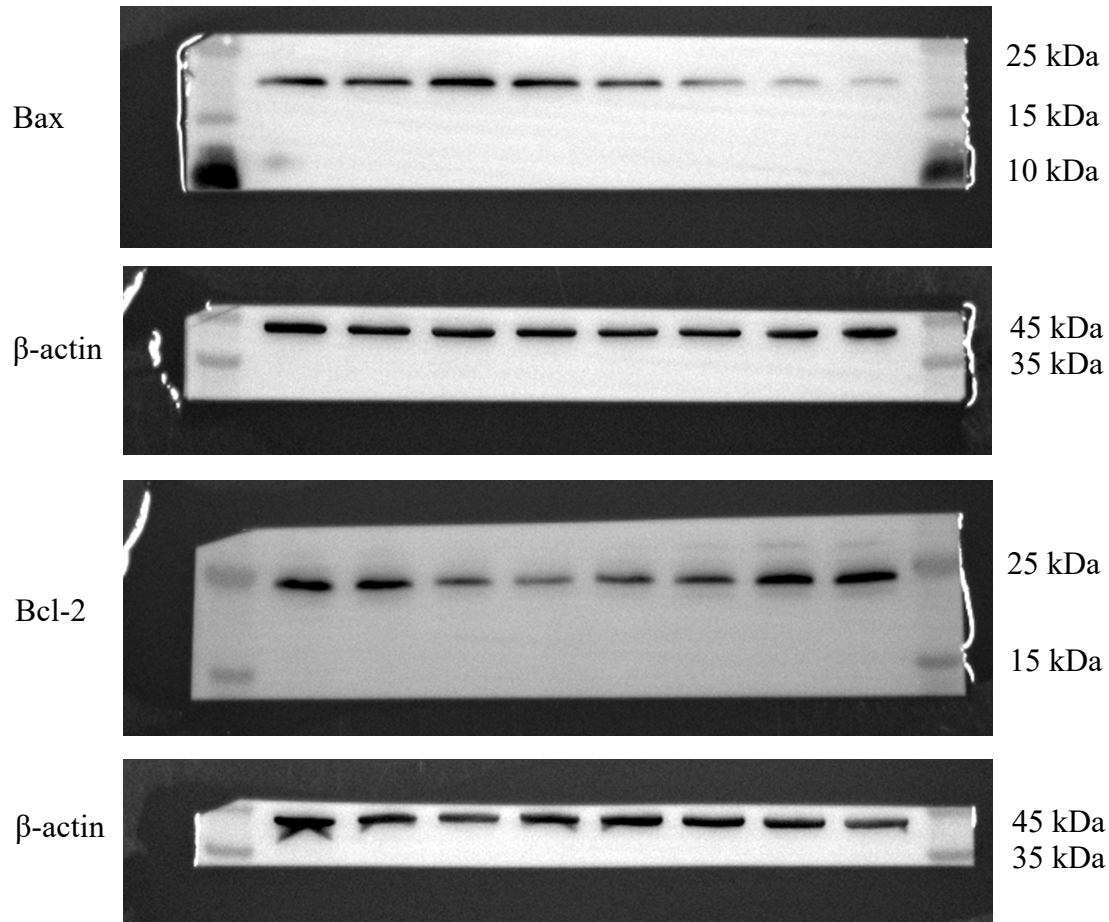
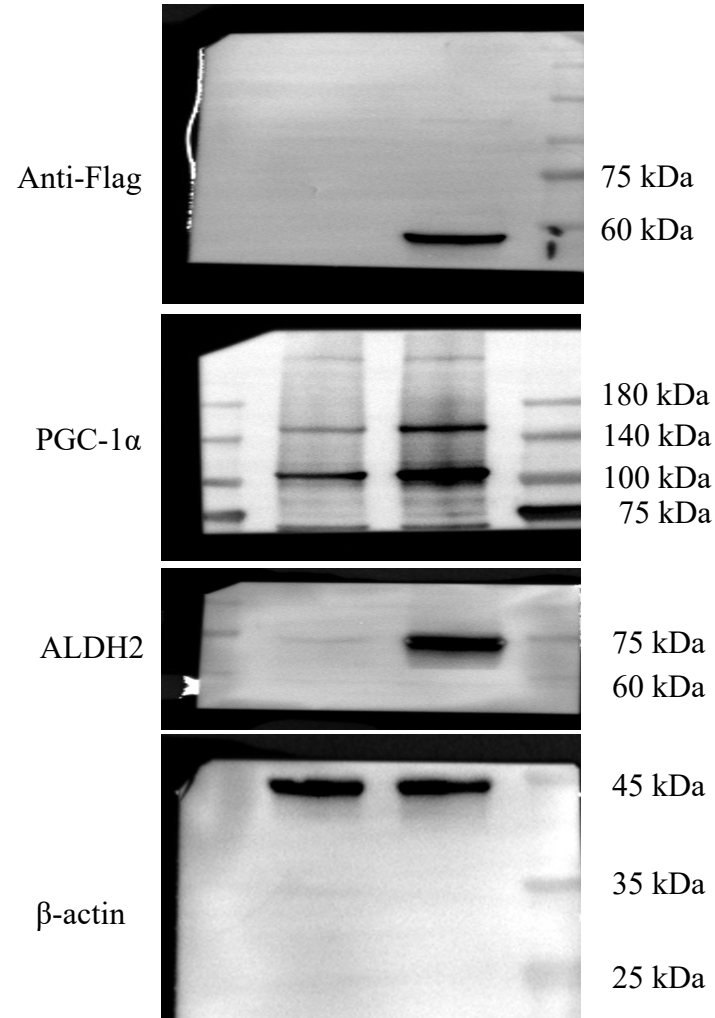


Figure 7B-C

Input



IP

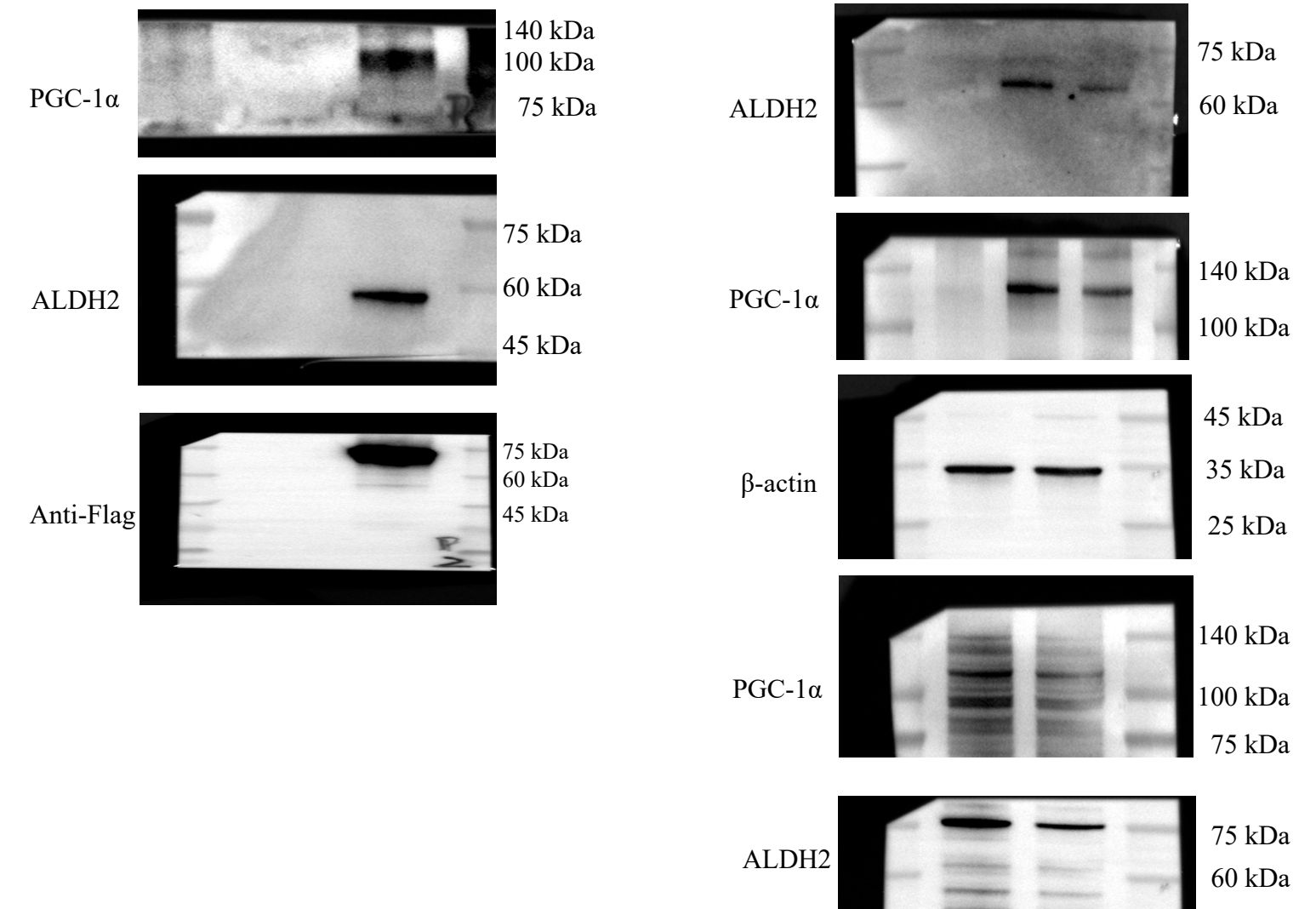


Figure 7D

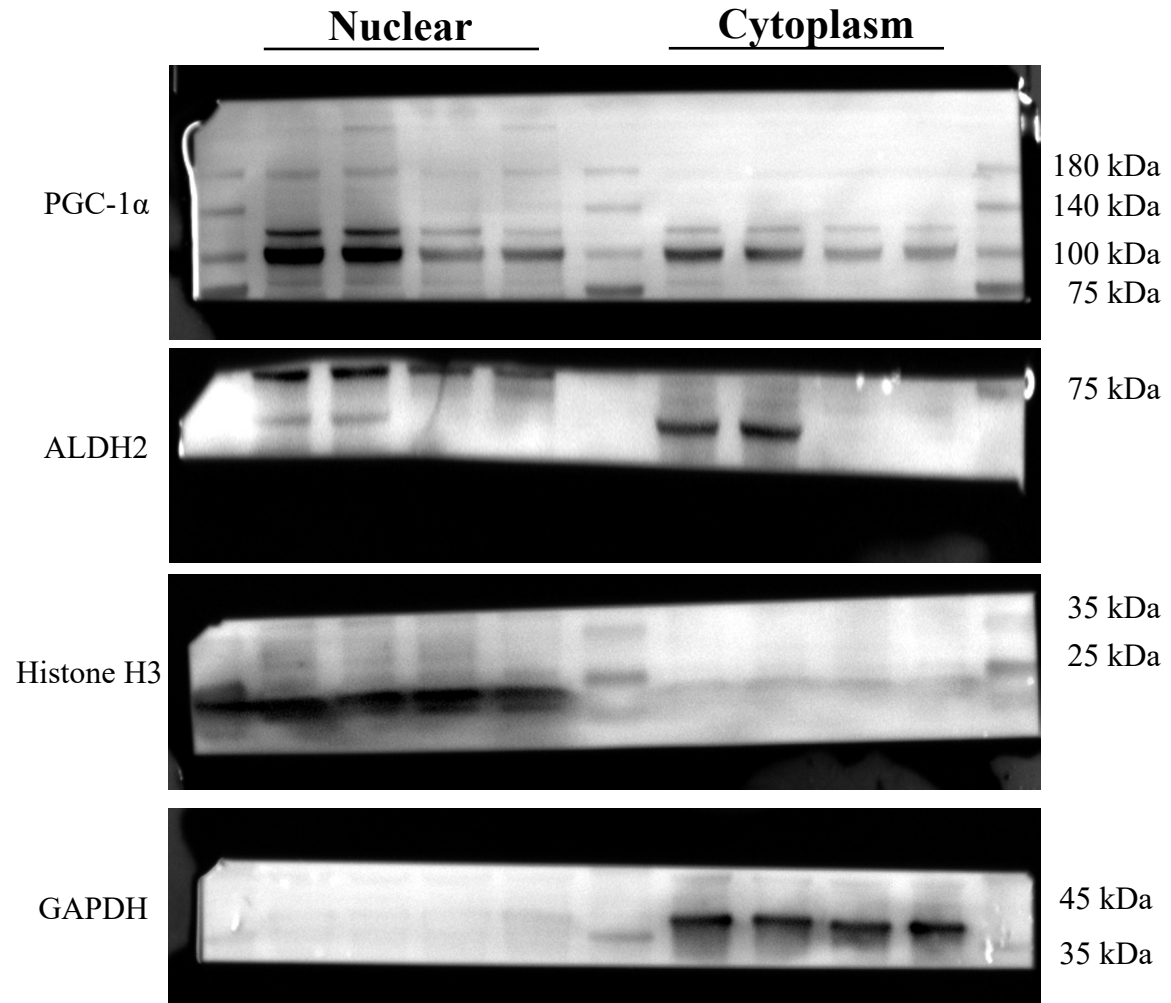


Figure 8

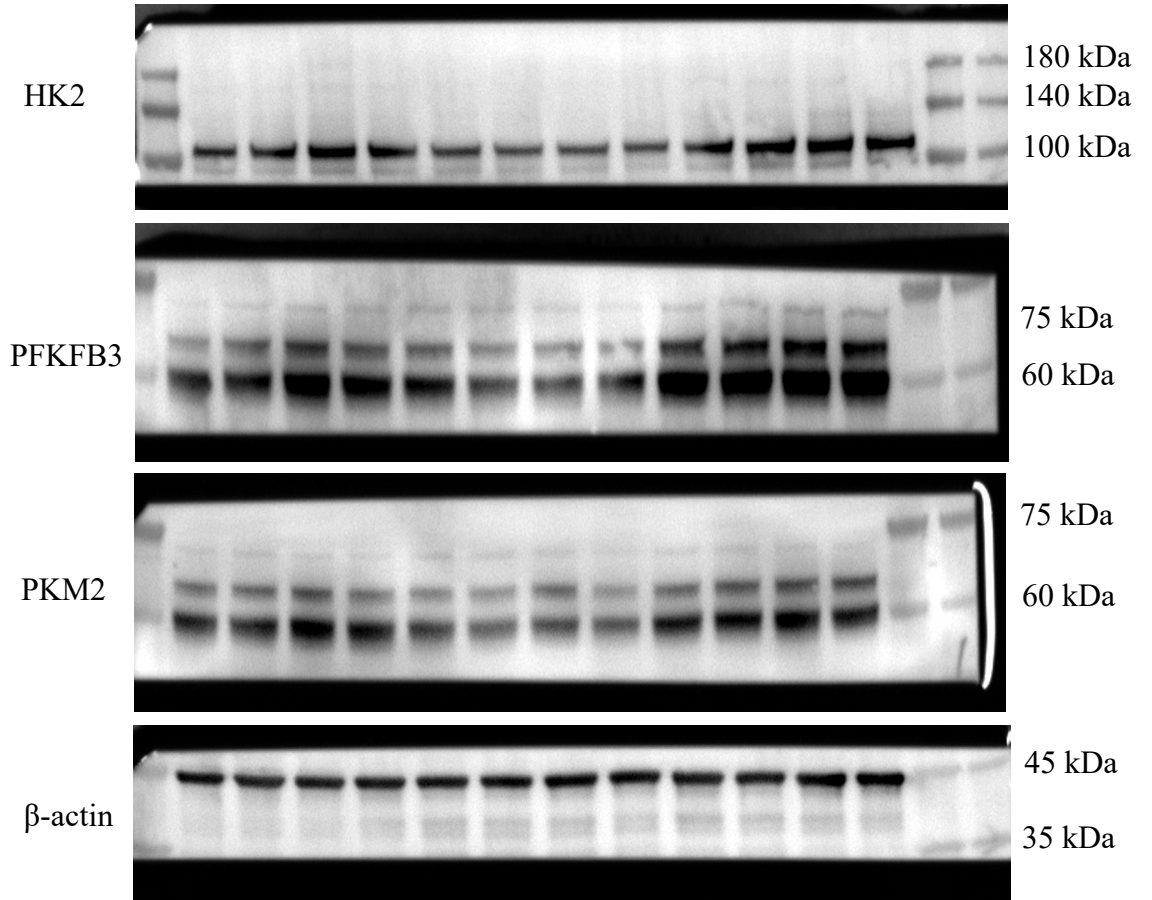
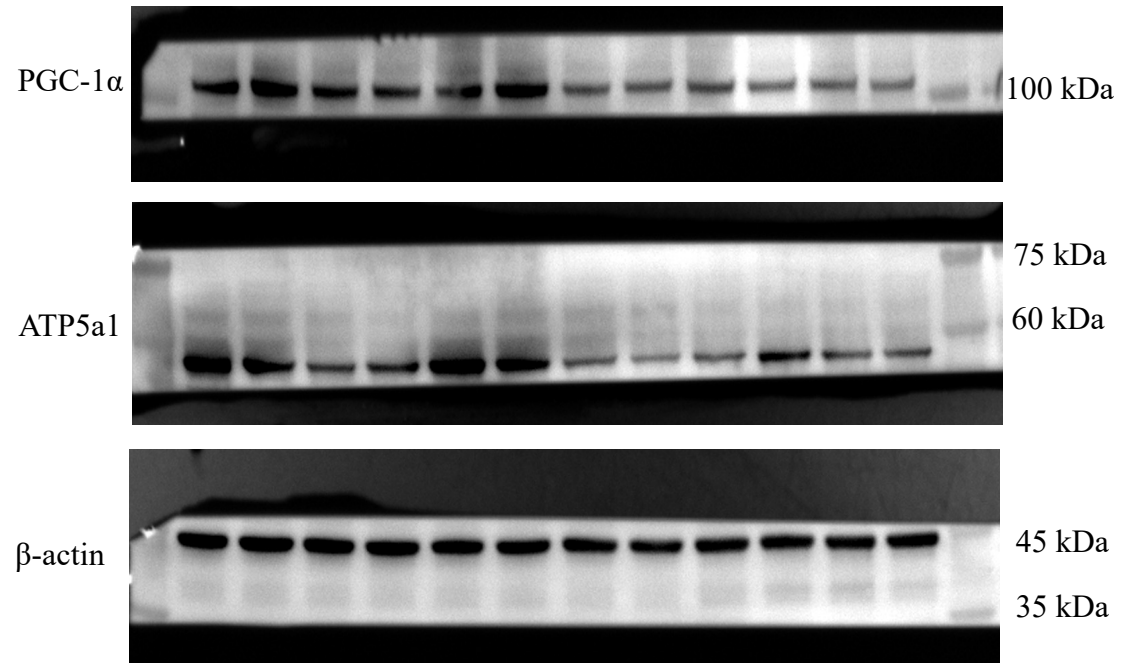


Figure 8D

