

# Supporting Information - Increased Light-Extraction of Thin-Film Flip-Chip UVB LEDs by Surface Texturing

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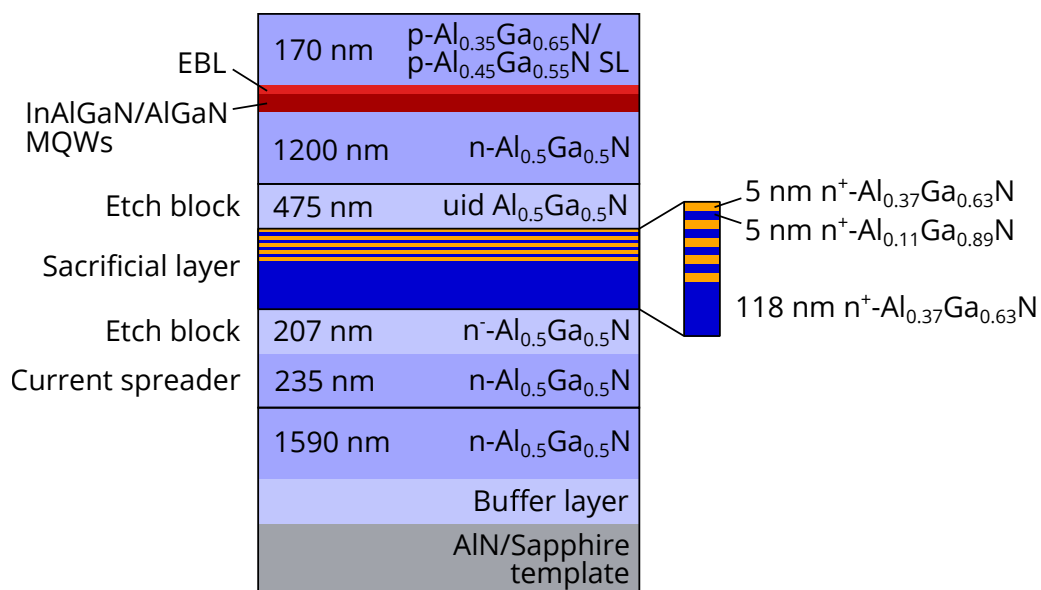
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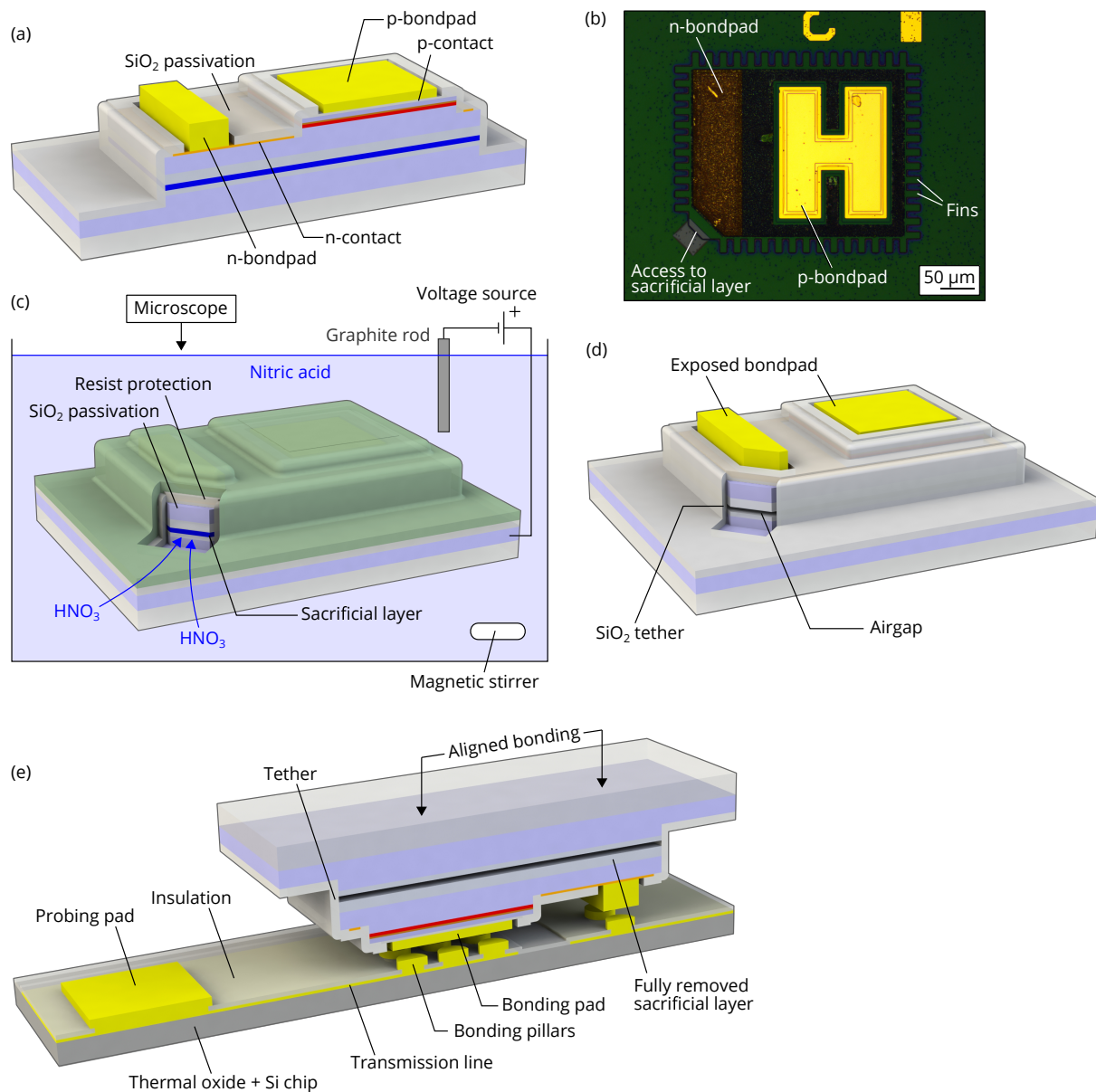
## Supplementary Note 1: Epitaxial growth



**Figure S1:** Epitaxial structure for fully-transparent TFFC-LEDs.

Figure S1 shows the epitaxial structure of the TFFC LEDs which was grown by metalorganic vapor-phase epitaxy in a close-coupled shower head reactor and the doping was achieved using silane ( $\text{SiH}_4$ ) as an n-dopant and cyclopentadienylmagnesium ( $\text{Cp}_2\text{Mg}$ ) as a p-dopant. In a first step, a pseudosubstrate was grown on a c-plane AlN/sapphire substrate with a relaxed  $\text{Al}_{0.5}\text{Ga}_{0.5}\text{N}$  toplayer [1]. To later enable substrate removal, a 235 nm  $\text{Al}_{0.5}\text{Ga}_{0.5}\text{N}:\text{Si}$  current spreading layer for the electrochemical etching was grown. After that a multilayered sacrificial layer comprising a 118-nm thick  $\text{Al}_{0.37}\text{Ga}_{0.63}\text{N}$  layer and a five-period structure of alternating 5-nm thick  $\text{Al}_{0.11}\text{Ga}_{0.89}\text{N}$  and 5-nm thick  $\text{Al}_{0.37}\text{Ga}_{0.63}\text{N}$  was grown in between two  $\text{Al}_{0.50}\text{Ga}_{0.50}\text{N}$  etch block layers with a thickness of 207 nm and 475 nm respectively. Whereas the top etch block layer is unintentionally doped, the bottom etch block layer has an n-doping level of  $0.5 \times 10^{18} \text{ cm}^{-3}$  to enable current flow to the sacrificial layer. The Si concentration in the sacrificial layer was  $2 \times 10^{19} \text{ cm}^{-3}$  for all layers. On top of the sacrificial layer and etch block layer, the LED heterostructure was grown. This consisted of a 1200-nm-thick n-doped  $\text{Al}_{0.5}\text{Ga}_{0.5}\text{N}$  current spreading layer (Si concentration:  $2 \times 10^{18} \text{ cm}^{-3}$ ) followed by a threefold InAlGaN MQW active region, a 25-nm-thick  $\text{Al}_{0.80}\text{Ga}_{0.20}\text{N}$  electron blocking layer, and a 170 nm Mg-doped  $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}/\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$  superlattice. The threading dislocations density of the epitaxial layers is around  $3 - 5 \times 10^9 \text{ cm}^{-2}$ .

## Supplementary Note 2: Process flow for TFEC LEDs



**Figure S2:** (a) Schematic and (b) microscope image of an LED after n- and p-side processing. (c) Schematic of the electrochemical etching setup and (d) schematic of an underetched LED. (e) Schematic of the aligned bonding process to transfer the LEDs.

The fabrication process started with the definition of the device mesa using Cl-based dry etching. The etching depth was chosen to fully expose the sacrificial layer. This was followed by a second dry etching step to define the lateral extent of the active region and to expose the n-side of the LED. Two different mesa shapes, a rectangular mesa and an interdigitated mesa, were fabricated to investigate the lateral current spreading and carrier injection. The V/Al/Ni/Au (15/90/20/30 nm) n-contact was evaporated and annealed for 40 s at 800°C in an N<sub>2</sub> atmosphere [2]. In the same process step, also the contact for applying the bias voltage during the electrochemical etching was formed. After that, a Pd/Al/Ni/Au (3/150/100/100 nm) p-contact was evaporated on the p-AlGaIn. To improve the planarity of the devices for the bonding, the n- and p-contacts were leveled using a Ti/Au metal pad on the n-contact. Both contacts were finished by Ti/Au (10/600 nm) bondpads to provide a base for the thermocompression bonding. In the next step, a 500-nm thick SiO<sub>2</sub> layer was deposited by reactive sputtering and patterned using Ar/CHF<sub>3</sub>-based dry etching (see Fig. S2(a)). This dielectric layer promoted unidirectional lateral

electrochemical etching, acted as a tether to keep the thin-film LEDs in place after the sacrificial layer removal and served as an insulation layer to prevent short-circuiting after the flip-chip bonding.

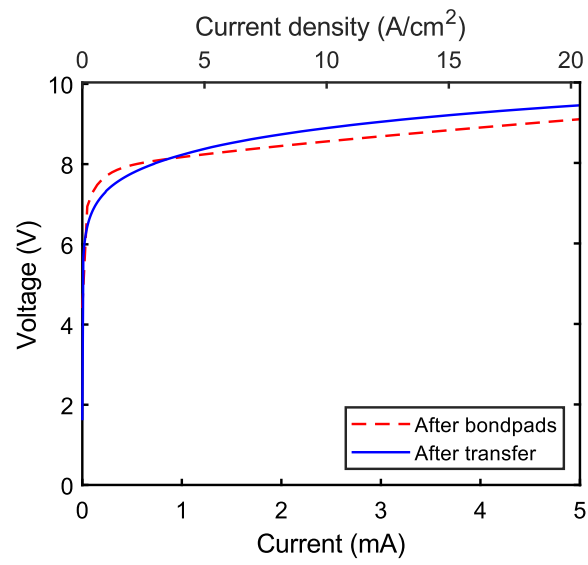
Before the sacrificial layer removal, a 3.5  $\mu\text{m}$ -thick photoresist layer was deposited to protect the surface of the devices, especially the n-contact, from parasitic etching during the electrochemical etching. The thick resist layer further supports the  $\text{SiO}_2$  tethers to keep devices in place. Figure S2(c) shows an LED at this stage, just before the electrochemical etching. The sacrificial layer was then laterally etched using a bias voltage of 15 V vs. a graphite rod in 0.3M nitric acid. The etching was done at room temperature and the electrolyte was stirred using a magnetic stir bar without intentional illumination. The etching process was intentionally started from one corner of the device to proceed unidirectionally from this point beneath the device. The progress of the etching was monitored in-situ using an optical microscope to time the etching. After the complete removal of the sacrificial layer, the sample was immersed in de-ionized water to remove acid residues, followed by acetone and isopropanol cleaning. These solvents removed the resist protection and reduced the force on the membrane during the subsequent drying in air. After the cleaning process, the thin-film LEDs were held by the  $\text{SiO}_2$  tether layer, see Fig. S2(d), which surrounds the device mesa. Because the tether area depends on the device perimeter, one group of devices included fins to increase the perimeter as shown in Fig. S2(b).

Figure S2(e) shows a schematic cross-section of the carrier chip onto which the thin-film LEDs were bonded. The carrier chip had electroplated Au-pillars of a height of 3  $\mu\text{m}$  and diameter of 15  $\mu\text{m}$ , which were arranged in a hexagonal pattern with a pitch of 30  $\mu\text{m}$ . These pillars for the bonding were used instead of continuous large-area bonding pads to facilitate deformation and adaption during the thermocompression bonding [3]. Ti/Au metal lines were used to connect to the LEDs, which were electrically separated by the  $\text{SiO}_2$ -on-Si substrate and a  $\text{SiO}_2$  layer on the top to further prevent potential short-circuiting of the LEDs after the flip-chip bonding.

Both the LED chips and the carrier chips were cleaned by UV-ozone to remove organic residues before the bonding. The thermocompression bond was accomplished under a mechanical pressure of around 100 MPa for 1 hour at 300°C in ambient air. After the bonding, during which the  $\text{SiO}_2$  tethers break, the growth substrate of the UV LED is separated from the carrier chip while the single LEDs remain bonded to the carrier chip.

Individual LEDs were selectively roughened to investigate the impact of different degrees of roughness on the device performance. The lithography was selectively done using direct laser writing using a 5.3  $\mu\text{m}$ -thick positive photoresist to avoid parasitic etching of other devices and device parts, especially the bonding and contact metal layer, during the roughening step. Because the TMAH-based developer (Microdeposit MF-CD-26) for the photoresist etches the N-polar AlGaIn surface, a PMMA interlayer was spun before the photoresist to separate development and roughening. Therefore, after the resist development which stopped on the PMMA surface,  $\text{O}_2$  plasma was used to remove the PMMA layer in the open area. These open areas were then exposed to the developer at room temperature for 9 minutes for one group of LEDs and 15 minutes for another group. After the roughening, the resist was stripped in solvents and  $\text{O}_2$  plasma.

### Supplementary Note 3: I-V characteristics



**Figure S3:** I-V-characteristics of an LED after bond pad fabrication and after sacrificial layer removal and transfer.

## References

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